5307 Brings Clock Doubling to ColdFire

Motorola's First ColdFire v3 Chip Enlarges Cache, Triples Clock Speed

by Jim Turley

Motorola's ColdFire family continues to grow but never seems to grow more expensive. Even as the chips get faster and sprout more integrated peripherals, Motorola has managed to keep prices well below $20 in volume. The newest member, the MCF5307, is no exception.

With a 90-MHz clock rate and larger, 8K cache, the 5307 is by far the fastest chip in this bargain line. It compares favorably with Motorola's stalwart 68EC040, nearly doubling its performance at a fraction of its price. The 5307, sampling now, should hasten the conversion from 68K to ColdFire.

First Chip to Use Third-Generation ColdFire Core

The 5307's biggest changes are internal. It is the first chip to use the ColdFire v3 core (see MPR 11/17/97, p. 8), which extends the pipeline, enlarges the instruction buffer, and allows clock multiplication. The new chip also sports a hardware multiply-accumulate unit—a first for ColdFire—and an integer divide instruction (with supporting hardware).

As Figure 1 shows, simulations indicate the 5307 executes a collection of test programs 2–3 times faster than a previous-generation (v2) ColdFire part. Of course, the 5307 has an internal clock rate that's nearly three times higher (90 MHz vs. 33 MHz), a cache that's four times larger (8K vs. 2K), and a bus interface that's 50% faster. Given all these advantages, the 5307 had better perform 2–3 times faster!

Working both for and against the 5307 is its longer pipeline. The longer pipe means mispredicted branches stall two clocks longer than before, but the chip's faster clock rate, bigger buffer, and branch hinting alleviate some of the burden. "Hinting" is a new feature with the v3 core that allows programmers to toggle the chip's default assumption about forward branches. Many processors assume all branches will not be taken. With the 5307, programmers can globally set the default taken/not taken direction for the chip. For code that normally does not fall through branches, this feature can add a small but measurable performance improvement.

Bus Interface Changes, Peripherals Accumulate

In what has become a ColdFire tradition, the 5307 has a different bus interface than all of its predecessors. Of the six ColdFire chips in production, each one has a substantially different bus; no two are hardware compatible. Part of the reason for this is that responsibility for ColdFire processors was split among different divisions during Motorola's most recent reorganization. Each division has its own customer base and target markets with, evidently, different needs regarding hardware interfaces.

The 5307's bus most closely resembles that of the 5206 or 68040 (more precisely, the 68EC040). It has nonmultiplexed 32-bit address and data buses that follow a synchronous protocol. Unlike the '040, the 5307 doesn't support asynchronous transfers or have cache-coherence signals, a TBI (transfer-burst inhibit) input, or a TEA (transfer-error acknowledge) input. This last omission makes the bus a bit more Intel-like than most Motorola microprocessors. Failed transfers (such as a parity error or a nonresponding slave) must time out or be signaled via interrupts. The chip supports external arbitration for multiple masters, a feature the 5206 also carries.

The 5307's 8K unified cache is the largest so far in the growing ColdFire family, as Table 1 shows. Both write-through and write-back update policies are supported, and half the cache can be locked, at the programmer's option.

A built-in DRAM controller offers welcome relief to hardware designers. The 5307's memory controller can handle fast page-mode, EDO, or synchronous DRAMs with equal aplomb. Coupled to 50-MHz SDRAMs, the chip can sustain 2-1-1-1 burst read or burst write cycles; with asynchronous memories, 3-2-2-2 timing must do.

Rounding out the on-chip peripheral mix are 4K of SRAM, dual UARTs, a four-channel DMA controller, eight programmable chip-select pins, 16-bit general-purpose I/O pins (multiplexed with the address bus), and an I^2C serial-peripheral interface, as Figure 2 shows. The peripheral mix is calculated to appeal to designers of imaging and storage applications.

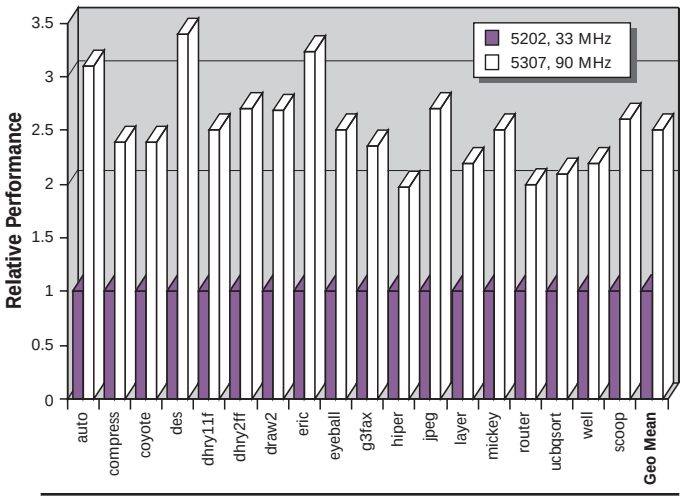

Figure 1. With its newer core, faster clock rate, and larger cache, the 90-MHz 5307 runs 2–3 times faster than a 33-MHz 5202 ColdFire part. (Source: Motorola)

Price & Availability

Motorola's ColdFire 5307 processor is sampling now at 66 and 90 MHz. Production is scheduled for 2Q98. In 10,000-unit quantities, the CF5307 is priced at $14.33 and $17.21, respectively. For more information, contact Motorola's Imaging and Storage Division (Austin, Texas) at 512.895.6422 or point your Web browser toward *www.mot.com/SPS/HPESD/prod/coldfire/MCF5307*.

ColdFire Joins 0.35-Micron Crowd

To reach a nearly triple-digit clock speed, Motorola had to fabricate the 5307 in 0.35-micron CMOS, a first for a ColdFire part. First samples of the part rolled out in January; production volumes will be available in a few months. The process shrinks the chip's die size to 27 mm^2 and its supply voltage to 3.3 V. Even though the 5307 runs at 3.3 V inside and out, it still tolerates 5-V I/O signals.

The 5307 introduces the concept of clock multiplication to the ColdFire family. Specifically, the CPU frequency can be divided by 2, 3, or 4 to yield the external bus frequency. Thus, the user of a 90-MHz chip can run its external bus at 22.5, 30, or 45 MHz, speeds well within the reach of most first-year hardware designers.

Another Blow to the 680x0 Family

Motorola highlights the 5307's "nearly 2×" performance improvement over the 68040, its closest ancestor and best-known relative. The company rates the 90-MHz 5307 at 70 Dhrystone MIPS, compared with 44 MIPS for the 68040 at 40 MHz, the fastest speed at which the '040 is available. (For the new year, Motorola has finally kicked its habit of using Dhrystone 1.1, which returned results about 10% higher than Dhrystone 2.1.)

	5102	5202	5203	5204	5206	5307
Min freq	20 MHz	16 MHz	16 MHz	16 MHz	16 MHz	66 MHz
Max freq	40 MHz	33 MHz	33 MHz	33 MHz	33 MHz	90 MHz
CPU rev	v1	v2	v2	v2	v2	v3
I-cache	2K	2K	2K	512	512	8K
D-cache	1K	unified	unified	none	none	unified
SRAM	none	none	none	512	512	4K
Address	32 bits	32 bits	32 bits	22 bits	27 bits	32 bits
Data	32 bits	32 bits	16 bits	16 bits	32 bits	32 bits
DRAM ctrl	no	no	no	no	yes	yes
Serial chan	none	none	none	1 port	2 ports	2 ports
DMA chan	none	none	none	none	none	4 chan
Timers	none	none	none	1 timer	2 timers	2 timers
Price (min)	$10.61	$6.28	$5.99	$6.63	$9.24	$14.33
Price (max)	$18.28	$8.10	$7.72	$8.54	$11.49	$17.21
Availability	now	now	now	now	now	2Q98

Table 1. Motorola's six ColdFire devices are similar but differ in the specifics of peripheral mix, cache size, and CPU core.

That rating gives the 5307 almost twice the integer performance of a 68040 at one-tenth of the price. The 68040 has an FPU, but at $180, it comes at a stiff premium. Even the pared-down 'EC040 and 'LC040 carry prices in the $40–$90 range and still top out at 40 MHz. As a faster-but-cheaper replacement for the 'EC040, the 5307 can't be beat. Unless designers badly need the 68040's floating-point unit or its automatic bus snooping, there's little reason to keep writing the big checks to Motorola.

ColdFire Leaves the Glory to Others

Outside of the Motorola camp, the 5307 is still a good bargain. There aren't many 32-bit processors that sell for around $15 in quantity, fewer still with as much integrated I/O as the 5307 carries with it, and none that can reach 90 MHz. Other chips in the 5307's price range are Intel's i960Sx, 'Kx, and 'JA parts (two of which have FPUs), IBM's PowerPC 401GF, a few of IDT's older MIPS chips—and the rest of the ColdFire family. With prices starting at $5.99 in quantity, Motorola has firmly staked out its territory at the low end of the 32-bit embedded landscape.

Given its genetic heritage, ColdFire will never be a performance leader, even after Motorola's ministrations with the v3 core design. The company sagely acknowledges this limitation and instead markets ColdFire as a package deal: a processor bundled with useful peripherals and good third-party tool support.

Performance is exciting, but good embedded designs call for more than just MIPS. For makers of moderately-priced consumer electronics, ink-jet printers, faxes, modems, and the other ubiquitous accoutrements of the modern age, ColdFire chips offer a good, solid value. Not exciting, perhaps, but reliable performers that are attractively priced and well supported. M

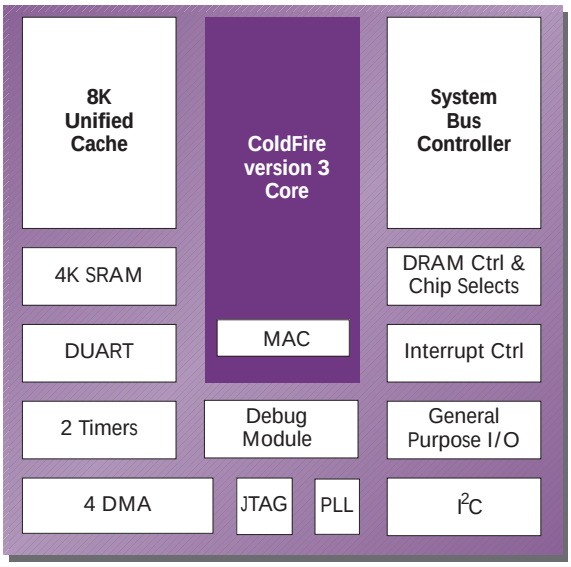

Figure 2: The 5307 has a large, unified 8K cache, 2K of SRAM, and a built-in DRAM controller, making it a single-chip controller.