Current source based standard cell model for accurate signal integrity and timing analysis

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***Abstract*— The inductance and coupling effects in interconnects and non-linear receiver loads has resulted in complex input signals and output loads for gates in the modern deep sub-micron CMOS technologies. As a result, the conventional method of timing characterization, which is based on lookup tables with input slew and output load capacitance as indices, is no longer adequate. The focus has now shifted to current source based standard cell models which are based on the fundamental property of transconductance of MOSFETs. In this paper [1] we propose a systematic methodology for obtaining a current based delay model for gates, which can accommodate both single (SIS) and multi-input (MIS) switching signals of arbitrary shape and complex non-linear output loads. We use an analytical model for the gate output current expressed as a function of the node voltages. This results in an average error less than 0.5% with maximum standard deviation of 2.5% in error when compared with SPICE for a large number of standard cells. When compared with SPICE, using the proposed models gives stage delay and output slew with an average error of less than 3% and 2% respectively for arbitrary inputs and output load combinations.**

I. Introduction

The scaling of CMOS technology has led to high speed, high density integrated circuits but every successive generation has given rise to new design challenges. The design tools today have to account for many complex phenomenons such as short channel effects, inductive and capacitive coupling of interconnects, power supply noise, process variations etc. Therefore, accurate modeling of cell libraries has become an extremely important and challenging task for accurate timing, power and noise analysis of modern deep sub-micron designs. The characterization of standard cells has therefore evolved with the technology generations starting from simple linear CMOS models to table lookup based noise, power, timing models to the more recent current source based models (CSMs) [2].

Multi-input switching and crosstalk effected input waveforms can have a significant impact on the performance (e.g. delay, slew) of a logic gate [5], [16]. The delay and output slew of a gate not only depend on the transition rate but also on the exact shape of the input signal. As shown in [16], the gate delay can change significantly with changes signal shape for fixed transition time. A further complication arises due to the fact that load at the output of the cell can be a distributed R(L)C network whose leaf nodes drive subsequent stages presenting non-linear receiver capacitances to the network. Replacing such loads with a single effective capacitance is very difficult. Therefore, the conventional timing library format which stores the data for a cell in 2-D lookup tables (LUT) with indices as input transition time (S_{in}) and effective load capacitance (C_{eff}) and outputs as output transition time (S_{out}) and gate delay is no longer sufficient to model a driver. To this effect, significant work has been done to approximate complex input waveforms by an equivalent waveform [11], to reduce the complex output loads to equivalent load capacitance [4], [9] and to find the delay for MIS using the SIS data [17], [7]. However, none of these methods provide an accurate and comprehensive method for obtaining cell response in the presence of complex input waveforms, output loads and MIS.

To alleviate some of these problems, the cells are characterized using CSMs [2], [3] where the gate output current as a function of time is stored for different pairs of output load and input slew. Although these models enable more accurate interpolation, they still require the input to be modeled as saturated ramp and the output as an effective capacitive load. Significant amount of work is being done to develop abstract CSM library models which are independent of the input waveform and output load. A cell is generally modeled using non-linear parasitic capacitances connected to a voltage dependent current source. Given an input signal and output load network, the gate transient response is then obtained by recursively evaluating the cell model parameters (parasitic capacitances and output current) and solving for node voltages in output network.

Substantial research effort is being made to develop CSMs which can provide high accuracy with minimum overhead. The authors in [14] proposed a model consisting of a DC current source, a linear resistance , an output capacitance and an associated gate delay. The values of the resistance and capacitance are determined to match the SPICE response of the gate. Another model proposed in [8] consists of a voltage controlled current source and an internal capacitance. The effect of non-linear parasitic capacitance is modeled by adding a time shift to the output. These models were not very accurate as they did not consider the miller effect on the parasitic capacitance. An improvised model consisting of a capacitor

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between the output and the input along with a load output capacitor was proposed in [13]. This model was better than the earlier models and captured the effect of non-linear inputs very well but required multiple iterative transient simulations to fit the capacitances in the model. The authors in [15] captured the non-linearity of the parasitic capacitances by adding a voltage dependent capacitor at the output of the gate and the input was connected to a 2 stage RC ladder to account for internal circuit delay. This model was suitable for SIS but it is not clear how it can be applied to MIS.

To avoid additional characterization, [12] proposed methods of extracting current based models from an existing voltage based timing library. Since the data in a voltage based timing library gives the information of equivalent output slew and delay and not the exact output waveforms, extracting the current models from that data can result in errors. A more accurate model consisting of a non-linear voltage dependent current source and non-linear voltage dependent capacitance at each node of a cell is presented in [5]. Although very accurate, this model requires significant characterization time and results in large size of libraries.

In this paper we propose a model which consists of accurate non-linear parasitic capacitances and only one non-linear current source to model the driver. An accurate analytical model for gate output current expressed as a function of the node voltages using orthogonal polynomials is described. A method for directly extracting the non-linear capacitances from transient SPICE simulations and storing them in a lookup table is also discussed. This is based on exploiting the arrangement of the transistors inside the cell to reduce the number of capacitors to be characterized and thereby reduce the size of the library. We show that for SIS we need only two capacitors and for MIS with n inputs overlapping we need a maximum of $n+1$ capacitors.

The rest of the paper is organized as follows. Section II contains the description of our model. The methodology for extracting the model parameters is explained in section III and section IV. Section V explains the use of the proposed model for MIS. In section VI we elaborate the recursive process of obtaining transient response. The results using the proposed model are compared with SPICE in section VII followed by the conclusions in section VIII.

II. Proposed Model

The DC current through the output node of a complex gate depends on the voltages at the gate's input and output nodes. This can be measured as the current flowing through the voltage source connected at the output of the gate in a SPICE DC simulation. The value of DC current at the gate output (for a set of input and output voltages) is a cell characteristic which is independent of the slope of input signal and the output load. However, in a transient simulation this current is used to charge/discharge the output load and intrinsic parasitic capacitances connected at the output of the gate. Therefore, the total current through the capacitances (at the output) at any instant of a transient simulation is equal to the DC current for the corresponding instantaneous voltages i.e,

$$I_{dc}(V_i(t), V_o(t)) = I_{load}(t) + I_{parasitic}(t) \quad (1)$$

where $I_{dc}(V_i(t), V_o(t))$ is the DC output current at instantaneous input voltage $(V_i(t))$ and output voltage $(V_o(t))$ at time t. $I_{load}(t)$ is the current through the output load capacitor, and $I_{parasitic}(t)$ is the current through the parasitic capacitances, at time t.

For a large load capacitance, I_{load} is much larger than $I_{prasitic}$ because the current is divided in the ratio of the capacitances. This is further illustrated in Fig. 1 where, we compare the transient output current through a load capacitor for a switching *aoi22* gate with the DC current obtained at instantaneous node voltages. As explained above, the current through the load capacitance is almost equal to I_{dc} when the capacitance is large (150fF) and much less than I_{dc} when the load capacitance is comparable to the cell's intrinsic capacitance i.e 10fF. This is an important result as it provides a

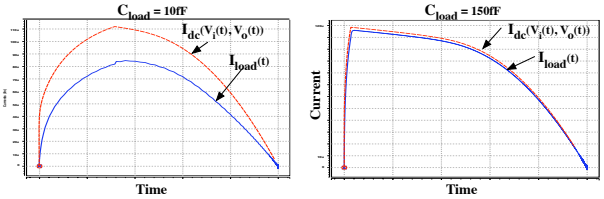


Fig. 1. Transient current compared with DC current for different capacitive loads

method for relating the characteristic output DC current of the gate to the transient current through the output load network. For pre-characterized DC output current of the gate, we need to evaluate the current through the parasitics at all instants to obtain the available load current in a transient analysis. This requires understanding of the parasitic capacitances of the gate. The output of a CMOS transistor has two sources of parasitic capacitance, namely, the gate-drain capacitance (C_{gd}) and the junction capacitance (C_{jd}) of the drain terminal of the MOSFETs connected to the output of the logic gate. Consider for example an *aoi22* gate shown in Fig. 2. There are total 4 junction capacitances and four drain-gate capacitances at the output node Z of the gate. The value of these capacitances depends on the voltages at the terminals of the transistor and therefore varies during an input(output) transition. The dependence of these capacitances on terminal voltages can be modeled as follows:

$$C_{jd} = Wd\sqrt{\frac{\epsilon_{si} q N_a}{2(\psi_{bi}+V_j)}} \quad (2)$$

$$C_{gd} \approx \begin{cases} WC_{ox}L_{ov} & \text{if, } V_{GS} < V_{th} \\ & \text{or, } V_{GS} > V_{th}, V_{DS} > V_{GS} \\ \frac{WC_{ox}L_{eff}}{2} & V_{GS} > V_{th}, V_{DS} < V_{GS} \end{cases} \quad (3)$$

The p-substrate (n-well) is connected to the lowest (highest) potential in the circuit and is therefore constant at all times. Thus, C_{jd} which is a function of reverse junction voltage depends only on the output voltage. The value of C_{gd} depends on the mode of operation and therefore the terminal voltages of the transistor. For single input switching in the worst case, inputs a2, b2 and a1 are constant while input b1 switches to change the output. Therefore, the miller capacitances (C_{gd}) for non-switching inputs are determined by the output node voltage alone and can be connected in parallel with the drain junction capacitances. Therefore, for the given *aoi22* gate we can combine together $C_{jdQ4}, C_{jdQ3}, C_{jdQ6}, C_{jdQ5}, C_{gdQ6}, C_{gdQ5}$ and C_{gdQ4} and replace it with a single non-linear capacitor $C_o(V_{in}, V_{out})$

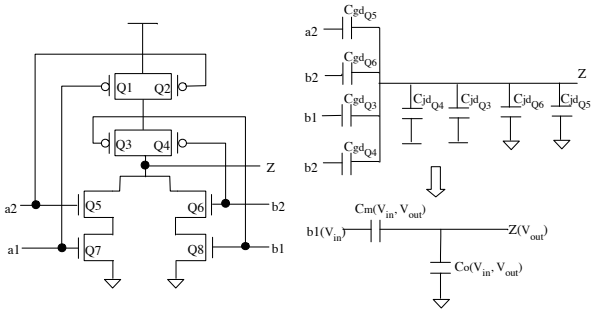


Fig. 2. Schematic and parasitic output capacitances of an aoi22x05 gate

connected between the output and the ground. We now have to deal with only two parasitic capacitances which can be easily extracted directly using the method explained in Section IV. Similarly, we can reduce the output capacitance of any complex gate to two non-linear capacitances for single input switching. From this we obtain our model of the gate shown in Fig. 3 consisting of two non-linear capacitances and one non-linear current source. The capacitor

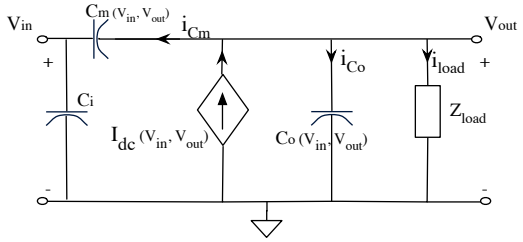


Fig. 3. Proposed gate model for single input switching

C_i in the model represents the receiver capacitance seen by the input. The output transient response is obtained by first solving the circuit in Fig. 3 by numerical integration methods to obtain output voltage $V_o(t + \Delta t)$ starting from initial condition$(t = 0)$. Secondly, the value of $V_{in}(t + \Delta t)$ is sampled and new values of C_m, C_o and I_{dc} for time $(t + \Delta t)$ corresponding to $V_{in}(t + \Delta t)$ and $V_o(t + \Delta t)$ are determined from the characterization data of the gate for the next simulation step. This process is repeated recursively till the output level is reached to complete the transient analysis.

The proposed driver model directly captures the behavior of a single channel-connected block (CCB) e.g. INV, NAND, NOR, AOI etc. However, for complex circuit cells having more than one CCB e.g. stage buffers, latches, adders etc. we need to break the transistor-level netlist of the cell into multiple CCBs as proposed in [1] and then generate current based model for each of those CCBs. The transistor-level netlist breaking and model parameter extraction is performed during cell characterization.

III. Analytical model for non-linear I_{dc}

For a MOSFET in the sub-nanometer technology the drain current is a non linear function of the voltages applied at the terminals. The equation for current is different for different operation conditions i.e. sub-threshold, linear and saturation. Short channel effects and second order effects like drain induced barrier lowering make these equations more complex. Apart from the sub-threshold region where the current is modeled as an exponential function of the voltages, current in other operating regions is modeled as a polynomial of the node voltages. Also, since the value of current and voltages in the sub-threshold region are very small we can expand the exponential function ignoring the higher order terms. For a given value of node voltages we need to evaluate the current for each transistor in a complex gate to obtain the current through the output of the gate. This requires analyzing the operation region of each transistor and solving the appropriate current equation which can be very expensive for large complex gates. Therefore, we model the DC current sourced (drained) from output terminal of the gate as a cubic polynomial function of the node voltages. The node voltages are treated as deterministic variables in the range of supply voltages with some margin added to account for the overshoot and undershoot.

The gate current is modeled as an orthogonal polynomial series in the variables corresponding to node voltages. Polynomial functions of deterministic variables can be modeled using either Legendre or Chebyshev polynomials [18] as the bases functions. For reasons that will be given later, we choose Legendre polynomials. Since the interval of orthogonality for Legendre's polynomial is [-1,1], we need to normalize the variables. For supply range $[V_{ss}, V_{dd}]$ (including the margins for overshoot and undershoot) the variable for voltage at node i is represented as:

$$V_i = \frac{V_{ss} + V_{dd}}{2} + \Big(\frac{V_{dd} - V_{ss}}{2}\Big)\zeta_i \quad \text{where, } \zeta_i \in [-1, 1] \quad (4)$$

For *m* node voltages the gate current I_{dc} can be expressed as an infinite series expansion in orthogonal basis polynomials $\Psi_k(\vec{\zeta})$ in *m* dimensional vector $\vec{\zeta}$ as,

$$f(\vec{\zeta}) = \sum_{k=0}^{\infty} \lambda_k \Psi_k(\vec{\zeta}), \quad (5)$$

where the coefficients λ_k can be shown to be the inner product of $f(\vec{\zeta})$ and $\Psi_k(\vec{\zeta})$, based on the orthogonality of $\Psi_j(\vec{\zeta})$ and $\Psi_k(\vec{\zeta})$ $(j \neq k)$ [10]. Thus $\lambda_k = \langle f(\vec{\zeta}), \Psi_k(\vec{\zeta})\rangle$, where the inner product is defined as,

$$\langle f(\vec{\zeta}), \Psi_k(\vec{\zeta})\rangle = \int f(\vec{\zeta}) \cdot \Psi_k(\vec{\zeta}) \cdot w(\vec{\zeta}). \cdot d\vec{\zeta} \quad (6)$$

In Equation (6), w is a weight function that is integrable and positive on $[-1, 1]$. Convergence implied in Equation 5 is with respect to the norm associated with the inner product. The node voltage of a gate is generally modeled as saturated ramp and therefore the most appropriate weight function is a constant equal to the slope of the ramp, which is precisely the reason why Legendre polynomials are used since their corresponding weight function is constant equal to 1. In contrast, the weight function associated with Chebyshev polynomials is exponential (e^{-x^2}).

Since we do not have a functional relation describing *f*, we evaluate the integral in Equation 6 using $N + 1$ order multi-dimensional Gaussian quadrature where *N* is the order of expansion of *f* (*N*=3 in our case). The integral in Equation 6 is then approximated as,

$$\int f(\vec{\zeta}) \cdot \Psi_k(\vec{\zeta}) \cdot w(\vec{\zeta}) = \sum_{i=1}^{q} f(\vec{\zeta_i}) \cdot \Psi_k(\vec{\zeta_i}) \cdot w_i \quad (7)$$

where $\vec{\zeta_i} = (\zeta_{1i}, \zeta_{2i}, \ldots, \zeta_{mi})$ is a zero (quadrature node) of the the orthogonal polynomial and w_i is the value of weight function at i-th point. The value of current function at q $(= m^{N+1})$ quadrature points is obtained by SPICE DC analysis

For single input switching, we have only two variables V_{in} and V_{out}. Therefore, the third order univariate Legendre's polynomials and the corresponding third order bivariate orthogonal polynomials can be represented as,

$$\begin{aligned}\Gamma_3(\zeta_1) &= \{1, \zeta_1, (3\zeta_1^2-1), (5\zeta_1^3-3\zeta_1)\}\\ \Gamma_3(\zeta_2) &= \{1, \zeta_2, (3\zeta_2^2-1), (5\zeta_2^3-3\zeta_2)\}\\ \Gamma_3(\zeta_1,\zeta_2) &= \Gamma_3(\zeta_1)\otimes\Gamma_3(\zeta_2) \qquad (8)\\ &= \{1, \zeta_1, \zeta_2, (3\zeta_1^2-1), (3\zeta_2^2-1), \zeta_1\zeta_2, (5\zeta_1^3\\ &\quad -3\zeta_1), (5\zeta_2^3-3\zeta_2), \zeta_1(3\zeta_2^2-1), \zeta_2(3\zeta_1^2-1)\}.\end{aligned}$$

Thus, the non-linear DC current can be expressed as,

$$\begin{aligned}I_{dc}(\zeta_1,\zeta_2) = {} & a_0 1 + a_1\zeta_1 + a_2\zeta_2 + a_3(3\zeta_1^2-1) + a_4(3\zeta_2^2\\ & -1) + a_5\zeta_1\zeta_2 + a_6(5\zeta_1^3-3\zeta_1) + a_7(5\zeta_2^3\\ & -3\zeta_2) + a_8\zeta_1(3\zeta_2^2-1) + a_9\zeta_2(3\zeta_1^2-1), \quad (9)\end{aligned}$$

where ζ_1 and ζ_2 correspond to variables for V_{in} and V_{out} respectively. Similarly, for multi-input switching we can obtain the expression for I_{dc} as a function of multiple node voltages. The proposed method is general enough to be applied to channel connected cells of any size and complexity. Our model when compared with SPICE over 2000 MC sample points for SIS and 5000 points for MIS, gave an average error of of 0.13% and 0.28% respectively across several gates. The average of standard deviation in error for all gates was 1.86% and 2.09% for MIS and SIS respectively.

IV. Characterization of Capacitances

The intrinsic capacitances in a gate are complex non-linear functions of the input and output node voltages as described in section II. In this section we elaborate the characterization process of reduced capacitances for the proposed model. The current through a nonlinear (voltage dependent) capacitor can be given from [6] as,

$$\begin{aligned}Q = {} & C(v) * V\\ I = {} & \frac{dQ(V)}{dV} * \frac{dV(t)}{dt} = C(v) * \frac{dV(t)}{dt} \qquad (10)\end{aligned}$$

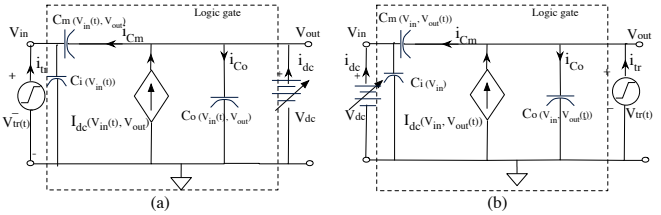
Using this formula, the Miller capacitance between the transient input and output node is evaluated using the setup shown in Fig. 4(a). A DC voltage source is connected at the output of the gate and a ramp signal at the input . The voltage of the DC source is swept from 0 to V_{dd} and transient analysis is performed for each sweep point. Solving the KCL at the output node we get,

$$I_{dc}(t) = i_{Cm}(t) + i_{Co}(t) - i_{V_{dc}}(t) \qquad (11)$$

where $i_{V_{dc}}(t)$ is the current from the DC voltage source, $i_{Co}(t)$ is the current through the equivalent grounded capacitor, $i_{Cm}(t)$ is the current through the equivalent Miller capacitance and $I_{dc}(t)$ is the gate output current corresponding to the instantaneous input voltage($V_{in}(t)$) and applied DC voltage (V_{out}), obtained from pre-characterized gate data. Using Equation 10 we can write Equation 11 as,

$$\begin{aligned}I_{dc}(t) + i_{V_{dc}}(t) &= C_m(t)(\frac{dV_{out}}{dt} - \frac{dV_{in}}{dt}) + C_o(t)\frac{dV_{out}}{dt}\\ &= -C_m(t)\frac{dV_{in}}{dt} \qquad (\because \frac{dV_{out}}{dt} = 0)\\ \text{hence, } C_m(t) &= \frac{I_{dc}(t) + i_{Vdc}(t)}{-k} \qquad (12)\end{aligned}$$

where $C_m(t)$ is the Miller capacitance corresponding to



(a) (b)

Fig. 4. (a) Setup for extracting $C_m(V_{in}, V_{out})$ (b) Setup for extracting $C_o(V_{in}, V_{out})$

$V_{in}(t)$ and V_{out} and k is the slope of the input ramp signal. Evaluating Equation 12 at different time instants during the input transition, gives the data for one column of the lookup table. Repeating this process for different output DC voltages generates the complete table for Cm. To extract the equivalent grounded capacitor Co, we exchange the voltage sources as shown in Fig. 4(b). The KCL for this circuit at the output node is,

$$\begin{aligned}I_{dc}(t) &= i_{Cm}(t) + i_{Co}(t) - i_{tr}(t)\\ \Rightarrow I_{dc}(t) + i_{tr}(t) &= C_m(t)(\frac{dV_{out}}{dt} - \frac{dV_{in}}{dt}) + C_o(t)\frac{dV_{out}}{dt}\\ &= (C_m(t) + C_o(t))\frac{dV_{out}}{dt} \quad (\because \frac{dV_{in}}{dt} = 0)\\ \Rightarrow \frac{I_{dc}(t) + i_{tr}(t)}{m} &= C_m(t) + C_o(t) \qquad (13)\end{aligned}$$

where $Co(t)$ is the equivalent grounded capacitance corresponding to $V_{out}(t)$ and V_{in} and m is the slope of the voltage source connected at the output. The value of $Co(t)$ can be obtained by subtracting the value of Miller capacitance extracted in the previous step but since we need their sum for solving the transient circuit we prefer to store the sum of the two capacitances in the lookup table.The slope of the transient voltage source is taken to be sufficiently large to obtain the characterization data at fine granularity. Although the response is evaluated at each time step, we store the data in the LUT at very few points and use linear interpolation in between. The surface plot of these capacitances as a function of input and output voltages for an *aoi22* gate are shown in Fig. 5. From the surface plot of theses capacitances we can see that they are highly non-linear function of the node voltages and cannot be approximated as linear or constant capacitors because of the large variability in their magnitude.

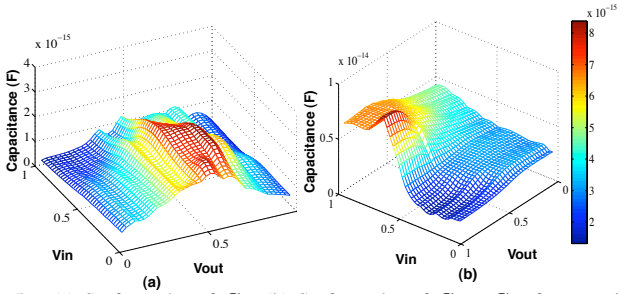


Fig. 5. (a) Surface plot of C_m (b) Surface plot of $C_o + C_m$ for an aoi22 gate

V. Modeling Multi-Input Switching

The suggested driver model for single input switching can be easily extended to handle multi-input switching (MIS). However, for MIS the maximum number of capacitors in the model is equal to to $n+1$. Where n is the number of Miller capacitances due to inputs with overlapping switching window connected to transistors at the output of the gate and one equivalent grounded capacitor connected at the output node. The maximum value of n depends on the design of the logic gate. Consider for example a four input $aoi22$ gate shown in Fig. 2. Although the gate has 4 inputs, as shown in Fig. 6 the maximum value of n is 3 (between b1, b2, a2 and Z) because input a1 is not connected to any transistor connected at the output.The gate output current and the parasitic capacitances are now functions of the output node and overlapping input node voltages. The analytical expression for gate output current as a function of switching node voltages can be obtained by adding respective variables to the expansion and solving for coefficients using the method explained in section II. Also, the

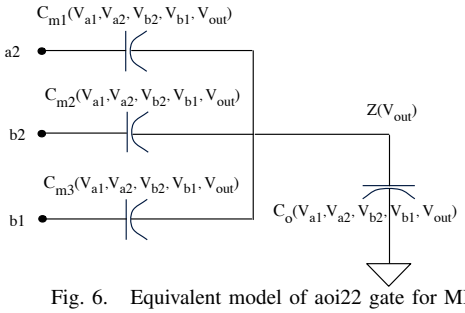


Fig. 6. Equivalent model of aoi22 gate for MIS

parasitic capacitance can be obtained from a series of transient SPICE simulations using the method explained in IV. Since the number of variables is more, the cost(time) of characterizing cells for MIS is significant but it is a one time process for every technology and therefore worth the effort. It is important to note here that our model for MIS considers the design of the cell to determine the parasitics of the driver unlike [5] where all nodes were replaced by a non-linear charge and current source thereby adding redundant data and increased runtime of the characterization process.

VI. Computing the Transient Response

The transient output response for the model is evaluated by using Euler's method of numerical integration. First, we characterize (i.e. compute the coefficients) the non-linear output current given by Equation 9 by running DC simulations at quadrature points. The number of quadrature points is fixed by the number of variables and the order of the expansion and the points are the roots of orthogonal polynomials. Next the capacitances C_m and $C_m + C_o$ are estimated using the method given in section IV. This results in two 2-D lookup tables with V_{in} and V_{out} as indices. Applying KCL at the output node of the model shown in Fig. 3 results in,

$$\begin{aligned} I_{dc}(V_{in}, V_{out}) &= i_{C_m} + i_{C_o} + i_{load} \\ &= C_m(V_{in}, V_{out})\Big(\frac{dV_{out}}{dt} - \frac{dV_{in}}{dt}\Big) \\ &\quad + C_o(V_{in}, V_{out})\frac{dV_{out}}{dt} + i_{load} \end{aligned} \tag{14}$$

For a capacitance C_l connected at the output of a gate, the value of the output voltage at intervals of time-step Δt is obtained as follows.

$$\begin{aligned} &I_{dc}(V_{in}(t), V_{out}(t)) = \\ &\quad (C_l + (C_m + C_o)(V_{in}(t), V_{out}(t)))\Big(\frac{V_{out}(t+\Delta t) - V_{out}(t)}{\Delta t}\Big) \\ &\quad - C_m(V_{in}(t), V_{out}(t))\Big(\frac{V_{in}(t+\Delta t) - V_{in}(t)}{\Delta t}\Big). \end{aligned} \tag{15}$$

With $\Delta V_{in} = V_{in}(t+\Delta t) - V_{in}(t)$, V_{out} is given by

$$\begin{aligned} &V_{out}(t+\Delta t) = \\ &\quad V_{out}(t) + \Big(\frac{I_{dc}(V_{in}(t), V_{out}(t))\Delta t + C_m(V_{in}(t), V_{out}(t))\Delta V_{in}}{C_l + (C_m + C_o)(V_{in}(t), V_{out}(t))}\Big) \end{aligned} \tag{16}$$

Starting from time $t = 0$ when both V_{in} and V_{out} are known, we first compute the gate output current by substituting equivalent normalized node voltages in the current Equation 9. The values of the parasitic capacitances corresponding to the node voltages at a given step are obtained from the pre-characterized lookup tables. If the node voltages are not in the table, the nearest neighbors are used and the corresponding capacitance values are averaged. Using this data, the output voltage at next time step $(V_{out}(t+\Delta t))$ is evaluated using Equation 16. The input voltage for next time step $(V_{in}(t+\Delta t))$ is sampled and new values of current and capacitances are obtained corresponding to $(V_{in}(t+\Delta t), V_{out}(t+\Delta t))$. This process is repeated recursively.

VII. Simulations and Results

We implemented the proposed models for 65nm technology using the BSIM4 predictive technology models [19]. The characterization process was carried out for different standard cells of varying drive strengths. The transient response was obtained by using Euler method for integration, taking sufficiently small step size and was implemented in MATLAB. All experiments were carried out on 2.16 GHz machine with 2GB memory. To evaluate the accuracy of the proposed analytical model for I_{dc}, we compare the model response with DC response obtained from SPICE for 2000 monte-carlo samples for SIS and 5000 samples for MIS. For MIS, all inputs were assumed to be switching with overlapping windows and therefore for an *n* input gate, current was modeled as a function of *n+1* voltages. For an AOI gate, Fig. 7(a) shows the contour plot of I_{dc} as a function of input and output node voltages (SIS) obtained from our model and SPICE and Fig 7(b) shows scatter plot of %error compared to the absolute value of DC current. Due to space constraint the results for average error

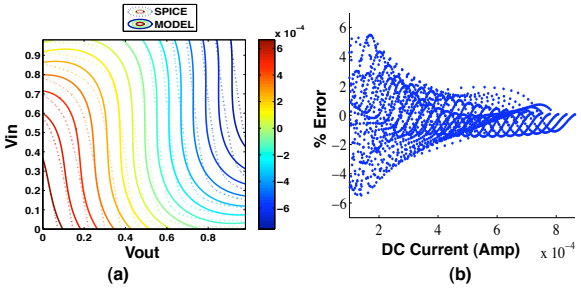


Fig. 7. (a)Contour of I_{dc} for AOI22 gate obtained as a function of input and output voltages from SPICE and our analytical model (b) Scatter plot for % error vs absolute DC current

and standard deviation of error for only a subset of the gates

characterized are shown in Table I. Our model gave an error of less than 0.5% mean with average standard deviation of nearly 2% for all gates in both switching conditions. Also, as shown in Fig. 7(b) the magnitude of error decreases for larger values of current and this is very important to get accurate results for delay.

Cell	I_{dc} SPICE vs our model (% Err for SIS)		I_{dc} SPICE vs our model (% Err MIS)	
	Mean	Std. Dev	Mean	Std. Dev
aoi22	0.02	1.85	0.24	1.95
inv4	0.13	1.70	-	-
oai22	0.08	1.76	0.32	1.96
nand4	0.29	2.12	0.48	2.33
xor2	0.11	1.87	0.22	2.16
nor3	0.14	1.9	0.17	2.05
Average	0.13	1.86	0.28	2.09

TABLE I

RESULTS COMPARING ANALYTICAL I_{dc} MODEL WITH SPICE

To compare the shape of the output waveform, the response of an aoi22 gate connected to a capacitive load for worst-case SIS obtained from our model and SPICE is shown in Fig. 8(a). To evaluate the robustness of our model we drive the gate by two input signals : (i) an inverter with the interconnect between the gate and the inverter modeled as a RC network coupled to an aggressor (ii) an oscillating piece-wise linear voltage source. As seen in Fig. 8(a), our model gave very accurate response for both input signals. The response obtained for rising and falling transitions in a NAND4 gate are also compared in Fig. 8(b). These figures show that the proposed model captures the shape of the output signal very accurately. We characterized a large variety of gates with different drive strengths and analyzed their response for different input voltages and output loads.

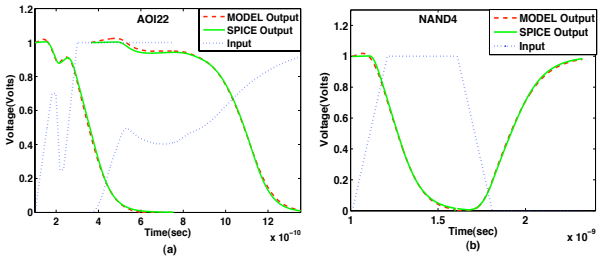


Fig. 8. Output voltage waveform of (a) AOI22 gate (b) NAND4 gate

Cell	Delay(SPICE vs our model)		$Slew_{out}$(SPICE vs our model)	
	Avg % Err	Max % Err	Avg % Err	Max % Err
aoi22	1.82	3.46	1.12	2.31
inv4	1.36	2.43	1.06	1.88
oai22	2.33	3.63	1.72	2.95
nand4	3.35	7.82	2.49	4.59
xor2	2.71	3.59	1.43	2.12
nor3	2.18	4.16	2.12	3.47
buf	1.16	3.12	1.189	2.19
DFF	1.96	3.37	1.53	2.77
Average	2.11	3.94	1.58	2.78

TABLE II

COMPARISON OF GATE DELAY AND OUTPUT SLEW

We calculated the transient response of the gates for three types of output loads: (a)capacitive (b) RC pi network (c) non-linear capacitive. The gates were driven by inverters considering coupled and uncoupled interconnects for both rising and falling transitions. The maximum error and absolute average error in delay and output slew for a subset of simulated gates is given in table II. We can see from the results, that complex gates like *oai* (or-and-invert) and *xor* (exclusive or) also give very accurate response using the proposed model. The average error in delay and output slew for all gates was less than 3% and 2% respectively. Thus, the proposed model accurately captures the delay, output slew and output waveform shape of the driver.

VIII. CONCLUSIONS

In this paper we propose an accurate current source based driver model for standard cells. A systematic methodology for characterizing the gates for single and multi-input switching is presented. An analytical model for gate output current as a function of node voltages is developed and compared with monte-carlo SPICE simulations for accuracy. The proposed model gave accurate delay and output slew along with near-spice shape of the output waveform for a large variety of gates. We are looking at extending this work for introducing process variations in the proposed model and techniques for developing analytical model for capacitances.

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