Design and Use of Memory-Specific Test Structures to Ensure SRAM Yield and Manufacturability

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Abstract

High-density and high-performance single-port and dual-port SRAM increasingly occupy a majority of the chip area in System-on-Chip product designs. Therefore, good yieldability and manufacturability of the SRAM are essential. At the same time there is tremendous competitive pressure to get the best SRAM density and performance. We have previously published and presented the industry's smallest and fastest embedded 6T SRAM bitcells in 0.18um and 130nm generation standard CMOS process [1]. We have described how these SRAM bitcells are robust by design even while aggressively driving density and performance. In this paper we discuss the design and use of SRAM-specific test structures that have enabled us to quickly evaluate process-design interactions [2] and to fine-tune process and/or design for improving yields and manufacturability. We have designed test structures using our aggressive production bitcell as basis to probe for any possible weaknesses of the process or design in SRAM. Results from these SRAM-specific test structures show good correlation to yield results and in-line SEM observations, and enable us to improve SRAM yields quickly. We have also designed SRAM-transistor test structures to characterize the SRAM cell devices in their real working environment. Results help to evaluate the circuit performance and provide us with guidelines for further design improvements. These data when used in the early stage of the development cycle are also useful for model validation.

1. Introduction

SRAM plays an increasingly important role in System-on-Chip (SoC) applications [3]. Statistics shows that on average SRAM has exceeded 50% of the total chip area. In [1], we reported on the development of the smallest high-density 6T-SRAM cells for SoC using standard CMOS processes ($3.87um^2$ for 0.18um technology node and 1.87 um^2 for 0.13um technology node). These cells are suitable in SoC applications to meet the demand for high-density and high-performance, and are highly manufacturable.

To ensure their manufacturability, robustness and reliability, ordinary Process Control and Monitoring (PCM) test structures are not sufficient to monitor the process for the high density SRAM, due to specific interactions between the process and the SRAM design [4]. Ordinary PCM are more generic in nature and are aimed at supporting the development of robust process module features and robust generic design rules (rules that can be used in any possible combinations and design environments). Therefore, these structures may not always allow us to test for the robustness of the chosen SRAM design rules in their specific SRAM array environment. For example, a conventional poly bridging structure is designed such to prove the robustness of the minimum poly-to-poly spacing design rule for very long and parallel poly lines. This structure may not be suitable for providing feedback for our SRAM, as typically the poly layer features are more complex in SRAM. The same may apply to metal bridging structures, where the SRAM pattern is more complex in nature than a simple array of parallel metal lines and uniform spacing.

A conceptual change in designing and using electrical test structures for SRAM-driven process development is thus needed: test structures need to be product-driven as well as process-development driven. The set of test structures used for developing and characterizing the process needs to be complemented with a set of suitable structures that prove the robustness of the high-density SRAM design and help quickly identify and correct process and design related yield issues in SRAM during the development phase.

2. Descriptions of Test Structures

The electrical parameters used to prove the robustness of our SRAM designs include, a.) leakage current to measure inter- and intra-layer bridging, b.) resistance measurement to detect integrity of connections, c.) SRAM transistor characterization to monitor any possible deviations from targets, and d.) beta ratio and static

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noise margin to evaluate the functional robustness of the SRAM design.

The designed test structures must be sensitive enough to allow monitoring of both systematic and random occurrences of any possible weakness of the memory cell. We also need to accurately characterize the SRAM transistors, beta ratios and static noise margins within the SRAM array environment. Therefore, in our SRAM qualification test chip, we have designed SRAM test structures to ensure SRAM cell robustness and characterize SRAM devices.

2.1. Ensuring SRAM Cell Robustness

To ensure the manufacturability of our SRAM cells, we have designed a series of test cells that are based on target SRAM cell. Each cell modification enables us to test one specific robustness requirement in the SRAM cell.

As illustrated in Fig.1, for the front-end process we identify among others: a.) poly-to-poly spacing at A and B, b.) poly-to-contact spacing at C and D, c.) island-to-island spacing at E, and the robustness of any SRAM-specific feature, such as shared contacts F and G.

For the back-end process (BOE) the critical design rules (Fig.2) include: a.) contact-to-contact spacing; b.) metal spacing; and c.) combined bridging between metal and contact of different pieces of metals (1,2,3,4) and contacts (i to iv) at three key locations A, B and C.

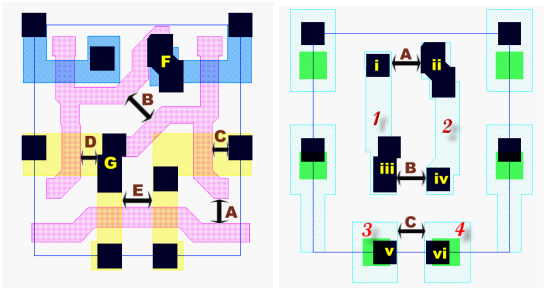


Fig.1 (left) Illustration of critical front-end design rules for our 130nm-generation 1.87um^2 production SRAM cell. A, B indicate the poly-to-poly spacing, C and D the poly to contact spacing. E the island-to-island spacing.

Fig.2 (right) Illustration of critical back-end design rules for our 130nm-generation 1.87um^2 production SRAM cell. A, B and C are metal 1 and contact related spacing, 1,2,3,4 are metal 1, i to vi are contacts (ii and iii are coupled contacts)

We use these modified SRAM cells to build larger arrays (~10,000 to 100,000 cells) just like repeating the SRAM cell in an SRAM array. The parameter of interest (leakage current, resistance, etc.) is then measured for the entire array. Hence, statistical information is gathered from a large number of cells, thus, increasing the confidence level of the quality of robustness for each individual design rule or feature.

These array structures help us to determine any additional SRAM cell design modifications that further improve its manufacturability, give feedback on the sensitivity of chosen critical design rules to process variations, and finally can also be used to quickly test the impact of proposed process modifications to the SRAM design.

Compared to traditional PCM test structure designs, the new concept has the following advantages. Test structures are more SRAM-cell-oriented, hence dedicated to prove the robustness of the cell design. The data is collected from the true SRAM array environment; hence captures process to design interactions, as is usually observed in real products. Finally, these structures allow evaluating all SRAM cell specific design rules as used in the SRAM array environment.

Another way to determine the robustness of critical design rules is by design split rather than process split. In this method we apply a constant bias to a critical layer and then study intra-layer and inter-layer effects. For example, we size the poly layer by 10% of its minimum feature size, and then study effects such as poly to poly bridging or contact to poly bridging, or monitor the impact of overall cell leakage as function of this bias. Typically, the same information could be collected by a split lot experiment at photo or etch. This method however, enables us to study the robustness of a specific design rule over a multitude of lots and allows us to study the additional margin of the design rule of choice when a process split is applied. We have applied this biasing operation on all critical layers, e.g. island, poly, contact and metal 1.

Finally, in addition to the above mentioned electrical test structures, we have also developed a powerful RAMPCM test chip methodology that allows us to gain additional statistical data to ensure the robustness of our SRAM designs.

The RAMPCM is a functional SRAM test chip that uses the same peripheral circuit and array size, as the regular SRAM test chips. The array however, is built from variations of the same basic cell. Each variation tests a specific SRAM-related design rule. For our 0.18um and 130nm RAMPCMs we identified 8 critical design rules and used four variations of each rule. Hence, a total of 32 variations were used to build the RAMPCM array. These were evenly distributed across the array, such as to average out systematic errors (column failures, row failures, block failures etc.).

The RAMPCM chip is subjected to the regular functional test program. A bitmap analyzer is then used to collect the number of failing bits per design rule variation. By this method we are able to collect statistical information of multiple megabits for each design rule

and determine the robustness of the rules used in our SRAM cells.

2.2. Characterizing SRAM Devices

We have designed test structures in order to measure SRAM cell transistors in their array environment and compare the results to the data from so-called isolated or semi isolated transistor structures of same dimensions. This allows us to quantify the effect that the high-density SRAM environment may have on these SRAM cell devices.

Furthermore we are able to measure the symmetry of the cell by means of comparing the data by the pairs of devices present in each memory (Fig.3). Typically all four rotations are monitored to take into account alignment conditions of the process. Finally, we use the coupled devices to measure so-called butterfly curves to determine the static noise margin of our SRAM cells.

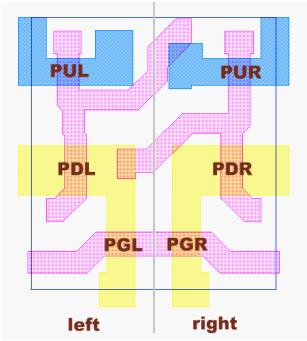


Fig.3 Illustration of the six transistors measured in 6T SRAM:
PD :Pull-down n channel transistor,
PU : Pull-up p channel transistor,
PG :Pass-gate n channel transistor,

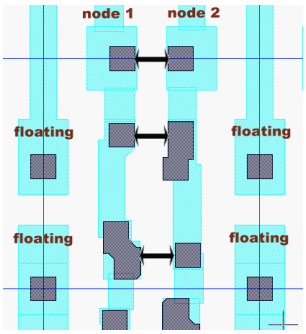
L= left, R= right.

3. Results and Discussions

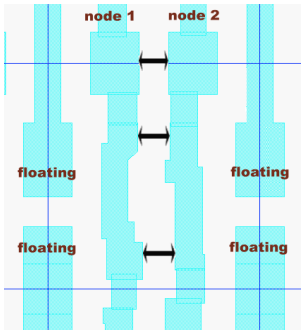
All critical design rules in our SRAM cells have been extensively studied with the test structures that have been described in the previous section. The robustness of our high-density SRAM cells, as established from yield and reliability results, is further confirmed by the results from our SRAM-specific test structures, as described below.

3.1. SRAM Design Rule Monitoring Results

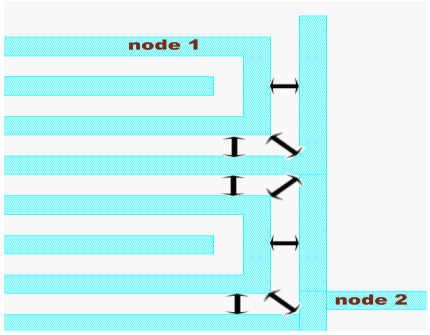
Fig.4(a) shows one of our SRAM cell-specific test structures that tests for metal 1 bridging within the cell. Usually metal bridging can be caused by either metal-to-metal short, or when contacts are present, also by contact-to-contact, or metal-to-contact interaction. In order to separate these effects, a complementary structure is designed without these contacts (Fig.4(b)). For reference, Fig.4(c) shows the metal 1 bridging test structure in a conventional PCM. Fig.5A shows typical electrical test results from very early lot. Only curve (a), corresponding to the SRAM-specific test structure of



(a)



(b)



(c)

Fig.4
(a) SRAM-specific test cell for metal 1 and contact interactive bridging test. Test cell is designed based on SRAM cell.

(b) SRAM-specific test cell for metal 1 bridging. This complements structure of (a). All contacts are removed such that only metal 1 related bridging is tested.

(c) Conventional metal 1 bridging test structure. Though the minimum metal-to-metal spacing is the same as that in SRAM, variations of metal width, density and environment are different.

sponding to the SRAM-specific test structure of Fig.4(a), shows an obvious bridging problem. Curves (b) and (c) do not reveal this marginality. This result indicates that this bridging mechanism involves contacts. Further investigations showed that the bridging was induced by a process-design interaction within the specific SRAM design. Either the conventional PCM or the metal 1 structures alone were unable to detect this fallout. This finding was used to improve the SRAM cell design and eliminate the leakage current tail, as shown in Fig.5B.

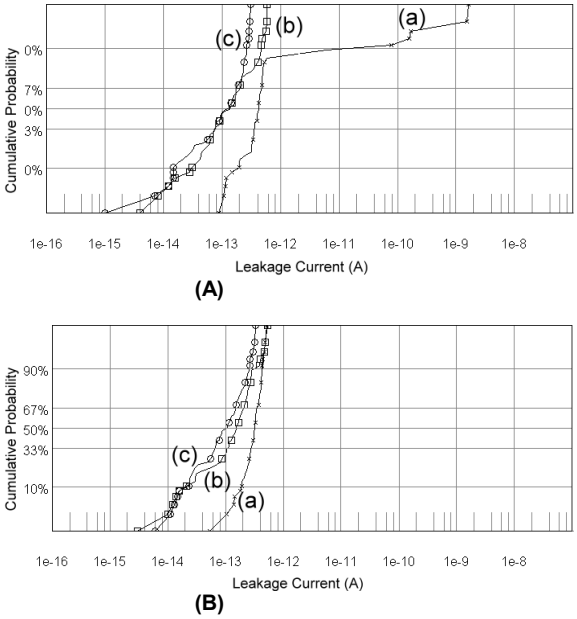


Fig.5 Metal 1 bridging leakage current of 100,000 unit-cells; curves (a), (b) and (c) correspond to test structures of Fig.4(a), 4(b) and 4(c), respectively. A: Early lot data; only the curve (a) shows the leakage fall-out while curves (b) and (c) do not show any fall-out. B: Data after design tuning; curve (a) shows significant improvement.

Next, we discuss results from our biasing study on critical layers. We use poly as an example. The critical locations where the biased poly layer is sensitive to bridging are illustrated in Fig.6(a). Fig.6(b) and Fig.6(c) show the poly-to-poly bridging and poly-to-contact bridging data of the three different biasing conditions. Based on the collected data we do not observe a significant increase of leakage current for the chosen biasing range and the poly-to-poly-spacing and poly-to-contact spacing rules used in the SRAM cell have excellent margin against process variations. The poly biasing will affect the transistor leakage too. Fig.6(d) shows this impact in the pass gate transistor. As seen, the leakage currents show a slight difference according to the poly-biasing and they are within the expected range predicted by device model.

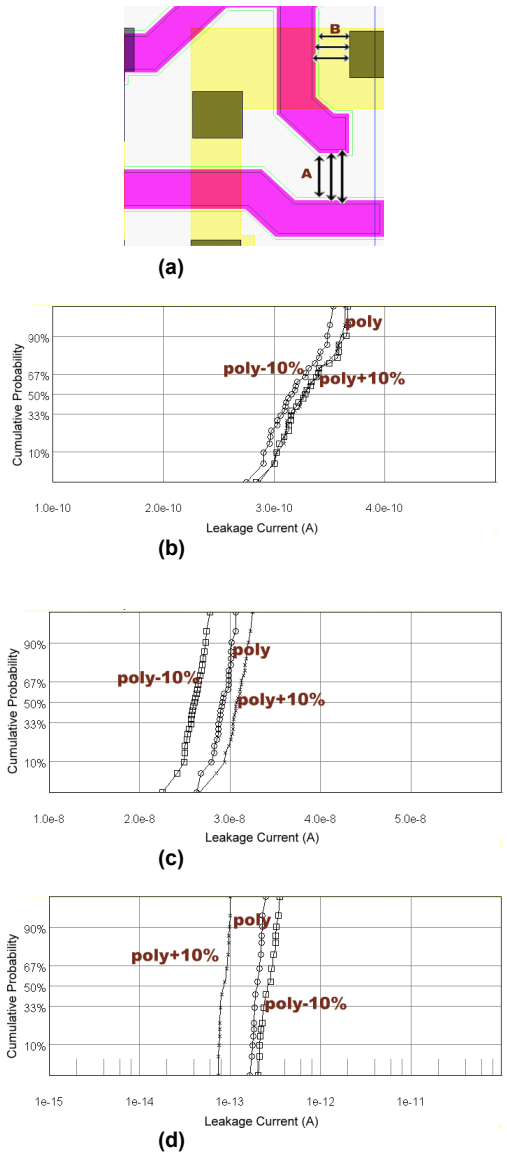


Fig.6
(a) Illustration of SRAM test structures for poly biasing. A: poly-to-poly spacing [ref. Fig.6 (b)]; B: poly-to-contact spacing [ref. Fig.6 (c)]

(b) Poly to poly bridging leakage current of 100,000 cells with different poly biasing. Result shows sufficient margin across the biasing range. Average leakage per cell is less than 1pA.

(c) Poly to contact bridging leakage current of 100,000 cells for different poly biasing. Results show again sufficient margin across the biasing range. Average leakage per cell is less than 1pA.

(d) Effect of poly biasing on the pass-gate transistor leakage current measured from 100,000 cells. Data is normalized to one cell. The data matches device models.

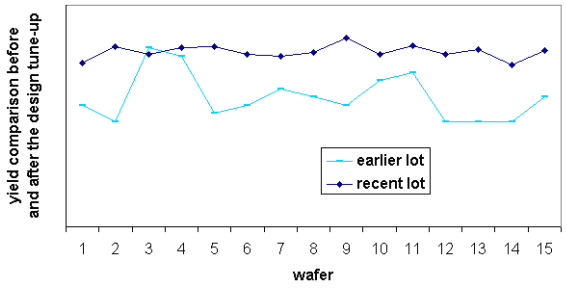


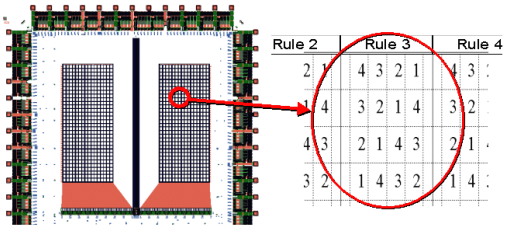
Fig.7 Yield improvement and stabilization after design tuning based on analysis of SRAM test structure data.

Based on thorough analysis of data from the SRAM-specific test structures, fine-tuning of design/process was quickly done resulting in improved and stable yields as shown in Fig.7.

3.2. RAMPCM

The array layout for our RAMPCM in 130nm technology is shown in Fig.8 (a). The eight design rules are placed in the array in stripe fashion, each design rule block is 64 columns by 512 rows. For each variation within one design rule we build a 16 by 16 bit sub-array. These sub-arrays are then evenly distributed across the design rule block.

We have used the data from three lots to analyze the RAMPCM chips. This resulted in a total of 17 Mb of data per design rule variation. We then normalized the data with respect to the background. The collected data from all critical design rules that were analyzed, as presented Fig.8(b), clearly shows that the design rules used in our 1.87um^2 cell are very robust and have sufficient manufacturing margin.



(a)

Relative Failure Rate

Rule Tightness	DR 1	DR 2	DR 3	DR 4	DR 5	DR 6	DR 7	DR 8
x	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
x - Δ	0.9	1.0	1.0	1.1	1.0	1.0	0.9	1.1
x - 2Δ	1.2	1.0	1.7	1.3	1.3	0.9	1.0	1.0
x - 3Δ	1.1	1.3	1.5	1.6	1.4	1.1	1.0	1.1

the design rule used in the 1.87 μm^2 cell

(b)

Fig.8 (a): RAMPCM array used for our 130nm SRAM technology. Different critical design rule variations are placed in each sub-array. (b): relative failure rate of the critical design rules used for our 1.87um^2 core cell. All rules used in the high-density SRAM cell are confirmed to be robust with sufficient manufacturing margin.

3.3. SRAM Cell Device Results

Fig.9 compares the pass-gate device drive current of our SRAM cell to an isolated device of same size. The results show an excellent matching of the two devices within the cell, and the devices within the SRAM cell match very well to the isolated device of same size. Since isolated devices are typically used for transistor model extraction, our SRAM devices are therefore, accurately represented by the device models.

As mentioned earlier, we also monitor the stability of the cell by means of measuring so-called butterfly curves. A typical result is shown in Fig.10. A minimum of 200mV signal to noise margin is achieved for our high-density SRAM cell in 130 nm generation.

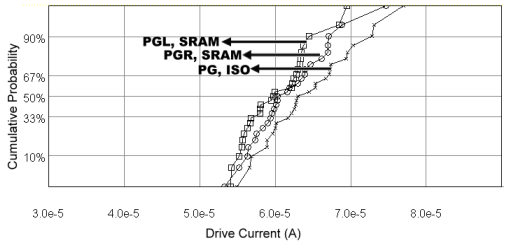


Fig.9 Left and right pass-gate transistor drive currents measured in our SRAM cell are compared to an isolated device of same size. Left and right devices match very well and perform very close to the isolated counterpart. This results in symmetric cell behavior and matching to device models.

Measuring the SRAM devices within the SRAM cell environment provides us the necessary feedback on cell symmetry and stability. The data collected from our test structures further underlines the robustness of our high-density SRAM cell.

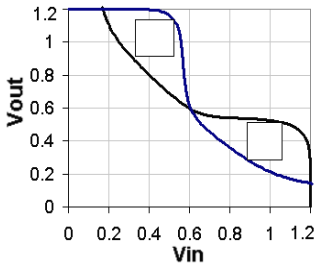


Fig.10 Typical measured butterfly curve (in Volt) of our high-density SRAM cell. Excellent signal-to-noise margin is achieved and symmetric cell behavior is observed as in Fig.9.

3.4. Specific Test Structures for 90nm SRAM Technology

For our 90nm SRAM development, we have designed some specific test structures for reliability studies and gate current characterization.

To obtain quick and earlier feedback on the reliability of an SRAM cell design we have designed test structures for our 90nm technology and beyond to detect random or systematic defects. The test array is fabricated based on high-density SRAM cells. The array is then subjected to bias-temperature stressing where a voltage is applied on the sample at high temperature while the degradation of parameters (leakage, current…) are monitored during the stressing. This allows us to evaluate chip-level reliability and study systematic defects at a very early stage in the SRAM development. We also build a series of test structures complementary to the above structure in order to differentiate various degradation mechanisms, such as gate leakage, transistor channel leakage and junction leakage.

Another concern in 90nm technology node is the thin gate oxide and associated higher gate oxide leakage contribution. We therefore designed SRAM-specific test structures to evaluate the bit line leakage in the SRAM array, since this may affect the overall signal to noise margin. Fig.11 shows the various leakage mechanisms in an SRAM cell that are affected by the additional gate oxide leakage component. This is another aspect of how SRAM-specific test structures are useful in providing helpful feedback for developing aggressive, yet robust and manufacturable SRAM cells for SOC applications.

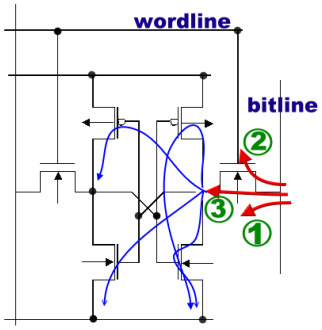


Fig.11 Bit line leakage mechanisms taking into account gate oxide leakage for 90nm-technology-node and beyond. Test arrays are generated in order to quantify the different mechanisms: 1.P-N junction associated leakage; 2.gate leakage of the pass gate transistor; 3. channel leakage of pass gate transistor via various gates.

4. Summary

We have designed and used SRAM-specific test structures as effective PCMs for SRAM technology development. The data obtained from these SRAM-specific structures has provided us quick and direct feedback on process-design interactions within our SRAM cell. We were also able to identify any possible yield-limiting factors and improve early SRAM yields rapidly by fine-tuning the process and SRAM design. Finally, the data from these SRAM-specific structures provides proof of the robustness and manufacturability of our SRAM cells.

5. Acknowledgements

The authors thank Arvind Kamath, Girish Patel and Rosie Cordova for useful discussions and support.

6. References

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