5Gbps Serial Link Transmitter with Pre-emphasis

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Abstract- High-speed serial link that achieves Gbps has the advantage of low cost and thus become popular. In this paper, we will implement the high-speed data serial link transceiver and demonstrate the pre-emphasis circuit. The overall circuit is implemented in TSMC 0.18um 1P6M 1.8v CMOS process. The performance of the transceiver can reach 5Gbps over the 10-meter long cable.

I. INTRODUCTION

Due to the multimedia applications, demand of bandwidth for the transmission has increased. This demand has resulted in the development of high speed and low cost serial link technology [1-7]. For the video of high resolution, the data rate may range from hundreds Mbps to Giga-bps to satisfy the need for playing real-time image of high resolution. In this high data rate application, the high-speed links play important role in computer-to-peripheral connections, local area networks, memory-busses, flat plane, etc. Nowadays, the known advanced high-speed links are listed in Table. 1. The standards are all for high-speed link over short distance in copper cable. The common characteristics are low swing differential signals with current mode driver and receiver because of the finite bandwidth of the channel.

Table. 1 Industrial standard for high-speed serial link

Standard	Speed
USB 2.0 (High Speed)	480Mbps [10]
IEEE 802.3	1Gbps [12]
IEEE 1394b	1.6Gbps –3.2Gbps [11]

With data rate up to Gbps range, the propagation of the signaling is affected by two limitations. The first limitation is in the package and the other is cable. The chip package dominates the output pin performance because of the pin's loading and bonding wire. The pin's loading causes one RC time constant that lowers the location of the 3dB frequency. Thus, when the loading is larger, the 3db bandwidth is smaller. The bonding wire results in the pattern dependent data jitter and lowers the signal to noise ratio. When the frequency is higher, the bonding wire and cable becomes more and more critical in the performance of the whole system.

We propose a pre-emphasis architecture that can enlarge the high frequency components, so the overall frequency response in the receiver is uniform within our desired frequency range. The pre-emphasis circuit can handle cable length from 1m to 15m. The paper is organized as follows. Section II shows the architecture of the transmitter. The circuit design of functional blocks are described in Section III. Section IV shows the implementation and simulation results. Finally, a conclusion is made in section V.

II. ARCHITECTURE DESIGN

This section describes the proposed transmitter for a binary 5Gbps serial link. Fig. 1 shows the block diagram of the transmitter, where the circuit elements designed are in solid blocks. This transmitter starts with high-speed parallel data stream, and follows a 5:1 multi-phase multiplexer which transmits the 5Gb/s data into the transmission line using a 1 GHz clock. The multiplexer needs five phases of the 1 GHZ clock. The architecture also contains a 2-tap pre-emphasis decision blocks, parallel data synchronizer and driver. However, the length of the transmission line is not always the same, the design issue is discussed in the second part of this section.

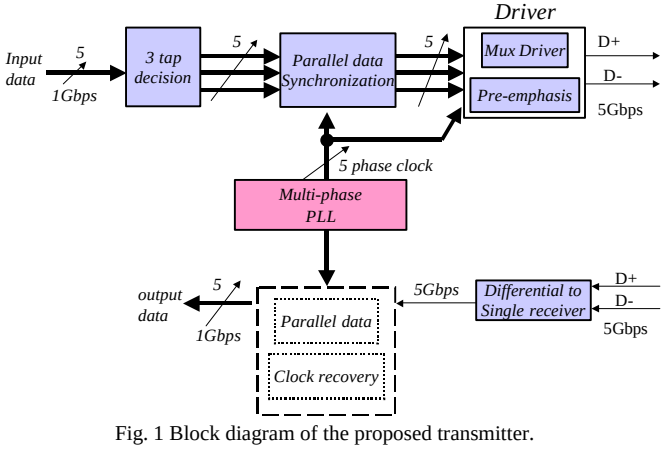


Fig. 1 Block diagram of the proposed transmitter.

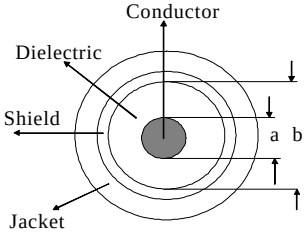


Fig. 2 Coaxial cable structure

We can calculate the skin-resistance of the cable (RG/223/U) by using a=0.889mm, b=3mm in Fig. 2 [13][14], and for copper conductor and solid polyethylene (PE) dielectric e_r =2.25, m_r =0.99999, and s =5.8×10^7(S/m), where $e_0 = 1/3p \times 10^{-9}(F/m)$, $m_0 = 4p \times 10^{-7}(H/m)$. From the above parameters, we can obtain the skin-effect resistance,

$$R_{nf} = 0.934 \times 10^{-4} \sqrt{f}\ (\frac{\Omega}{m}) \quad (1)$$

Once we have R_{nf}, we can use Hspice Welement cable model to model the cable and the frequency response of a 5m cable[3][13]. Fig. 3 is the simulation result of 10cm cable

and the 3dB frequency is about 400MHz. The comparison of the attenuation in dB of the cable model and the measurement result is shown in Fig. 4. Their –3 dB frequencies are quite the same.

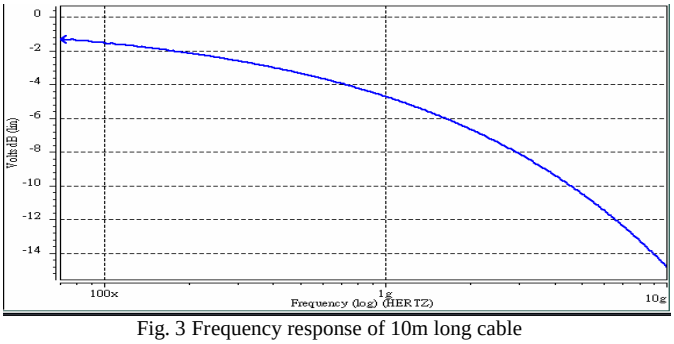
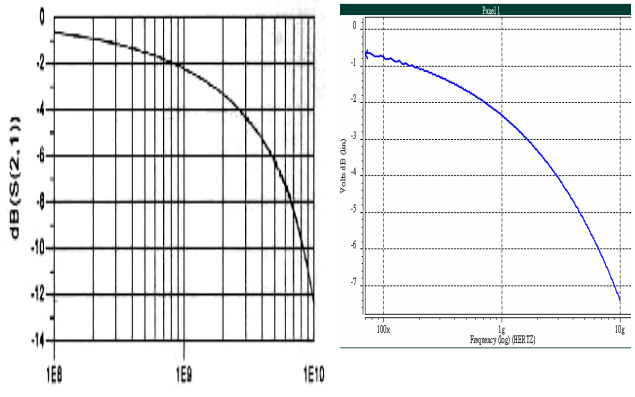


Fig. 3 Frequency response of 10m long cable



(a) (b)

Fig. 4 Frequency response of 5m long cable, (a) measurement and (b) HSPICE cable model.

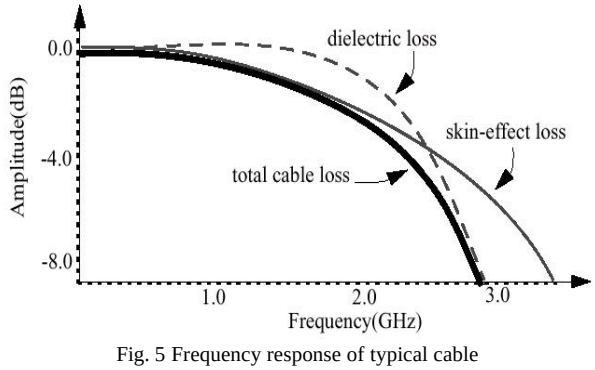


Fig. 5 Frequency response of typical cable

We know that the attenuation increases in higher frequency, and it is primarily due to the skin effect for frequency below 3GHZ as shown in Fig. 5. The skin effect distorted the signaling because the attenuation of the low frequency and high frequency is not uniform as shown in Fig. 4. Fig. 6 shows the distortion of the signaling caused by the skin effect. The way to overcome the bandwidth of the cable is to compensate for the frequency response of the cable. There are two ways to do this work. The first method is to pre-shape the signal in the transmitter so that the amplitude of the low frequency and high frequency response in the receiver is the same. The second way is to make an equalizer circuit in the receiver to equalize the received data. The transmitter pre-emphasis or receiver equalizer woks like a filter so that the wanted signal is passed and the unwanted signal is rejected.

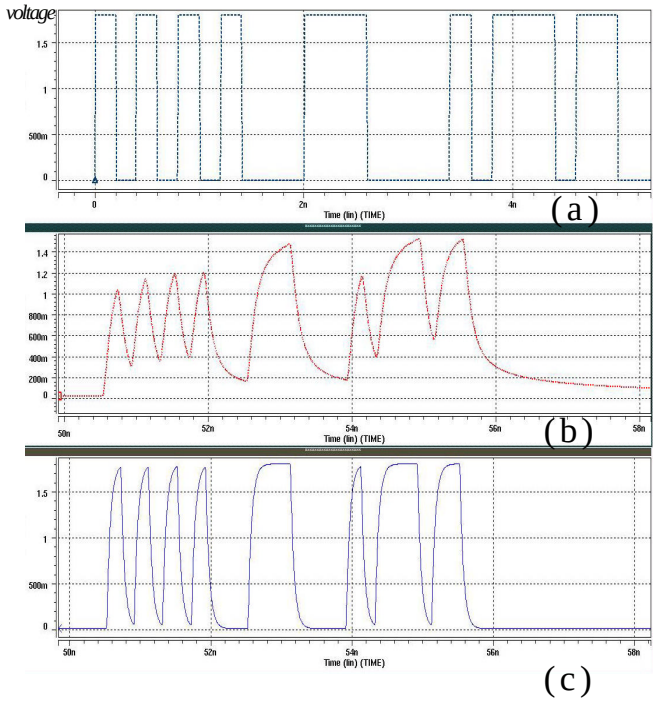


Fig. 6 (a)The output signal in transmitter, (b) the input signal in the receiver with skin effect and (c) the input signal in the receiver without skin effect

III. CIRCUIT DESIGN

A. Package effect

The chip-package interface is shown in Fig. 7. In general, 1mm bonding wire stands for 1nH. The location of the termination resistor (on chip or off chip) has the impact on the receiver's frequency responset. As shown in Fig. 8, when the resistor is on the chip, the gain in the frequency domain is degraded and the signal will be distorted in time domain. Moreover, when cable length decreases, this problem is more serious. When the operating frequency is higher, the voltage drops in the bonding wire is large. So the pulse to propagate over the transmission medium is seriously distorted because the bonding wire effect distorted the transmitting signaling.

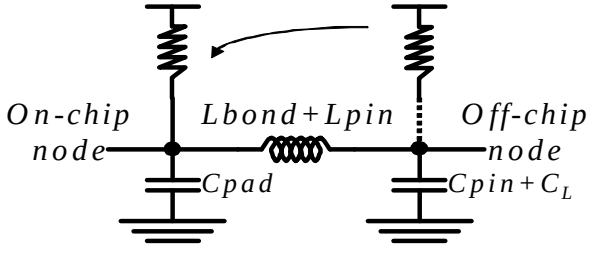


Fig. 7 Termination on chip (transmitter)

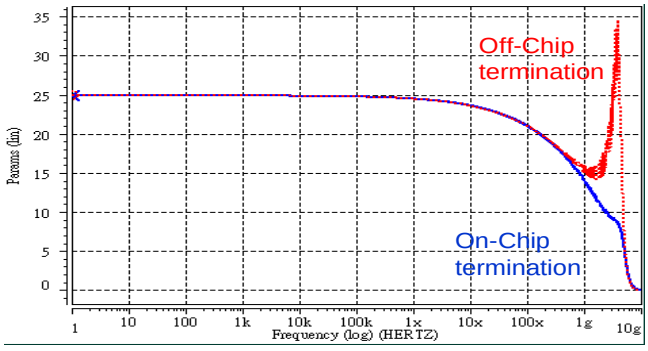


Fig. 8 The difference between the on chip and off chip node

B. Pre-emphasis

The transmission line is a low pass function. Pre-emphasis circuit plays a role of high pass filter, so in the receiver the frequency response is flatten within the bandwidth of our desired frequency range. The pre-emphasis either amplify the high frequency component or attenuate the low frequency component. The frequency response of the transceiver is depicted in Fig. 9. In Fig. 9 (a) [1][[3], the pre-emphasis filter attenuates the low frequency components and in this work as shown in Fig. 9 (b), the pre-emphasis amplifies the high frequency components. In the diagram, the dotted line means the overall frequency response.

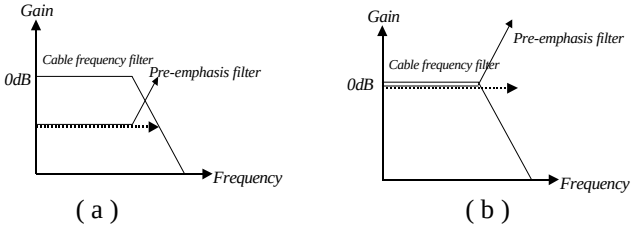


Fig. 9 The function of Pre-emphesis, (a) the low frequency part is attenuated and (b) the high frequency part is amplified.

We use the scheme of Fig. 9 (b). The primarily reason is that Fig. 9 (a) attenuate the low frequency part and the voltage swing in the receiver end may not be large enough to correctly recover the data. This similar architecture is used by the 4-PAM serial link[2]. As shown in Fig. 10 , in order to increase the high frequency components, we enlarge the transition of the signaling.

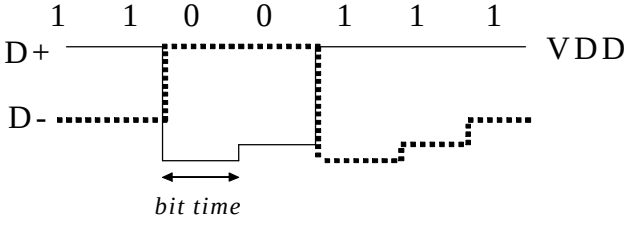


Fig. 10 The pre-shaped signal in the transmitter

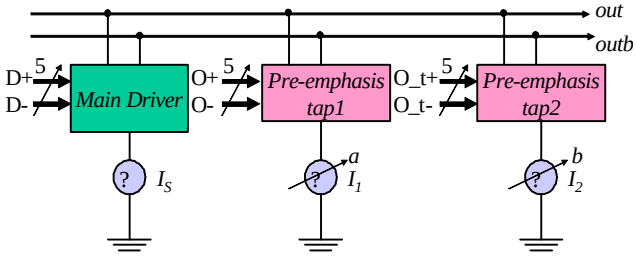


Fig. 11 Driver architecture: main driver and pre-emphasis

C. Tap decision

The driver includes the circuit blocks of the main driver and the pre-emphasis as shown in Fig. 11. The numbers of taps are decided by the dada rate and length of cable. In high-speed link, the relationship between current (I) and differential amplitude of signal (ΔV) is

$$\Delta V = I \times Re \qquad (2)$$

where Re is the equivalent resistance.

From Eqn. (2), we know that the amplitude increases linearly with current if the termination resistance is constant. The main driver represents the circuit of the principle driver and the pre-emphasis: tap1and tap2 represent the pre-shaping circuit to emphasize the high frequency components. The function of tap1 is shown in Fig. 12. The circuit of tap1 operates when a data transition is detected and it supplies current I1 to enlarge ΔV. Fig. 13 is tap1 decision circuit.

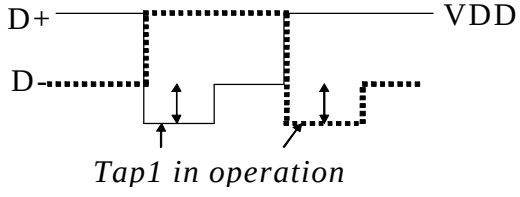


Fig. 12 Signal waveform when Tap1 is operated

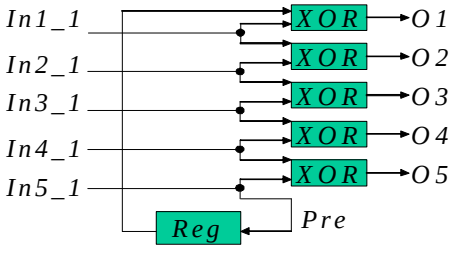


Fig. 13 Tap1 decision circuit

Tap1 is used to enlarge the ΔV in 1, 0, 1,0… transition (~2.5GHZ). However, there must be another tap (tap2) to deal with the attenuation due to 0, 0, 1, 1, 0, 0, 1, 1… (~1.25GHZ) transition. Tap2 is essential in our design to cancel ISI problem. On the other hand, tap3 is required or not is determined by the receiver sensitivity, the area and the loading overhead due to the tap3 circuit. The function of

the tap2 is shown in Fig. 14. and the decision circuit is shown in Fig. 15.

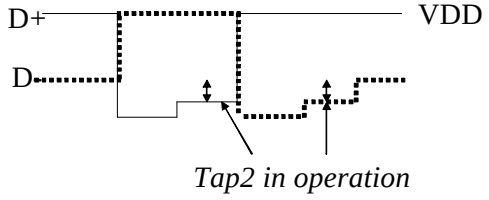


Fig. 14 Tap2 function

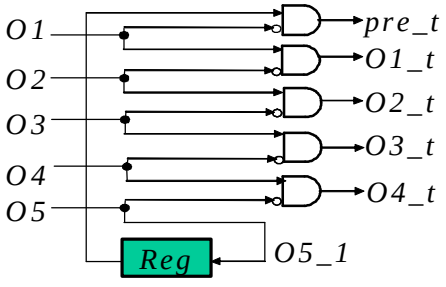


Fig. 15 Tap2 decision circuit

D. Driver

The five parallel data operate at 1Gbps rate, and we need multi-phase clock to transform the parallel data to serial data operating at 5Gbps rate over the cable. A parallel data synchronizer should be used as shown in Fig. 16 to synchronize with the multi-phase clock. as shown in Fig. 17.

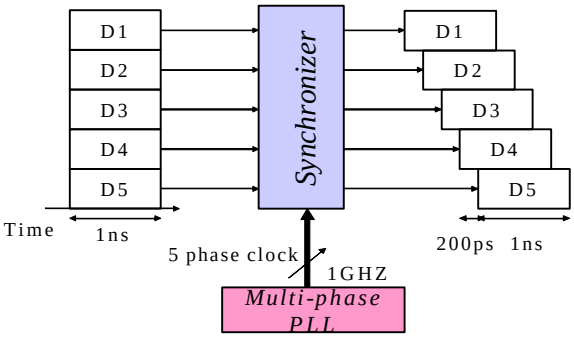


Fig. 16 Pre-skew of parallel data.

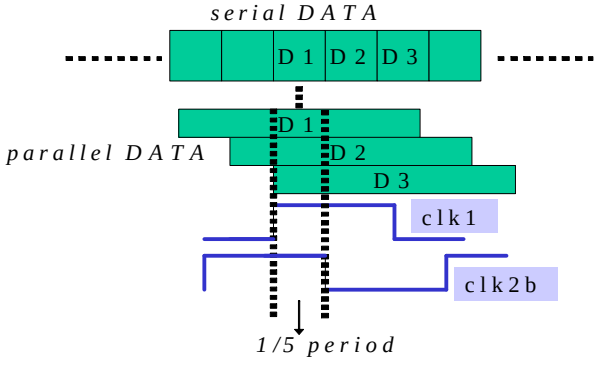
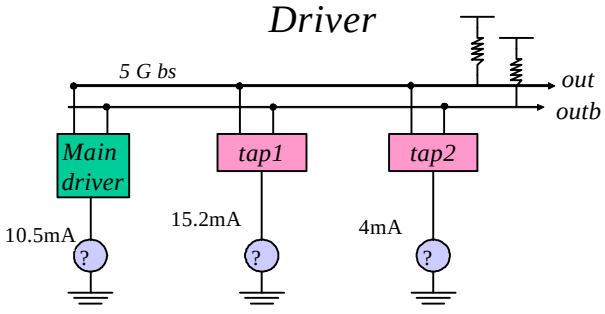


Fig. 17 synchronization of the skewed parallel data with the clocks

The driver includes the main driver, tap1 and tap2, and all have five data path. When the length of the coaxial cable is 10 meter, the driver current is depicted as shown in Fig. 18. In Fig. 19, the tap1 controls seven current sources with each of 3.8mA and the tap2 controls three current sources with each of 2mA. The control signals of Tap1 and Tap2 are "a" and "b". The current of the man driver is 10.5mA that means the voltage of the signaling in the DC situation is 1.55V~1.8v and ΔV is 0.25V. The current of Tap1 is 15.2mA and when four switches are turn on, ΔV is enlarged by 0.38V. The current of Tap2 is 4mA and when two switches are turn on, the ΔV is enlarged by 0.1V.



*DV=I*R=(10.5+3.8*a+2*f)mA*R*

a=0~7, f=0~3

Fig. 18 Driver structure

The total current transmitted to the cable can be

$$I = IS + a \cdot I1 + b \cdot I2 \qquad (3)$$

If the "a" and "b" parameter can be adaptively changed to deal with cable length and data rate, then it can be more robust in different environment. The "a" and "b" parameters can be controlled by the receiver end through an adaptive scheme. The performance of differential input in the receiver and the attenuation of the cable determine the control bits of the decoder. In our design, there are 3 bits (A3 A2 A1) to control tap1 (Fig. 19) and 2 bits to control tap2.

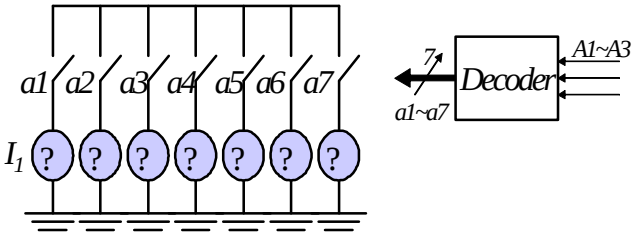


Fig. 19 Current decoder for tap1

The circuit of the main driver is shown as Fig. 20. In Fig. 20, it shows one of the five parallel circuit, and the driver uses multi-phase clock to transform the parallel data to serial data: when clock (N)=1 and clock (N+1)=0, it is turn on.

IV. SIMULATION RESULTS

The input pattern can be periodic data or pseudo random. In general, pseudo random makes the data jitter worse. Fig. 22 shows the eye diagram in the output of the transmitter with PRBS for the pre-simulation. The eye diagrams of the A and B nodes in Fig. 21 are shown in Fig. 22 (a) and Fig. 22 (b) respectively. Fig. 23 shows the eye diagram of the receiver for the pre-simulation. The eyes diagrams of the C and D nodes in Fig. 21 are shown in Fig. 23 (a) and Fig. 23 (b) respectively. The eye diagram without pre-emphasis is shown in Fig. 24. Obviously, this eye is very poor and it's amplitude is smaller than 200 mV.

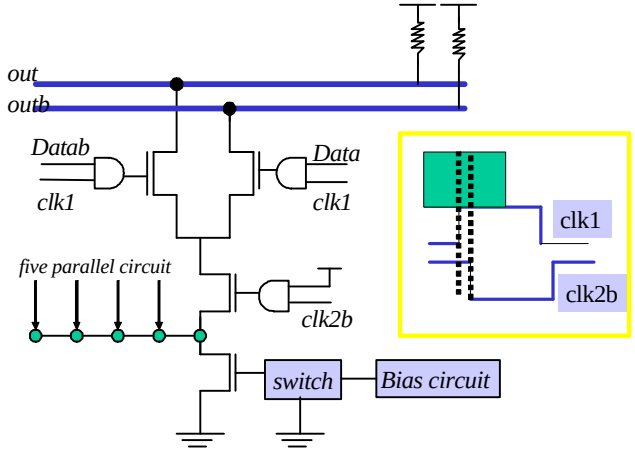


Fig. 20 Main driver circuit

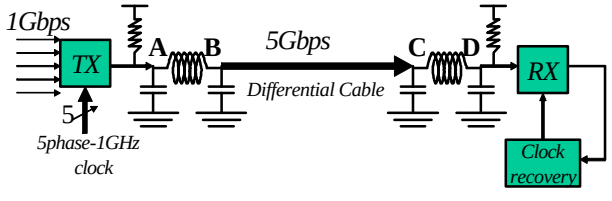
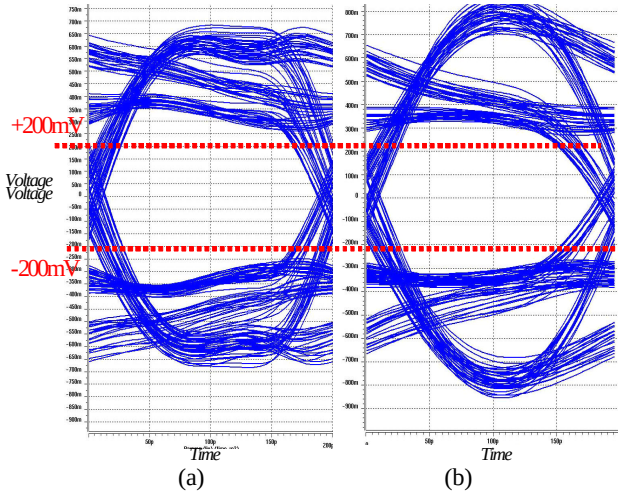


Fig. 21 Transceiver architecture



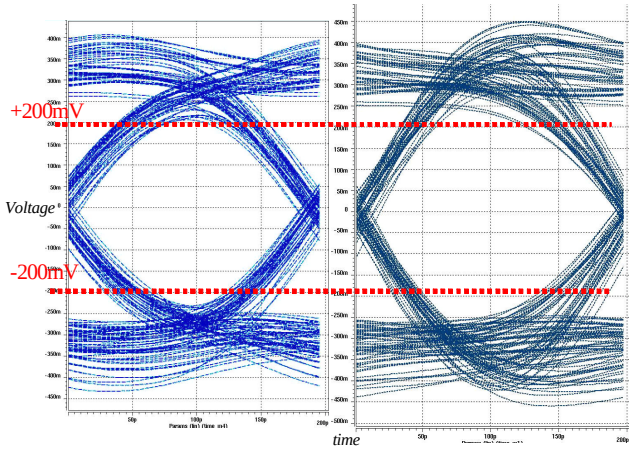
(a) (b)

Fig. 22 The eye diagram in node A and B of the transmitter (pre-simulation)

The overall circuits including PLL, transmitter, and differential-to-single receiver are implemented by using the full custom design flow. Clock buffers are used to insure the equal driving capability of multi-phase clocks. The circuit is implemented by using the process of TSMC1P6M 0.18um. The transmitted signal in node B, node D (Fig. 21) and the differential-to-single receiver output are shown in Fig. 25 (a) (b) (c). The eye diagram of node D (Fig. 21) is shown in Fig. 26. Fig. 27 and Table. 2 show the overall layout and chip summary.

V. CONCLUSIONS

In this paper, we describe the limitation of the transmitter due to package and cable and introduce a better method to design the proposed transceiver. We have described the specification of the cable and we make a cable model with skin effect for the cable to be simulated in Hspice. The multi-phase multiplexer driver can relax the speed requirement. Moreover, the current of Tab1 and Tab2 can be tuned digitally to pre-emphasize the signal to improve the signal quality in the receiving end. By doing so, the length of the coaxial cable can be in the range of 1 meter to 15 meter. We use a five phases clock in the transceiver to achieve the 5Gb/s data rate over the cable with 10m length. All the transmitter and PLL circuit use full custom flow to handle 1GHz clock rate. The chip is implemented in TSMC1P6M 0.18um CMOS technology.



(a) (b)

Fig. 23 The eye diagrams in the node C and D of the receiver (pre-simulation)

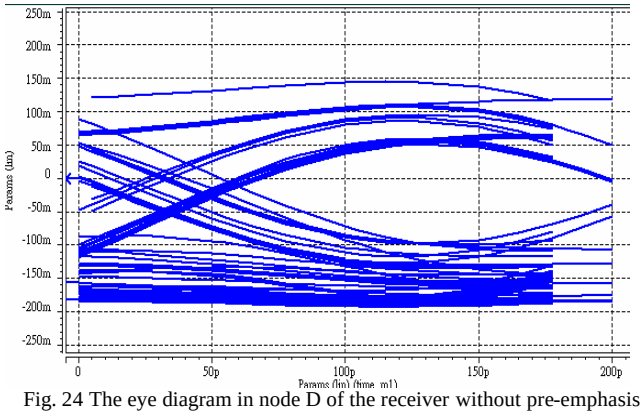
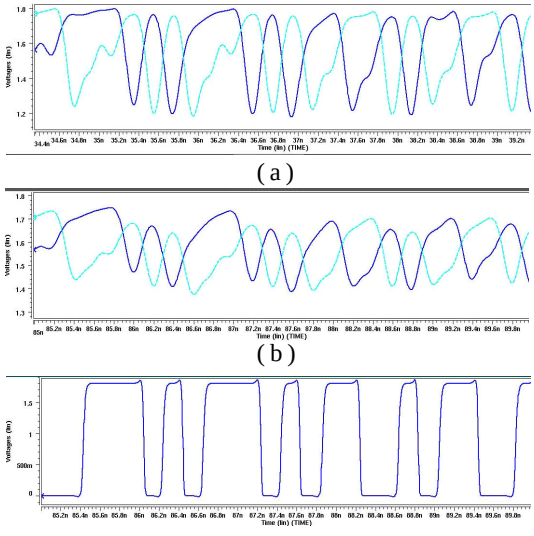


Fig. 24 The eye diagram in node D of the receiver without pre-emphasis



(a)

(b)

(c)

Fig. 25 (a) The transmitted signal, (b) the receiver signal and (c) the differential-to-single receiver output (post-simulation).

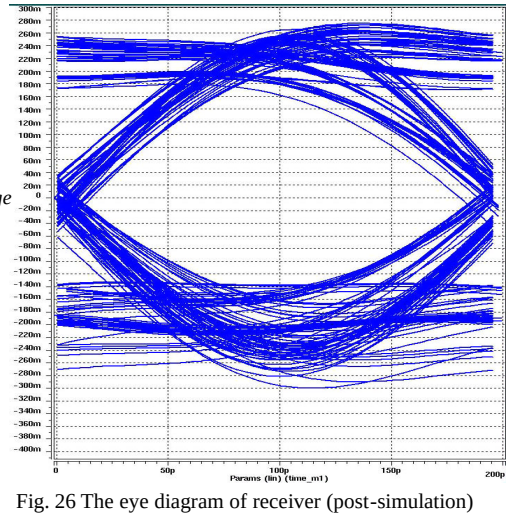


Fig. 26 The eye diagram of receiver (post-simulation)

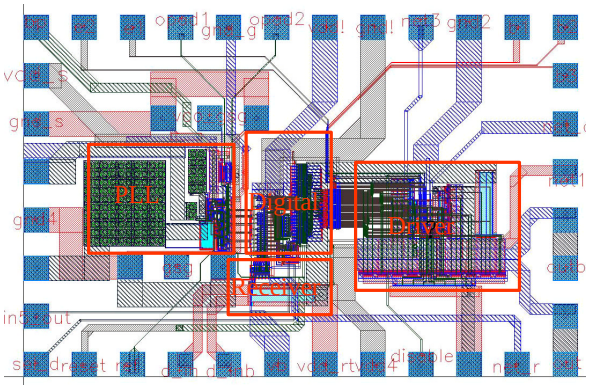


Fig. 27 Overall chip layout

Table. 2 Overall circuit performance summary

Technology	TSMC1P6M 0.18um
Supply	1.8v
Clock rate	1GHz (5 phase)
Data rate	5 Gbps
Total Power (in 5Gps)	150.2 mW
Total Area Decision Logic Driver Receiver	815 x 480 um2 300 x 400 um2 479 x 418 um2 133 x 262 um2
Gate count	830

VI. REFERENCE

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