Experience in Critical Path Selection For Deep Sub-Micron Delay Test and Timing Validation

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Abstract— Critical path selection is an indispensable step for AC delay test and timing validation. Traditionally, this step relies on the construction of a set of worse-case paths based upon discrete timing models. However, the assumption of discrete timing models can be invalidated by timing defects and process variation in the deep sub-micron domain, which are often continuous in nature. As a result, critical paths defined in a traditional timing analysis approach may not be truly critical in reality. In this paper, we propose using a statistical delay evaluation framework for estimating the quality of a path set. Based upon the new framework, we demonstrate how the traditional definition of a critical path set may deviate from the true critical path set in the deep sub-micron domain. To remedy the problem, we discuss improvements to the existing path selection strategies by including new objectives. We then compare statistical approaches with traditional approaches based upon experimental analysis of both defect-free and defect-injected cases.

I. Introduction

Process variations, manufacturing defects, and noise are major factors to affect timing characteristics of deep sub-micron (DSM) designs [1, 2]. Process variations may result in a wide range of possible device parameters, which make timing estimation and validation extremely difficult. Delay faults, caused by interconnect defects and noise sources, are hard to predict in terms of their actual delay sizes, adding more difficulties for ensuring design quality. For these DSM effects, the traditional assumptions of discrete timing and delay models become less applicable [3] [4]. These effects should better be captured and simulated using statistical models and methods [5] [6].

In today's industry, single transition fault model remains one of the most affordable and effective models for AC delay testing. To ensure correct timing behavior, it is also a common practice to include testing of a set of *critical paths*. The definition of a critical path depends on the timing length of the path, which is often calculated using discrete delay models based upon nominal or worst-case timing scenarios.

If critical paths are selected for explicit testing, the definition of a path being critical obviously will affect the effectiveness of the tests. Hence, in this paper, we investigate the change of test effectiveness when the delay assumption is changed from nominal or worst-case models to a statistical model. We demonstrate, through experimental analysis, that with a statistical delay model the traditional method of selecting the *k* longest paths is not adequate. Consequently, adding new criteria for path selection is required, and various new path selection strategies will be analyzed. We describe an efficient path-based test quality evaluation framework that supports both defect-free and defect-injected statistical simulation. While our earlier work [6] explores the theoretical aspects of the problem, this paper focuses on in-depth experimental analysis and report our experience of applying the various path selection strategies.

II. Background/Problem Definition

Historically, the definition of a critical path is based upon the nominal or worst-case timing analysis [7, 8, 9, 10, 11] (i.e., the delay of each cell/interconnect is of discrete timing values based upon either nominal or worst-case delays). In the industry, timing analysis often relies on cell characterization where the earliest, latest, and average signal arrival times are estimated for each pin-to-pin pairs of the cell [12]. With these discrete timing values, the delay of a path can be defined as the accumulated delay on the path. The set of critical paths can then be constructed by selecting either a fixed number of the longest paths, or all paths that fall into a pre-defined timing range. If circuit segment coverage is considered, then the set of critical paths can include, for each signal segment, the timing longest path and ensure a complete topological coverage of the circuit [7, 8].

In DSM delay testing, delay variations resulted from manufacturing process, small defects, and/or signal noise can alter the discrete timing assumptions. Consequently, the sets of critical paths in different chips can be different. It is then questionable that testing a set of critical paths selected based upon a traditional discrete timing model can still be effective in the DSM at-speed test applications.

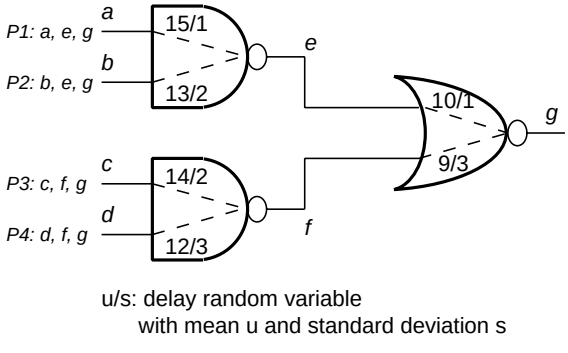


Figure 1: An Illustrative Example

To illustrate the problem, consider the example shown in Figure 1. Suppose cell characterization gives the mean and standard deviation of the delay random variable for each pin-to-pin delay. For example, the pin-to-pin delay $a \rightarrow e$ is a random variable with mean 15 and standard deviation 1. By assuming 3σ bound, the minimal and maximal delays are $15-3\times1$ and $15+3\times1$, respectively. Hence, in a discrete delay model, the pin-to-pin delay can be denoted as $\{12, 15, 18\}$ which represents the earliest, the average, and the latest signal arrival delays. Then, with this discrete delay model, which of the four paths P1, P2, P3, and P4 is the most critical path? Under a worst-case scenario, path P4 is the most critical path because the worst case accumulated delay is $12+3\times3+9+3\times3=39$. The most critical path will be different if 1σ bound is used instead of the 3σ bound. In this case, P3 will be most critical because $14+1\times2+9+1\times2=27$ represents the worst case. On the other hand, if the critical path is defined based

upon the average delays, then P1 will be the most critical one because the sum of the average delay values $15+10=25$ is the largest.

The above example demonstrates the inadequacy of the discrete delay assumptions used to identify the most critical path. If pin-to-pin delays are characterized as random variables, then the delay of each path should be characterized as a joint probability density function (pdf) of all pin-to-pin random variables on the path. For example, the delay of path P1 in the example should be a random variable whose probability distribution is the joint pdf of the two pin-to-pin random variables from "$a \rightarrow e$" (15/1) and $e \rightarrow g$ (10/1). Note that the calculation of the joint pdf depends on whether the two random variables are correlated or independent.

Further notice that if each pin-to-pin delay is a random variable, then the most critical path in each chip instance can be different. This means that if we manufacture 4 chips of the example circuit, the most critical path in these four chip instances can all be different. In other words, any one of the four path can be the most critical path in a particular chip instance. From this perspective, the definition of a critical path is no longer deterministic. Instead, the most critical path should be defined as the path that has the highest probability of being critical when a large number of the chip instances are produced. To support this definition, a statistical timing analysis tool is required.

II-A. Statistical Timing Analysis

In our earlier work, a statistical timing analysis framework was proposed [5]. In that framework, the delays of cells/ interconnects are modeled as correlated random variables with known probability density functions (pdf's). Given cell/interconnect delay functions and a cell-based netlist, the statistical framework can derive the pdf's of signal arrival times for both internal signals and primary outputs.

With the statistical framework in hand, in [13], a critical path was defined based upon its probability of exceeding a given cut-off period. Then, selecting the k most critical paths is to select the k paths whose probabilities are the k largest. These paths are called the *statistical long paths*. Although the statistical nature in this new definition of critical path is expected to improve the quality of the critical path set, our earlier theoretical analysis indicates that for delay testing, considering statistical *path correlation* is crucial [6]. If topologically two long paths overlap substantially, then the return of testing the second path after testing the first path should be reduced, and is not the same as that by testing of the second path alone. Therefore, selecting the k most critical paths would result in an inferior critical path set.

II-B. Path Correlation

Take Figure 2 as an example. Suppose after statistical timing analysis, the arrival time pdf's are characterized in terms of their means and standard deviations at circuit POs. Three paths are shown in the example with these pdf's denoted as 24/3 (path A), 25/3 (path B), and 22/2 (path C). If two paths are to be selected, simply choosing two *statistical longest* paths would include paths A and B into the critical path set. However, suppose path A is first tested, and it is ensured that the output arrival time is within the given clock period *clk*. Then, the timing pdf of path A should be altered. The new pdf of path A should be the conditional probability distribution based upon the new fact that the arrival time of path A is less than *clk*.

After ensuring that path A is less than *clk*, the timing pdf's of each individual segment on path A should be changed accordingly as well. As a result, the timing pdf of path B will be changed. In a sense, testing path A would have implicitly tested a significant part of path B already. In other words, by knowing the fact that path A is less than *clk*, the chance of path B exceeding *clk* now becomes smaller. This is reflected in the reduced return of testing path B afterwards as shown in the figure.

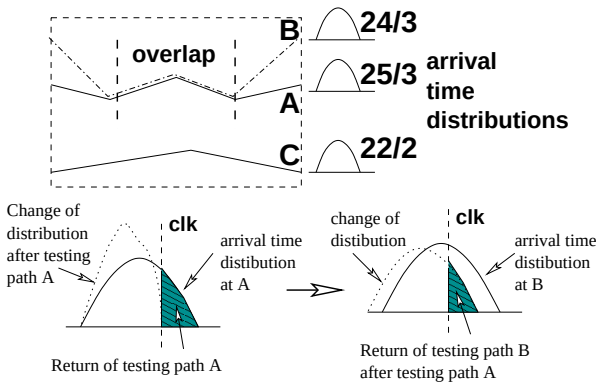


Figure 2: Path Correlation and Diminishing Test Return

Consider path C that is topologically independent of path A. Since statistically path C is slightly "shorter than" path B, testing path C may result in a higher return after path A is tested. Hence, the critical path set should consist of paths A and C instead of paths A and B.

II-C. Path Independence

Path correlation is not the only reason to favor path C as the second critical path. Consider a single-site small-size delay defect occurs randomly in the circuit. If it occurs on path B, it may be likely that by testing path A it has already been covered due to the topological overlap. We note that this is true even though we assume that 100% transition fault testing is applied before testing the critical paths. Transition fault testing usually does not guarantee the capture of small-size delay defect.

II-D. Objectives For Selecting Critical Paths

The above analyses suggests three objectives in critical path selection. These objectives are (1) selecting the statistical long paths rather than the deterministic long paths (as proposed in [13]), (2) avoiding inclusion of paths that are highly correlated, and (3) covering as many independent segments as possible. Note that these objectives may be in conflict of each other.

We emphasize that objective (2) and objective (3) are different because achieving one does not imply the other. We further emphasize that both objectives are different from the transition fault model. In the transition fault model, every site in a circuit is guaranteed to be covered. However, objectives (2) and (3) have to be considered together with the objective of selecting the statistically long paths and the results may or may not ensure 100% topological coverage.

III. Basic Path Selection Strategies

In this section we first discuss path selection strategies based upon the first two objectives, namely selecting the statistical long paths and minimizing path correlations. The extension to consider path independence will be discussed later. Here, we propose to compare three path selection strategies.

Statistical Given a cut-off period T, the statistical framework will calculate the probability of a path whose signal arrival time is greater than T. Then, we will select k paths whose probabilities are the largest [13]. k is a user-defined number. This method does not consider path correlation.

Statistical with Optimization This method improves the above statistical method by taking path correlation into account. In the above method, the delay pdf associated with each signal segment is calculated once, and does not change during the path selection process. This is not true if we consider path correlation. Re-calculating the delay pdf's for all correlated paths

after each time a path is selected can be very time-consuming. In our experiments, we adopt an approximation method based upon Monte Carlo sampling.

In the re-construction of the pdf's, a cut-off period T' is assumed. T' can be shorter than or equal to the clock clk. Suppose path A is selected, and consists of a sequence of signal segments of which delays are characterized by random variables $s_1 \ldots s_n$. The path delay of A can be characterized as the joint pdf $f(s_1 \ldots s_n)$. After the selection of path A, we re-construct all pdf's of $s_1 \ldots s_n$ based upon sampled instances whose delay on path A is $\leq T'$. Now suppose another path B overlaps with A by consisting of $s_i \ldots s_j$. Since the distributions of $s_i \ldots s_j$ have changed, the joint pdf distribution of B can be re-calculated based on these sampled instances accordingly.

The changes of joint pdf's due to path correlation imposed by T' is re-calculated after each path is selected. To speed-up the calculation, we utilize a limited number of Monte Carlo runs to sample the changes of distribution. Moreover, since $T' \leq clk$, a smaller T' would result in faster converging of the process, i.e. after selecting i paths, no paths have a delay greater than T'. In other words, the smaller the T' is given, the smaller the i will be.

In summary, the optimized method consists of two steps: 1) Select the statistically longest path based upon current delay distributions, and 2) Re-construct delay distributions to reflect path correlation resulting from the selection. Note that for selecting the first path, the statistical method above and the optimized method will both pick the same path.

Traditional For comparison purpose, we will also include a traditional method that utilizes the discrete worst-case (the 3σ bound) timing model.

Our conjecture is that the **statistical** method will be better than the **traditional** method, and the **statistical with optimization** method should deliver the best results. Before presenting the experimental results, we discuss the experimental setup below.

IV. Quality Evaluation Based Upon Universal Path Candidate Set

In path delay fault testing, one metric of estimating the test quality is to count the number of paths covered. If all paths are covered, then the circuit performance can be guaranteed. This approach is impractical due to the exponential growth in number of paths. Moreover, this approach is inadequate because it does not differentiate long paths from short paths.

Our approach is first to prune the set of all paths by the false-path-aware statistical timing analysis proposed in [14]. In the process, we remove those paths that are unlikely to cause a delay problem. Paths that cannot be sensitized by any test are also removed [15]. In our methodology, the output of the false-path-aware statistical timing analysis tool is an *universal path candidate set* (U). The size of U is much smaller than the number of all paths and the circuit delay is dominated by the paths in U with almost a 100% probability. Hence, if the entire U is tested, circuit performance can be guaranteed with a very high probability. Essentially, the U set serves as the basis for developing a "golden metric" scheme for quality evaluation.

Figure 3 illustrates the construction of U. The size of U depends on the cutoff period T, and so does the quality of the path coverage metric developed based upon U. To select a reasonable T, one can utilize manufacturing data with characterization of delay defects. In this work we select T based upon results from transition fault testing.

In transition fault testing, many paths have been tested. We first use our false-path-aware statistical timing analysis tool to determine the

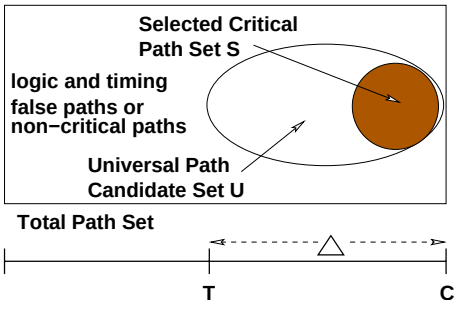


Figure 3: Universal Path Candidate Set

timing lengths of those paths. Then, T essentially denotes the *shortest* timing length among the paths. In this methodology, the higher quality the transition patterns are, the larger the T will be and the smaller the size of U is.

V. Statistical Evaluation of Quality

If we can afford to test all paths in U, then there is no need to develop another test quality metric. In practice, only a subset of U (say S) are selected for testing. Then, the underlying question is how to evaluate the quality of those selected paths S based upon U? In our study, we focus on the quality of selected paths, instead of the quality of tests generated based upon those paths [16]. Hence, our metric involves only static analysis and is pattern-independent.

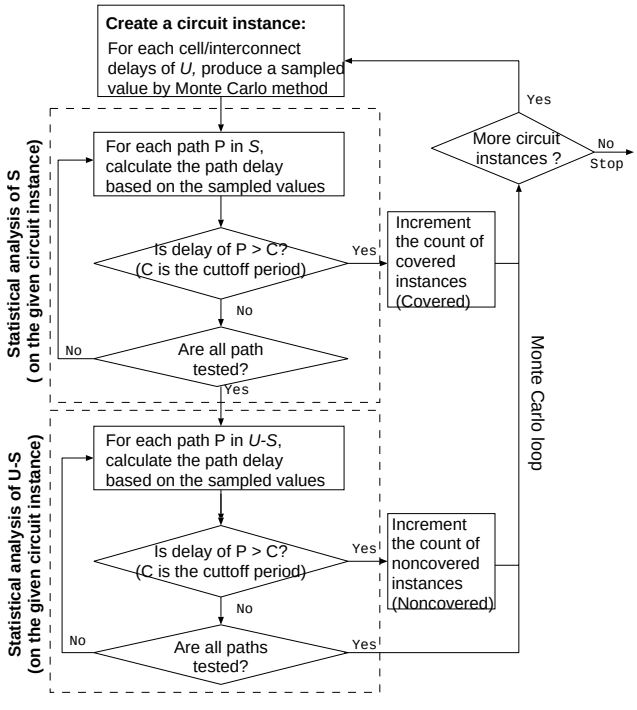


Figure 4: Flow chart for statistical evaluation of S based on U

Figure 4 illustrates the complete procedure of our static quality evaluation scheme. In each Monte Carlo sampling run, first a circuit instance with cell/interconnect delays is generated according to the delay distributions characterized through Monte Carlo SPICE earlier. This instance will then be evaluated by two analysis steps: "statistical analysis of S" and "statistical analysis of U-S". The "statistical analysis of S" is to check if there is any path in S (on the given instance) longer than the testing clock C. If there is, then this instance is said to be faulty and covered by S (*Covered*). The "statistical analysis of U-S" performs a similar analysis on the set of $U - S$ and reports the number of faulty instances not covered by S (*Noncovered*). At the

end, our scheme will calculate the probability of a faulty path captured by S based upon all the instances statistically produced. This *conditional missing probability* is defined as

$$\wp = \frac{Noncovered}{Covered+Noncovered}$$

In other words, the conditional missing probability $\wp$ is the probability that a delay defect (or variation) is not covered by S given the fact that the delay defect (or variation) will affect the circuit performance.

VI. Initial Experiments

Our experimental flow consists of three major phases: timing analysis, path selection, and quality evaluation as described below.

1. Timing Analysis Phase

Our statistical timing analysis framework is cell-based [5]. It requires pre-characterization of cells, i.e., building libraries of pin-pin cell delays and output transition times (as random variables). In our experiments, we utilizes a Monte-Carlo-based SPICE (ELDO) [17] to extract the statistical delays of cells for a 0.25μm, 2.5V CMOS technology. The input transition time and output loading of the cells are used as indices for building/accessing these libraries. Each interconnect delay is also modeled as a random variable and is pre-characterized once the RCs are extracted. For traditional worst-case analysis, we use the same framework by fixing the cell delays to be the 3σ values of the random variables in the delay libraries.

2. Path Selection Phase

The first step in path selection is to produce the universal path candidate set U (Section IV) and then, use each of the three path selection methods to derive a reduced subset S (Section III).

3. Evaluation Phase

This phase will follow the statistical quality evaluation method described in Section V.

VI-A. Basic Results

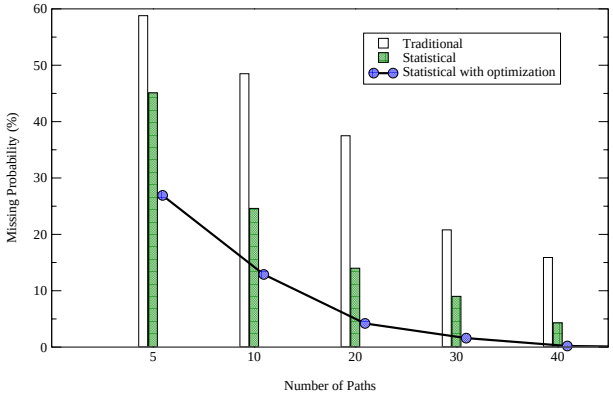


Figure 5: Results of Defect Free (s5378)

We first focus on the results from circuit s5378 for detailed discussion. In our experiments, three cases were studied:

Defect Free This represents the case of small delay variation without explicit defect occurrence. The intention is to approximate process variation and to compare the effectiveness of the three methods with respect to timing validation.

1-Unit Defect Injected We randomly inject a delay defect of size 1 unit (1 gate delay) onto the circuit. This is to compare the test effectiveness of the three methods with respect to their ability to capture a small-size delay defect.

3-Unit Defect Injected Similarly, in this case we randomly inject a delay defect. Yet in this case we try to compare the three methods with respect to their ability to capture a relatively larger-size delay defect.

In all cases, the conditional miss probabilities $\wp$ are shown as percentages. Figure 5, Figure 6, and Figure 7 present the results.

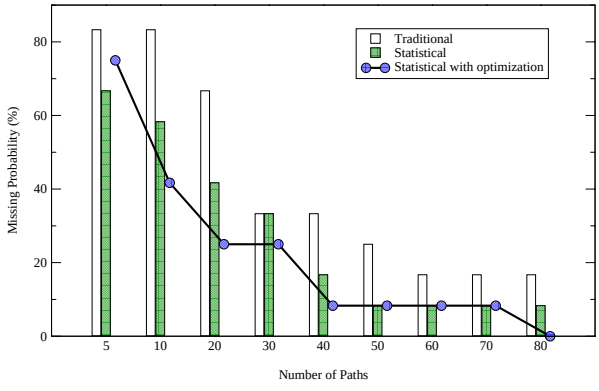


Figure 6: Results of 1-unit Defect Injected

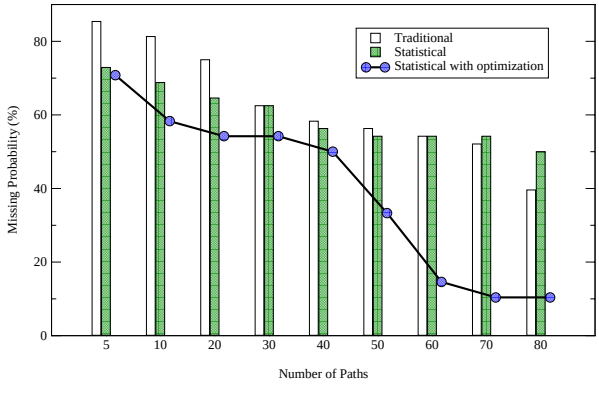


Figure 7: Results of 3-unit Defect Injected

In the defect-free case, Figure 5 clearly demonstrates that the traditional method is ineffective. The difference between the **statistical** method and the **statistical with optimization** method is noticeable. We note that after the **statistical with optimization** method selects the 40th path, the miss probability becomes zero. From the results in Figures 6 and 7, we make three further observations.

1. Selecting long paths as critical paths favors the detection of small-size delay defects (results in Figure 6 in general are better than the results in Figure 7.
2. In the case of small-size delay defect, the two statistical methods consistently out-performs the traditional method. In the case of large-size delay defect, the results are mixed depending on the number of paths included in S. This is understandable because all three methods intend to capture small-size delay defects, not large-size delay defects.
3. The **statistical with optimization** method consistently outperforms the other two. Intuitively, by considering path correlation, this method tends to produce a set of paths that are more independence.

VII. Considering Path Independence

Our next goal is to include the objective of *path independence* into the path selection process. We also propose to compare three methods in the experiments.

Traditional with Segment Coverage To achieve path independence, we associate a weight w_i with each signal segment s_i. When s_i is covered by a selected path, w_i will be slightly decreased by a ratio. Then, the method will select a path with the highest total weight covered. If more than one paths have the same total weight, it will select the timing longest one where timing is defined using the worst-case delay model. Note that in this method we intentionally make path independence outweight the the other two objectives in order to demonstrate its effect in the experiments. We also note that with a sufficient number of selected paths, this method will ensure the coverage of every segment (site) in U.

Statistical with Segment Coverage This method is similar to the first one except that it is based upon the statistical timing model.

Statistical with Optimization By considering path correlation, the **statistical with optimization** method may "run out of" path after selecting i paths where $i < \mid U \mid$ (as explained before). In other words, after i paths are selected and path correlation is applied to re-construct the pdf's of the remaining paths, no path in U exceeds the cut-off period T. When this happens, the path selection objective will be switched to path independence and continue the selection of paths. In other words, after selecting the ith paths, we make it behave the same as the **statistical with segment coverage** method described above.

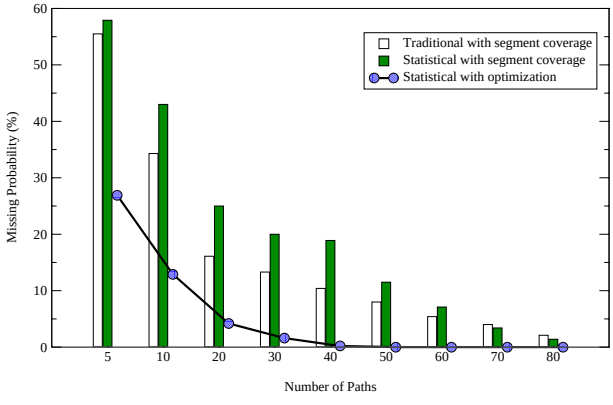


Figure 8: Results of Defect Free (s5378)

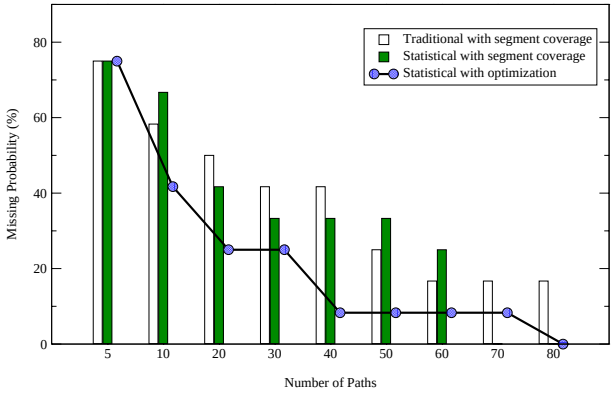


Figure 9: Results of 1-unit Defect Injected (s5378)

Figures 8 to 10 show similar comparison results for the three methods just described. Under the defect free condition, the **statistical with optimization** method still achieves far better results than the other two. If we compare Figure 8 with Figure 5 at path set size 40, two interesting observations can be made:

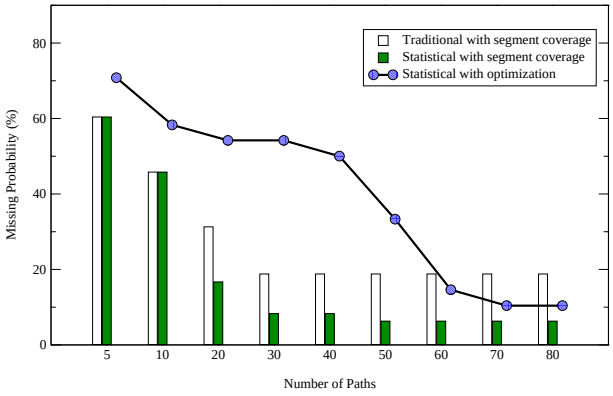
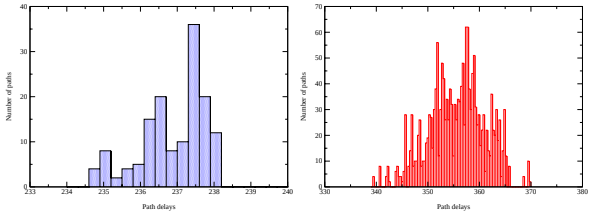


Figure 10: Result of 3-unit Defect Injected (s5378)

1. When comparing the statistical path selection strategies in the two figures, including the objective of path independence degrades the results.
2. However, when comparing the two traditional approaches, including path independence as the first selection objective actually improves the results. In other words, selecting the long paths given by the discrete worst-case timing model is less effective than simply achieving a high segment coverage.

For the two defect-injected cases, the **statistical with optimization** method is not always the best. It performs quite well in the case of the 1-unit delay defect, and is competitive only when the number of included paths is large for 3-unit delay defects. Again, this is not a surprise because the method is optimized for small-size delay defects.

VII-A. Design Characteristics



(a) Path Profile (s5378) (b) Path Profile (s15850)

Figure 11: The profile of path delays.

To better understand the results from s5378, Figure 11(a) demonstrates the path profile of the path universe U. This profile indicates that the performance of the circuit is not dominated by a few paths (more equally distributed). In contrast, Figure 11(b) shows the path profile from s15850 where its performance is dominated by only a few long paths (the two spikes on the right hand tail).

Figures 12 and 13 show results for circuit s15850. Notice that when the circuit performance tends to be dominated by only a few extremely long paths, the results also tend to polarize. First, for defect-free (and small-size defect) cases, focusing on path independence tends to get worse. For large-size delay defects, selecting the long paths can be very ineffective. These examples demonstrate that the objective of selecting the long paths and the objective of achieving path independence can be opposite to each other.

Due to the relatively small number of the long paths shown in the profile of s15850, focusing on selecting the long paths restricts the selection within a small subset of all paths. As a result, the topological coverage of path segments will be limited. On the other hand, focusing on path independence significantly reduces the chance of selecting the long paths and hence, degrade the quality in the cases of

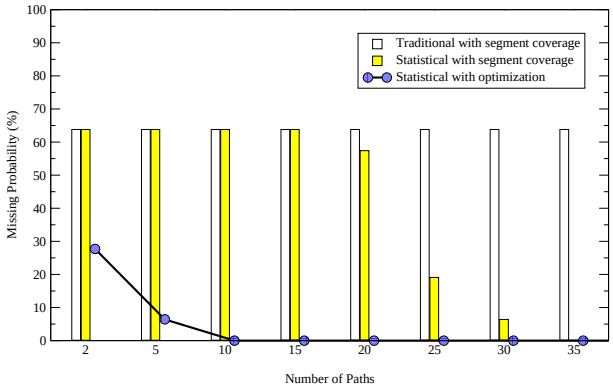


Figure 12: Results of Defect Free (s15850)

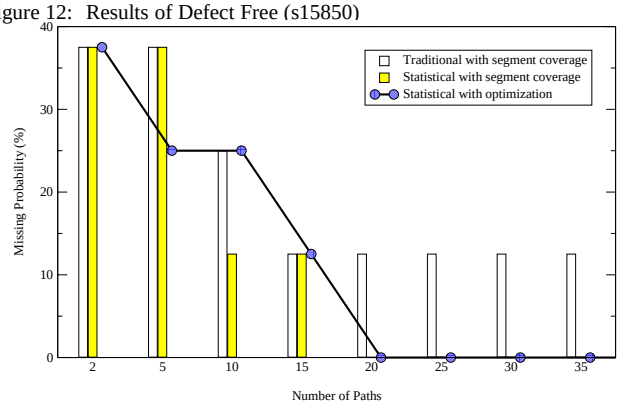


Figure 13: Results of 3-unit Defect Injected (s15850)

small-size defect and defect-free variation. In both figures, the **statistical with optimization** method is able to reach zero miss probability at a reasonable pace.

VIII. Results From Other Circuits

circuit	# of paths in U	missing prob. (%) (traditional)	missing prob. (%) (statistical)	Mem (bytes)	CPU (s)
s5378	1238	48.5%	12.9%	3M	0.29
s9234	842	0.0%	0.0%	4M	1.37
s15850	1728	4.3%	0.0%	6M	5.23
s35932	4702	26.6%	0.0%	20M	11.7
s38417	3972	80.9%	47.4%	24M	6.95
s38584	136	0.0%	0.0%	12M	0.26

TABLE I: Comparison Results on Large ISCAS89 Benchmarks with 10 Paths Selected

Table I presents comparison results between the traditional method (without considering path independence) and the statistical method (with path correlation) for several benchmark circuits using the defect-free simulation. Results from this table further confirm the inadequacy of using a traditional discrete timing model for critical path selection. Notice that depending on the circuit characteristics, in general the size of the universal path set U is quite small. This allows our statistical evaluation framework to estimate path set quality much more efficiently (as shown in the run time and memory usage columns in the table).

IX. Conclusion

In this paper, we studied various critical path selection strategies based upon defect-free and defect-injected simulation. We proposed a flexible and efficient path quality evaluation methodology based upon the false-path-aware statistical timing analysis framework developed before [14]. In our study, we considered three path selection objectives: including statistically long paths, considering path correlation, and path independence. These objectives may be opposite to each other during the path selection process.

Our analysis concludes the inadequacy of using a discrete timing model in traditional path selection approaches. The importance of using a more realistic, statistical timing model and the importance of considering path correlation are demonstrated through the extensive experiments. The newly proposed **statistical with optimization** strategy consistently out-performs all other methods in our study. Therefore, for deep sub-micron delay test and timing validation, we suggest that a statistical timing analysis tool should be used, and path correlation should be included as a key objective in critical path selection.

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