Cross Talk Driven Placement

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Abstract

Due to the fast shrinking of process geometries, signal integrity issues are becoming increasingly critical to the performance and reliability of electronic systems. Traditional post-layout based fixing methodologies quickly break down when hundreds of thousands of nets need to be tailored for signal integrity concerns. In order to achieve signal integrity closure, cross talk, electro-migration, IR drop and other effects must be addressed earlier in the design cycle. In this paper, a new placement algorithm considering cross talk minimization is presented. First, a probabilistic technique is presented to estimate the coupling capacitance during coarse placement. Based on this technique, an effective placement flow is introduced to remove the highly coupled spots via placement density control. By addressing cross talk at placement level with this algorithm, the value and count of the highest post route peak noise were successfully reduced in a set of industrial benchmarks. Furthermore, due to reduced coupling capacitance, the design speed is 8% faster on average in comparison with traditional timing-driven, congestion-aware placement flow.

I. Introduction and Background

Advances in the semiconductor fabrication technology, such as the scaling down of minimum feature size, the increasing in number of metal layers, the usage of stacked vias, etc., have contributed to the fast and steady enhancement of the performance and density of the Very Large Scale Integrated (VLSI) circuits for more than two decades. However, when the VLSI designs evolve to sub-0.18 micron processes, a number of electrical effects such as cross talk, electro-migration, wire self-heating and IR drop, are becoming critical to the performance and reliability of electronic systems. This set of new challenges is referred as signal integrity in general. Among all these problems, capacitive coupling induced cross talk is the issue that has been seen by an increasing number of backend vendors. Cross talk typically happens between two adjacent wires when their cross-coupling capacitance is sufficiently large to influence each other's electrical characteristic. Two major impacts of cross talk are: (1) cross talk induced delays, which change the signal propagation time, and thus may lead to setup or hold time failures; (2) cross talk glitches, which may cause voltage spikes on wire, resulting in false logic behavior.

Many works have been done to address cross talk. The previous works can be categorized into two groups: analysis and optimization. Numerous models have been proposed to extract the RCL network of nets [3]. After the high-coupling nets are identified, optimization techniques are performed to reduce the cross talk effects [1][4]. However, most of the existing optimization techniques work with a post-layout circuit, thus greatly limiting the effectiveness of these approaches. For example, if the initial placement introduces a lot of potential coupling, the router may not be able to fix all of them without violating design constraints. In such a case, a cross talk aware placement tool is required to prevent coupling between signal nets from happening at a higher level. In this paper, a cross talk driven placement algorithm is presented.

The rest of the paper is organized as the following. The coupling capacitance estimation technique is presented in section II. The placement algorithm is discussed in section III. Experimental results and conclusions are given in section IV and V, respectively.

II. Coupling Capacitance Estimation

II.1. Overview

Coupling capacitance estimation during coarse placement includes two separate tasks: unit coupling capacitance estimation and topology estimation. Unit coupling capacitance estimation is to estimate the capacitance values per unit length for horizontal and vertical directions. The goal of topology estimation is to find a good approximate for the post routes during the pre route phase. The techniques include net bounding box, Steiner routing, global routing, etc.

We decompose coupling capacitance into three components as shown in Figure 1:

- *Area capacitance: the capacitance between the top/bottom side of a net and its upper/lower layer*
- *Fringe capacitance: the capacitance between the vertical side of a net and its upper/lower layer*
- *Lateral capacitance: the capacitance between the vertical side of a net and its neighboring nets on the same layer*

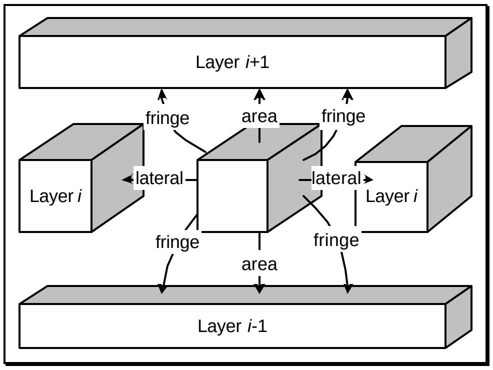


Figure 1 Components of coupling capacitance

It can be easily seen that neighborhood congestion significantly impacts the coupling capacitance. Different designs with different congestion characteristics cannot share a same unit coupling capacitance value even if they use the same manufacturing process. Even for the same design, the congestion tends to differ drastically from region to region. Therefore, any method that uses a single unit coupling capacitance value for the entire design will lead to great inaccuracy. In this section, we introduce a novel technique to estimate the coupling capacitance based on congestion analysis for any given region of the design.

II.2. Congestion Analysis

There are many papers addressing the congestion problem [6][10]. We use the probabilistic technique described in [6] to perform congestion analysis. We define a *congestion map* by dividing the core area of a design with a homogeneous rectangular mesh (c.f. Figure 2), and then analyze the congestion for every grid in the mesh. We first compute the *capacity* of a grid, which is defined as the number of available routing tracks within the grid, and then compute the *usage* of a grid, which is defined as the number of used routing tracks within the grid. The ratio between the usage and the capacity is the congestion value for this grid.

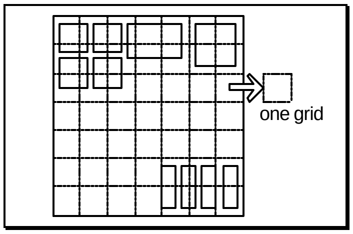


Figure 2. Congestion analysis

II.3. Unit Coupling Capacitance

II.3.1. Worst case coupling values

The worst case coupling values for the unit area/fringe/lateral capacitances can be computed from the manufacturing process parameters, such as the metal thickness, oxide thickness and oxide permittivity. Most industrial extraction tools have a technology file that defines these parameters. The exact details of this computation are well studied in literatures [8], and are omitted in this paper. For each individual region, we compute the unit coupling capacitance by properly scaling down these worst-case values with respect to congestion values for the particular region.

The capacitive coupling effects between two metal layers are determined by two factors: the *coupling factor* and the *visibility factor*. The coupling factor determines the tightness of the coupling between the layers, and the visibility factor determines the shielding effects of other layers.

II.3.2. Coupling factor

The coupling factor k_i gives the percentage of a metal that are coupled to the metals on layer *i*. Assume there is a metal on layer *j*, and layer *i* and *j* are with perpendicular routing directions (c.f. Figure 3). Let us denote the routing width and pitch of layer *i* as $width_i$ and $pitch_i$. If the particular region on layer *i* is 100% congested, all routing tracks will be occupied. Therefore, the percentage of coupled length for this piece of metal to layer *i* is $width_i/pitch_i$. When a layer is not 100% occupied, we assume the routes will be distributed within the region with the same probability. For example, assuming layer *i* is 50% congested, based on this even distribution assumption, every other track will be occupied. Therefore, the percentage of coupled length for the metal on layer *i* becomes $\frac{width_i}{2\times pitch_i}$. It is not difficult to conclude that for any non-zero congestion values, the effective pitch becomes *pitch*/*congestion*. Therefore, the coupling factor k_i for layer *i* is:

$$k_i = congestion \times \frac{width_i}{pitch_i} \quad (1)$$

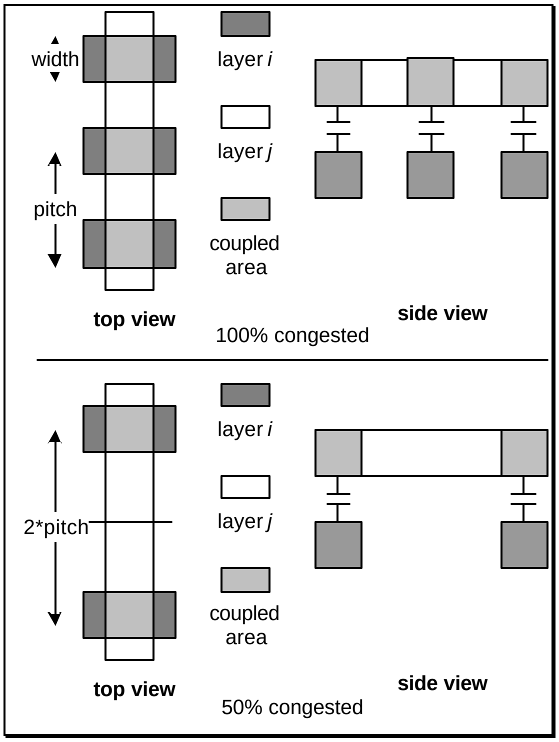


Figure 3. Coupling factor for perpendicular routing direction

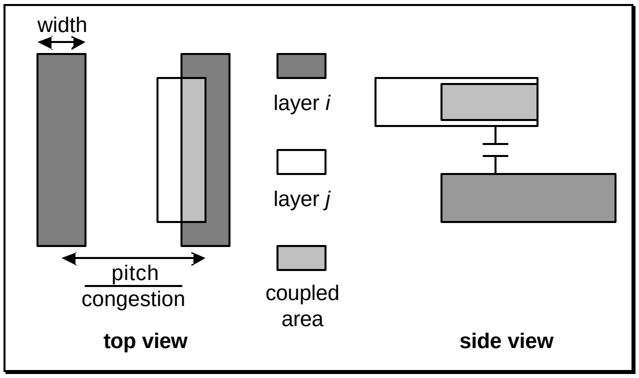


Figure 4. Coupling factor for the same routing direction

If layer *i* and *j* have the same routing directions (as shown in Figure 4), the actual coupled width depends on the location of the metal on layer *j*. Assuming this metal can be placed anywhere with the same probability, the expected coupled width between this metal and layer *i* can also be computed using (1).

II.3.3. Visibility factor

For two adjacent layers, the visibility factor v_{ij} is always 1. To compute the capacitive effects between non-adjacent layers, we must consider the shielding effects of the layers in between. These layers act as filters where electrical flux is only allowed between the gaps of metals. For a layer whose coupling factor is k_i, the percentage of gaps is 1-k_i. Therefore, We derive the following equation to compute the visibility factor v_{ij} for layers *i* and *j*:

$$v_{ij} = \begin{cases} 1 & \text{if } j = i+1 \text{ or } j = i\text{-}1 \\ v_{i(j\pm1)} \times \left(1\text{-}k_{j\pm1}\right) & \text{else} \end{cases} \qquad (2)$$

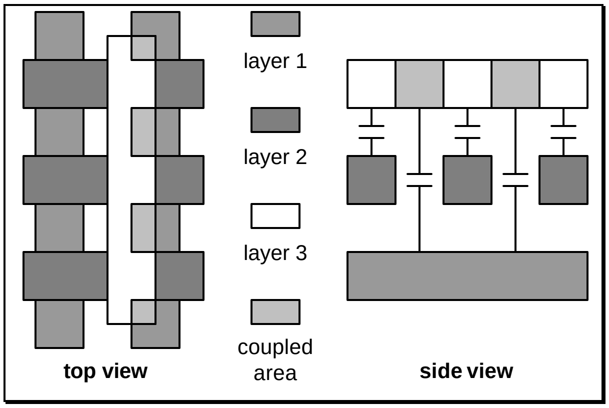


Figure 5. Visibility factor

In Figure 5, we show an example on how to compute the visibility factor between metal layer 1 and metal layer 3. Let us assume 100% congestion and *width*/*pitch* = 0.5 for all layers. From (2), we know that $v_{13} = v_{12} \times \left(1 - k_2\right)$. From (1), we can compute k_1=k_2=0.5. Hence, v_{13}=0.5. This means because of the shielding effect of layer 2, the coupling between layer 1 and 3 has been reduced by 50%. It can be easily seen from the side view of Figure 5, where only half of the coupling capacitance from layer 1 reaches layer 3. In addition, because k_1=0.5, the effective coupling between layer 1 and 3 is now 0.25.

II.3.4. Area capacitance

The area capacitance between layers *i* and *j* can be computed as:

$$area\_cap_{ij} = k_i \times v_{ij} \times worst\_case\_area\_cap_{ij} \qquad (3)$$

and the total area capacitance of layer *i* is:

$$area\_cap_i = \sum_{\forall j \neq i} area\_cap_{ij} \qquad (4)$$

II.3.5. Fringe capacitance

Similarly, the fringe capacitance between layers *i* and *j* is:

$$fringe\_cap_{ij} = k_i \times v_{ij} \times worst\_case\_fringe\_cap_{ij} \qquad (5)$$

and the total fringe capacitance of layer *i* is:

$$fringe\_cap_i = \sum_{\forall j \neq i} fringe\_cap_{ij} \qquad (6)$$

II.3.6. Lateral capacitance

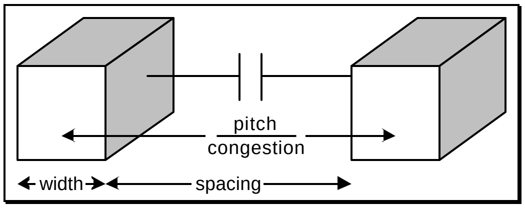


Figure 6. Lateral factor

Lateral capacitance depends on the spacing between the adjacent wires on the same layer. We define the lateral factor as the ratio between the expected wire spacing and the minimum wire spacing. The minimum wire spacing is *pitch* - *width*. For any non-zero congestion value, the expected wire spacing can be computed as $spacing = \frac{pitch}{congestion} - width$. Therefore, the lateral factor d_i for layer *i* can be computed as:

$$d_i = \frac{pitch_i - width_i}{\frac{pitch_i}{congestion_i} - width_i} \qquad (7)$$

As a result, the lateral capacitance can be computed as:

$$lateral\_cap_i = d_i \times worst\_case\_lateral\_cap_i \qquad (8)$$

II.3.7. Total Coupling Capacitance

The unit coupling capacitance for the vertical direction is the weighted average of unit capacitances of all vertical routing layers. Similarly, the unit coupling capacitance for the horizontal direction is the weighted average of unit capacitances of all horizontal routing layers:

$$coupling\_cap_h = \frac{\sum_{\forall horizontallayers} w_i \times coupling\_cap_i}{\sum w_i} \qquad (9)$$

$$coupling\_cap_v = \frac{\sum_{\forall verticallayers} w_i \times coupling\_cap_i}{\sum w_i} \qquad (10)$$

The weight for each layer is to model the probability that the layer will be used for routing purpose. These values can be obtained from a trial route, or derived empirically.

II.4. Coupling Capacitance for a Net

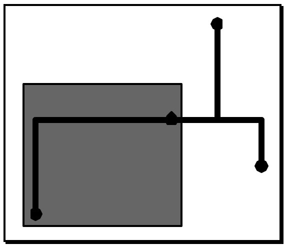


Figure 7. Quick Global Routing

We use a quick global router to perform the routing topology estimation. It differs from conventional global router by skipping the layer assignment phase. For each wire segment in the routing tree, we compute the congestion for the region where this segment passes through, and use (9) and (10) to compute the horizontal and vertical unit coupling capacitance. The total coupling capacitance of this wire segment is then computed as:

$$\begin{aligned} ccap_{seg} = {} & horizontal\_length \times coupling\_cap_h \\ & + vertical\_length \times coupling\_cap_v \end{aligned} \tag{11}$$

III. Coupling Capacitance Optimization

III.1. Overview

Based on the coupling capacitance estimation, we propose a placement technique to reduce the highly coupled regions. Our approach uses a recursive partitioning method similar to that used in [5] with build-in coupling capacitance cost, modeled by a coupling capacitance map.

III.2. Coupling Capacitance Map

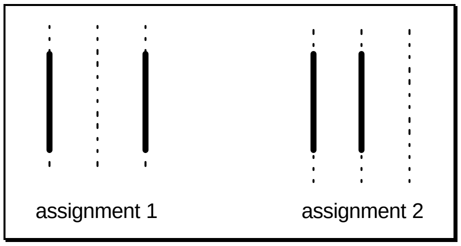


Figure 8. Track assignment

The coupling capacitance of a net depends on the net topology and the congestion. However, both of them are not precisely known at the placement stage. Only after routing, the track and layer are assigned to each net segment, and the coupling capacitance can then be accurately extracted. Figure 8 shows an example that a small difference in track assignment could lead to a large difference in lateral capacitance. In this example, two nets need to be assigned to three tracks. In assignment one, the second net is routed two tracks away from the first net, and in assignment two, these two nets are routed next to each other. Therefore, the lateral capacitance of assignment two is twice as large as that in assignment one. On the other hand, because of the probabilistic nature of coupling capacitance estimation techniques, we will assume that these two nets are evenly distributed over three tracks, making them one and a half track away. This is obviously not legal, nor correlates to any one of these two assignments. However, even though the value of coupling capacitance for a particular net may not be absolutely correct, according to the statistical theory [7], the estimation of a set of sufficiently large number of nets can be highly accurate. Therefore, during placement, we target the sub-regions for coupling capacitance optimization, not individual nets.

We re-use the mesh in *congestion map* defined in section II.2 to model coupling capacitance. The coupling capacitance of $grid_{i,j}$ is computed as the summation of coupling capacitances of all net segments that are within this grid:

$$ccap_{i,j} = \sum_{\forall seg_k \in grid_{i,j}} ccap_{seg_k} \tag{12}$$

where $ccap_{segk}$ is calculated by (11). In Figure 9, the coupling capacitances of the gray grid equals to the coupling between the two horizontal segments of net_a and net_b that are within this grid. We define the mesh as *coupling capacitance map*.

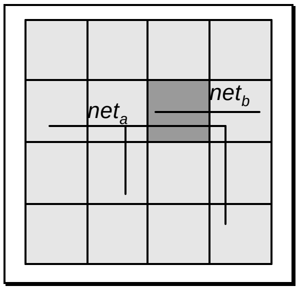


Figure 9. Coupling capacitance map

In section II.3, we show congestion plays an important role in the coupling capacitance estimation. However, coupling capacitance map is not the same as congestion map. Layer variation, wire segment length, routing obstructions and keepouts, pre-routes and P/G nets, all contribute differently to congestion and coupling capacitance estimation. Therefore, congestion optimization usually does not produce a satisfactory result for coupling capacitance reduction.

III.3. Placement Density Control

Based on the coupling capacitance map, we can predict highly coupled regions of any given placement. We will then try to reduce the cross talks by assigning each cell to an appropriate location. To remove the highly coupled spots, fewer cells should be placed in such areas. In this way, the routing demand will be reduced, and routes can be placed farther away from each other. This technique efficiently reserves routing resources used by post route optimizer. We use a placement density map to achieve this goal.

One of the objectives of the placement algorithm is to spread cells evenly in the core area, achieving even density. Without this objective, it is likely that placer will put all cells in the center of the core area and results in zero total wire length. During cross talk driven placement algorithm, the coupling capacitance in a grid is optimized by controlling the target placement density. We add a pseudo cell whose size is proportional to the ratio of the coupling capacitance of the grid versus the average coupling capacitance. Consequently, the number of vacant placement sites in the grid is reduced by the added pseudo cell, resulting in the reduction of final placement density.

The average coupling capacitance is computed as:

$$ccap_{avg} = \frac{\sum_{M \ge i \ge 0} \sum_{N \ge j \ge 0} ccap_{i,j}}{M \cdot N} \tag{13}$$

where M and N are the dimensions of the coupling capacitance map.

The size of the pseudo cell for $grid_{ij}$ is computed as:

$$size_{i,j} = \begin{cases} 0 & ccap_{i,j} < ccap_{avg} \\ \dfrac{ccap_{i,j}}{ccap_{avg}} & otherwise \end{cases} \tag{14}$$

The larger the estimated coupling capacitance, the larger the pseudo cell is. Because of the added pseudo cells, the placer will not place as many cells in the coupled regions as other regions. The real density excluding the pseudo cells looks similar to the inverse of the coupling capacitance map. For example, the corresponding placement density map of the example in Figure 9 is shown in Figure 10, where in Figure 9, the lighter color means less coupling capacitance, and in Figure 10, the lighter color means less number of cells.

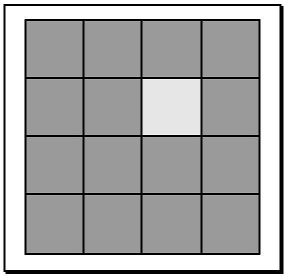


Figure 10. Placement density

III.4. Algorithm Flow

Our placement algorithm works in an interleaved, partition based flow similar to that used in [2] [5]. The flow chart is shown in Figure 11. The objective of the placement is to minimize the total timing-weighted wire length and achieve even distribution of cells with respect to the added pseudo cells.

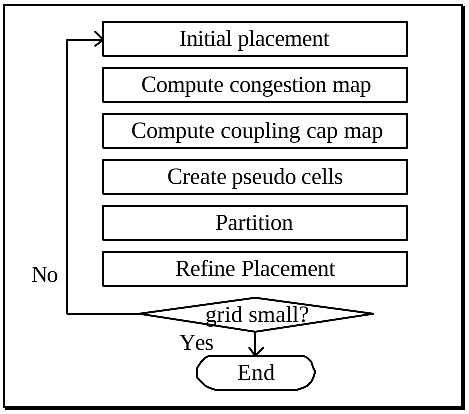


Figure 11. Algorithm flow

At the beginning, an initial placement is performed. During that process, the whole chip is regarded as a big grid. Only the center of mass constraint in term of the whole chip is applied. After the initial placement, we compute the congestion map and coupling capacitance map. We will then add the pseudo cells to the grids which see high coupling. Next, we recursively partition the placement region r and the module set M_r into smaller regions similar to [5]. The major difference is that now the area F_r of r is defined by:

$$F_r = \sum_{m \in \mathrm{M}_r} F_m + F_r^{'} \qquad (15)$$

where F_m is the area of the cell/sub-module m and F'_r is the area of the pseudo cell inserted in r. During the refine placement phase, the cell placement will be further refined within the regions. Moreover, during this refinement phase, in addition to the center of mass constraints, the placement density constraint sets upper limit on the number of available placement sites in each grid. These two constrains can (1) force the cells to be placed evenly on the whole core area, (2) smooth the highly coupled grid by reducing the space utilization.

This analysis, partition and placement loop is repeated in iterations until the number of cell in a grid is small enough for detailed placement. With the size of grid increasingly smaller, the degree of placement and coupling capacitance estimation are progressively finer. During each iteration the size of each pseudo cell is updated on the latest analysis. Consequently, the previous inaccuracy can be corrected.

IV. Experimental Results

IV.1. Experiment Flow

To prove the effectiveness of this approach, we set up the following flow as baseline to do experiment on a set of industrial benchmarks. Both the reference run and our proposed algorithm go through this flow. The only variation is that in the reference run, the traditional timing driven, congestion aware placement is used in the coarse placement stage; while with our algorithm, the presented cross talk driven placement is invoked. We use Physical Compiler® to perform routing, extraction and noise/delay computation.

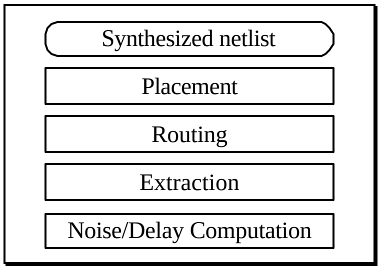
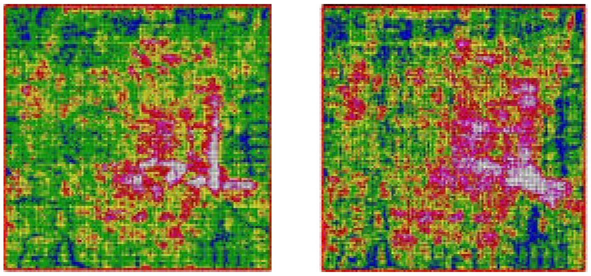


Figure 12. Experiment flow

IV.2. Correlation of Coupling Capacitance



Estimated Actual

Figure 13. Correlation of coupling capacitance

The precision of the coupling capacitance estimation determines the performance of the algorithm. The correlation between our estimation and the extraction value after detailed routing is compared in Figure 13. The left figure is the coupling capacitance map based on the estimation using the techniques described in section II. This is done by running the estimation with the placed netlist. The right figure is the coupling capacitance map based on post-routing RC extraction. This is done by detail route the same placed netlist and then extract the design using Physical Compiler's 2.5D extractor. The color code from the lowest coupled to the highest coupled is blue – green – yellow – red – white. The pictures showed our estimation is able to predict the highly coupled areas during the placement. The proposed approach is reliable to predict the potential highly coupled area.

IV.3. Peak Noise Reduction

In this section, we compare the peak noise values after extraction for a set of industrial benchmarks. The size for these benchmarks ranges from 10K to 85K cells, and all of them are implemented on a 0.15μ technology library. The characteristics of these benchmarks are given in Table 1. The reduction of peak noise for using our algorithm is presented in Table 3. "Ref" stands for the reference flow, whereas SI means our proposed flow. The numbers are the percentage of nets that has the corresponding peak noise value. It demonstrates that our flow can significantly reduce the value and count of the highest peak noise.

	Design 1	Design 2	Design 3	Design 4
cells	11226	21649	86312	70379
nets	12645	26010	86618	77821

Table 1. Benchmarks

IV.4. Timing Improvement

	Reference		SI		Improvement	
	Delay	CPU	Delay	CPU	Delay	CPU
Design 1	0.99	2668	0.86	2953	0.87	1.10
Design 2	1.80	6344	1.71	8359	0.95	1.32
Design 3	6.30	7349	6.09	11044	0.96	1.50
Design 4	5.12	11960	4.72	14919	0.91	1.25
Average					0.92	1.29

Table 2. Delay and runtime comparison

Because the coupling capacitance is critical to the net capacitance when the process technique goes to sub-0.18um, its value is key to determine the circuit speed. This algorithm can effectively reduce the hot spot coupling capacitance. Consequently, it helps to improve design performance. Table 2 compares the delay and runtime of the reference flow and the proposed flow. The delay numbers are in nanosecond, and the cpu time is in second. The experimental results showed 8% improvement could be achieved by adopting our proposed SI flow, while the run time penalty is within 30% of the traditional one.

V. Conclusions

In this paper, a cross talk driven placement algorithm is presented. This algorithm uses a novel probabilistic model to estimate the coupling capacitance at placement level, and uses density control during placement to reduce the number of highly coupled regions. The experimental results prove that our proposed algorithm is able to correctly predict coupling capacitance, and the placement density control approach can effectively reduce cross talk coupling after post-layout.

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Peak Noise (%)	Design 1		Design 2		Design 3		Design 4	
	Ref	SI	Ref	SI	Ref	SI	Ref	SI
0-10	56.39	56.77	60.60	60.33	72.24	72.93	79.42	80.34
10-20	21.77	21.89	19.96	21.19	15.51	15.44	10.84	10.79
20-30	11.53	12.42	9.89	10.21	6.80	7.40	6.48	6.38
30-40	6.60	7.93	6.13	7.20	3.38	3.95	2.73	2.41
40-50	3.12	0.95	2.54	1.02	1.62	0.27	0.49	0.08
50-60	0.57	0.04	0.87	0.05	0.44	0.01	0.03	0
60-70	0.02	0	0.01	0	0.01	0	0.01	0

Table 3. Peak noise comparison