Delta-sigma Modulator Based Mixed-signal BIST Architecture for SoC

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Abstract— This paper proposes a mixed-signal Built-In Self-Test (BIST) architecture based on a second-order delta-sigma modulator. This modulator, which incorporates a design-for-testability (DfT) circuitry, is capable of testing/characterizing itself using digital stimulus. This characteristic is attractive for implementing the modulator as an on-chip analog signal analyzer. When applied for mixed-signal BIST, the modulator-based analog signal analyzer is first characterized using digital stimulus. Then the analyzer is utilized to characterize the stimulus generator in the BIST application. Some critical implementation issues of the BIST architecture are also discussed.

I. Introduction

In general, Built-in Self-test (BIST) schemes based on Digital Signal Processing (DSP) for mixed-signal Integrated Circuit (IC) [1, 2, 3, 4] utilize a pair of converters – the digital-to-analog converter (DAC) and the analog-to-digital converter (ADC). The DAC produces an analog stimulus to test on-chip analog circuitry whereas the ADC converts the analog signal response from the circuitry into digital form for analysis. This setup allows the digital processor to test the on-chip analog circuitry without additional analog components or analog/mixed-signal ATE. However, both converters need to be tested/characterized before utilizing them as on-chip stimulus generator or signal digitizer. Several built-in self-test (BIST) schemes have been proposed for DAC and ADC, but most rely on one converter to test the other and vice versa. This interdependence would result in a deadlock.

The BIST approach reported in [5] relies on analog circuitry and reference voltages for measurements, which makes it vulnerable to analog parameter variations/imperfections. Another scheme for ADC/DAC BIST uses an efficient polynomial-fitting algorithm to reduce the computational complexity [6]. Like the previous schemes, this one requires both types of on-chip converters. Although the oscillation-test scheme does not require an externally provided test stimulus [7], it has yet to determine the converter noise floor, which determines the converter resolution. Another recently proposed scheme uses a linear ramp stimulus to test both the ADC and DAC [4]. However, testing both converters still require generation of on-chip stimulus, which was not characterized in the proposed scheme [4]. Reports [1, 4, 8, 9, 10] have shown that band-limited test stimulus can be easily generated on-chip using the delta-sigma modulation technique. However, the technique relies on an analog filter and voltage references to generate test stimulus. Hence, noises from these analog components would have direct effect on the stimulus These reports have yet to mention how to measure or ensure the quality of the test stimulus. Recently, a technique [11] is reported using a pseudo-random digital sequence to test a delta-sigma modulator by characterizing the latter's parameters. However, this method relies on characterizing the modulator parameters, which are not sufficient to model practical modulator to deduce the modulator SNR.

In this work, we propose to use a digitally-testable second-order delta-sigma modulator [12] as an on-chip signal analyzer in the mixed-signal BIST architecture. This modulator, incorporating additional design-for-testability (DfT) circuitry, requires only a digital stimulus to test/characterize itself, thereby, avoiding the expensive analog test stimulus generation for characterization. Then the characterized modulator is used to test the stimulus generator in the BIST architecture. Hence, the interdependence deadlock is broken.

This paper is organized as follows. Section 2 gives a background on the digital-stimulus testing technique and the digitally-testable second-order delta-sigma modulator. Section 3 presents the mixed-signal BIST architecture and the procedure for self-characterizing. Section 4 presents the simulation results to demonstrate the technique's capability for characterizing the digitally-testable second-order delta-sigma modulator. Section 5 concludes this paper with a discussion of implementation issues.

II. Background

Oversampled delta-sigma modulation has gained much popularity in analog-to-digital conversion applications since it was first proposed four decades ago. The delta-sigma modulator Analog-to-Digital converter (ADC) is based on the principle of trading time resolution for amplitude resolution, i.e. it converts an analog signal into a high-speed (tens of Nyquist rate) but low-resolution (typically single-bit) digital signal. The digital signal is digitally filtered to extract the information of the analog signal at a high resolution. With the continual scaling down of the transistor size, digital filters are getting cheaper to implement. Given the modulator's robustness in dealing with process variations, the delta-sigma modulator is suitable for integrated circuit implementation especially for System-on-chip (SoC) designs as the front-end signal digitizer/ADC. Other applications based on the delta-sigma modulation technique include digital telephony, digital signal processing, instrumentation, digital audio, and Built-In Self-Test (BIST) for mixed-signal circuits [1, 4, 8, 9, 10]. Today, most applications use a second-order single-bit delta-sigma modulator, even for applications that require 24-bit resolution [13, 14]. In the proposed mixed-signal BIST architecture, a digitally-testable single-bit second-order delta-sigma modulator is used as a signal digitizer.

The second-order delta-sigma modulator was first introduced by Candy [15]. Our study is based on the model introduced by Lainey et al. [16], which is shown in Figure 1. This modulator is easier to implement, as both of its integrators introduce a unit-sample delay into the signal path [17]. The modulator consists of two integrators, one quantizer and a DAC in the feedback loop. Each integrator consists of an adder, a delay block, and a unit feedback loop (z^{-1} denotes a sample delay as shown in Figure 1). Preceding the output y, is a two-level quantizer, which compares the second integrator output, I_2, with

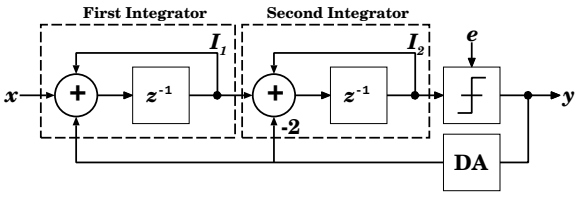

Figure 1: A second-order delta-sigma modulator

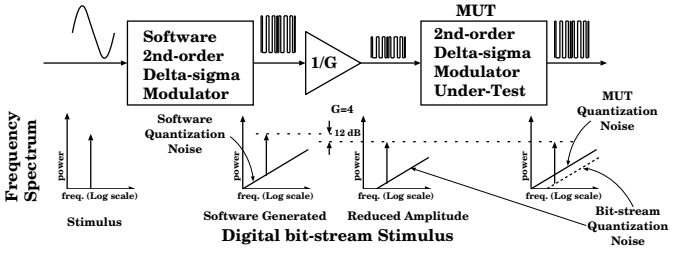

Figure 2: Digital Stimulus Measurement Technique

its threshold. It is common in analysis to model the quantizer as an adder of its input, I_2, and a random quantization noise, e. Hence, the modulator function can be represented by Equation 1 where the quantizer error, e, is associated with a second-order differential function.

$$y = xz^{-2} + e(1-z^{-1})^2 \quad (1)$$

II-A. Digital-stimulus Measurement Technique (DSMT)

This section presents the technique of using digital stimulus to measure the modulator performance/Signal-to-Noise Ratio (SNR). SNR is the ratio of the analog signal power to the noise power within the bandwidth of interest. Figure 2 shows the overview of the digital stimulus measurement technique.

First, a sinewave stimulus is numerically modulated into a digital bit-stream using a *software* second-order delta-sigma modulator. Then, the bit-stream amplitude is reduced to $1/4$ of the modulator's input range before applying it to the modulator-under-test (MUT). The amplitude reduction is to maintain the stable operation of the MUT.

The reduction reduces both the power sinewave stimulus and the quantization noise floor in the bit-stream by 12 dB. Due to the reduction, the quantization noise floor of the MUT now dominates that of the bit-stream at the MUT output. This reduction allows us to calculate the SNR of the MUT by calculating the ratio of the sinewave signal power to the MUT's noise power within the bandwidth of interest. Since stimulus power applied to the MUT is reduced by 12 dB, the SNR calculated using DSMT needs to be corrected with additional 12 dB to reflect the actual MUT performance.

II-B. The digitally-testable Delta-sigma Modulator

Some DfT circuitries are added into the second-order delta-sigma modulator to facilitate the accuracy of the proposed DSMT. Figure 3 shows the block diagram of the modified delta-sigma modulator. The 1-bit DAC in the feedback loop of the delta-sigma modulator is normally implemented with switches controlled by the quantizer output. The digital-to-analog conversions are realized when the quantizer output selects either the positive or negative reference voltage to the input of the adders.

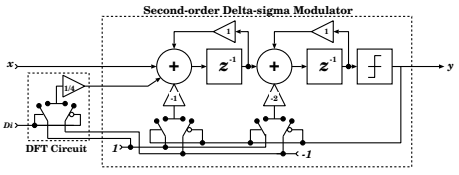

Figure 3: A DfT Second-order Delta-sigma Modulator

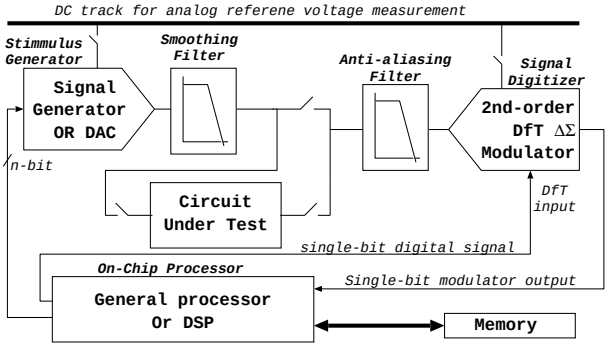

Figure 4: The Proposed Mixed-signal BIST Architecture

The difference between this DfT modulator and the conventional one is the additional DfT circuit. The DfT circuitry enables the modified modulator to use its internal reference voltages to test itself. This DfT circuit avoids the need to generate additional reference voltages. Through the digital input *Di*, the digital stimulus selects either of the two reference voltages to the gain block, which is part of the DfT circuitry. Then the gain block reduces the selected reference voltage by a factor of 4 before applying it to the first adder of the modulator. This is equivalent to generating a digital bit-stream with a quarter of the reference voltage levels. Hence, the quality and precision of the actual digital stimulus applied to the modulator is equivalent to that of the reference voltages.

III. The BIST Architecture

Figure 4 shows the BIST architecture for SoC with mixed-signal/analog circuits based on the proposed digitally-testable modulator. It contains three major blocks – the stimulus generator, the signal digitizer, and the processor. The stimulus generator, which could be a DAC or some analog circuitry, generates a test stimulus for the circuit-under-test (CUT). The stimulus generator output is usually filtered by a smoothing filter. The output of the CUT is sampled and modulated by the signal digitizer, which is the digitally-testable second-order delta-sigma modulator [12]. Prior to any sampling device, there is usually an a low-pass filter to prevent aliasing of high frequency component into the bandwidth of interest. The on-chip processor, which could be a general processor or a digital-signal-processor, will perform filtering and analysis on the modulated bit-stream from the signal digitizer. If the stimulus generator is a DAC, the processor will be required to generate the digital equivalent of the test stimulus for the DAC. If the stimulus generator is an analog circuitry whose function is to generate specific test stimulus, the processor only require a signal to start generating the stimulus.

III-A. BIST Architecture Self-Characterization

Prior to using the BIST circuitry to test other CUTs, itself needs to be characterized. The self-characterization procedure begins with measuring the performance of the delta-sigma signal digitizer by applying the digital test stimulus as proposed in the DSMT. The digital test-stimulus used in the DSMT can be generated by (1) modeling

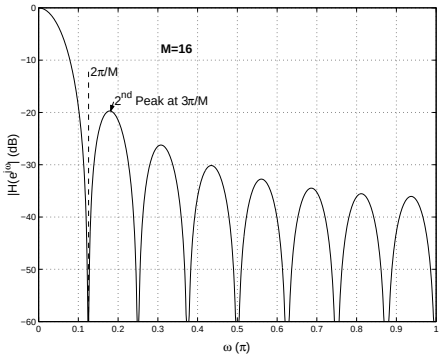

Figure 5: Frequency response of sinc^3 filter with M=16

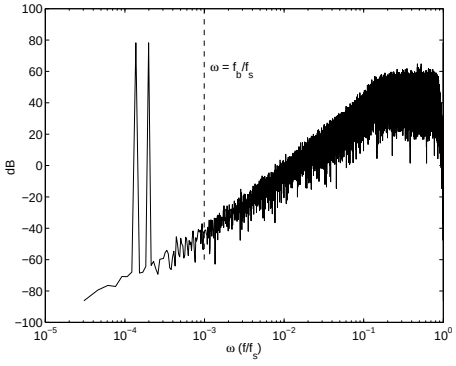

Figure 6: Frequency Spectrum of a Delta-sigma Modulated Bit-stream

the modulator using the processor, (2) pattern, pre-stored in the memory, sent through the processor, or (3) implementing the digital portion of the delta-sigma oscillators [9]. The output of the modulator is digitally filtered and Fast-Fourier Transformed (FFT) to calculate the modulator's characteristic, which include SNDR, noise floor, etc. The digital filtering may be implemented using the processor or on-chip digital blocks. The implementation of digital filter will be described in the next section. An additional track is proposed in the BIST architecture so that simple DC voltage measurement can be performed on the reference voltages through the track, which is made accessible to the external equipment. The DC measurement on the reference voltages can be made when the voltages are switched to the track. This track does not need to be low impedance since it is used only to measure DC signals.

After the modulator is characterized, the stimulus generator is characterized by analyzing the analog signal it generates via the two filters and the modulator. First, appropriate switching ensure the generated signal passes through the smoothing and the anti-aliasing filters before it is digitized by the modulator. Then the digitized signal is filtered and and FFT by the processor to analyze the quality of the generated signal. To reduce the load of the processor, the digitized signal is filtered and stored into the memory block. Then the processor would perform the FFT on the filtered signal, which is stored in the memory block. FFT on the filtered signal is less computational-demanding on the processor since the filtered signal will be shorter than the bit-stream.

III-B. Digital Filtering

In this BIST, digital filtering consists of an important process known as Decimation. Decimation is a process, used in our analysis, for converting the bit-stream to the desired pulse code modulation (PCM) at a lower sampling rate through a digital smoothing and re-sampling process [18]. In this process, the bit-stream is digitally filtered and down-sampled. A factor M down-sampling is a process where the signal sampling rate is reduced by M. This is equivalent to selecting one out of M samples from the signal. This section presents the design of a simple comb filter, which minimizes the coefficient word length, eliminates the need for a high speed parallel multiplier, and reduces the memory storage requirement. The design of the comb filter will take into account the aliasing effect associated with sampling and down-sampling to reduce the effect.

The Comb filters, also known as the sinc filters, are very attractive for implementation because they do not require the use of a digital multiplier. Although they are often used with other digital filter to achieve the desired PCM sampling rate, this application requires only the sinc filters. They are most efficiently implemented by cascading K stages of accumulators operating at the sampling rate of the modulator, followed by K stages of cascaded differentiators operating at the down-sampled rate [19]. The transfer function for a sinc filter with K stages and a down-sample factor M has the general form of

$$H(z) = \left(\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right)^K \tag{2}$$

and its frequency response is

$$\left|H(e^{jw})\right| = \left(\frac{1}{M}\frac{sin(\omega M/2)}{sin(\omega/2)}\right)^K \tag{3}$$

where

$$\omega = 2\pi f/f_s \tag{4}$$

Figure 5 shows the frequency response of the sinc^K filter with $M = 16$. When a signal is filtered by the sinc filter, its frequency components are shaped by the filter frequency response. The desired frequency components of the signal should be contained within the first peak of the sinc filter frequency response, and their attenuation should not be larger than, in this experiment we choose, 3 dB. This constrains the design of the sinc filter design with its parameters satisfying

$$\begin{aligned} 20log\left[\left(\frac{1}{M}\frac{sin(\omega M/2)}{sin(\omega/2)}\right)^K\right] &> -3dB \\ \omega &< 2\pi f_b/f_s \end{aligned} \tag{5}$$

where f_b is the bandwidth of the desired signal. When a signal is down-sampled by a factor M, its frequency components, whose frequencies are within $2\pi/M$, will be aliased by those, whose frequencies are greater than $2\pi/M$, in the frequency spectrum. Hence, to retain the quality of the signal after down-sampling, the 2^{nd} peak of the filter frequency response has to be low enough so that the alias effect is minimized. Therefore, the sinc filter design is constrained by its parameters satisfying

$$\begin{aligned} 20log\left[\left(\frac{1}{M}\frac{sin(\omega M/2)}{sin(\omega/2)}\right)^K\right] &> -130dB \\ \omega &= 3\pi/M \end{aligned} \tag{6}$$

for reconstructing a signal with 130 dB SNR. The largest peak of the filter frequency response for $\omega > 2\pi/M$ occurs at $\omega = 3\pi/M$. In general, a larger K will yield a larger attenuation. A larger M will yield more, and hence thinner, peaks in the filter frequency response.

Figure 6 shows the frequency spectrum of a dual-tone signal modulated into a bit-stream with a length of 2^{16}. A 114 SNR dB signal can be reconstructed from the bit-stream with proper filtering. Using

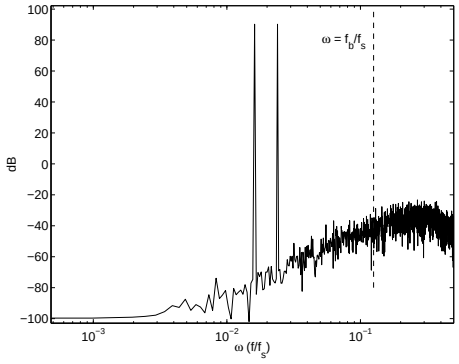

Figure 7: Frequency Spectrum of a Sinc-Filtered Signal

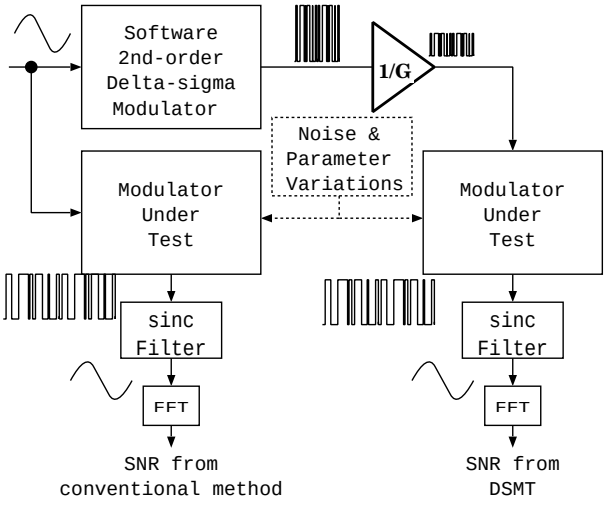

Figure 8: Simulation Setup for Validating the DSMT

Equations (5) and (6), K and M are calculated as 8 and 128, respectively. Using the calculated parameters, the reconstructed signal has a reduced length of 2^9.Its frequency spectrum is shown in Figure 7. There is no sign of significance aliasing on the reconstructed signal due to down-sampling, and the SNR of the dual-tone signal is retained at 114 dB.

III-C. Advantages and Limitations

The BIST architecture offers a mixed-signal test solution that does not requires external analog stimulus or analog signal analyzer. It could self-test without the interdependency of the stimulus generator and the signal digitizer. This self-test avoids the mentioned interdependence situation where most BIST architectures faced.

However, the BIST architecture can only characterize a CUT only up to the lowest resolution among the analog blocks in the BIST architecture. If the modulator has the lowest resolution among the BIST's analog blocks, then the CUT could only be tested up to the modulator's resolution. Since the modulator is based on oversampling technique, the BIST architecture is limited to testing CUT baseband characteristic. Other band of interest may be characterized by using bandpass sigma-delta modulator. One other draw back is the need to perform FFT to analyze the digitized signal. Performing on-chip FFT routine may consume too-much of the on-chip memory and processing power. This may be overcome by the mentioned digital filtering that reduces the length of digitized signal.

IV. Simulation Results

This section presents some numerical simulation results to validate the proposed Digital Stimulus Measurement Technique [12] used in

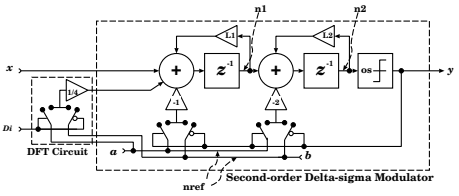

Figure 9: A Non-ideal Model for DfT Modulator

TABLE I: Parameters for Simulation Setup

Setup Parameter	Value
f_s	1
OSR	2^9
f_{BW}	$\frac{1}{2OSR}$
f_1	$\frac{2f_{BW}}{2^6}$
f_2	$\frac{3f_{BW}}{2^6}$
G	4
K	8
M	128

the self-characterization of the BIST architecture. Simulation results in this section shows that the error of estimating the modulator performance is reduced to a maximum of 3dB from 6 dB as previously reported [12]. The reduced error is attribute to performing analysis and FFT on the filtered modulator output. The filtering makes the analysis more robust to the selection of digitized signal segments. Each segment of a signal has the same length but different starting point. In [12], FFT and analysis are directly performed on the modulator output and different segment selections of bit-stream yeilds different SNRs.

IV-A. Simulation Setup

In our simulation, we assume to be testing a second-order delta-sigma modulator with 18-bit resolution, which is equivalent to 110 dB SNR. The SNR of the signal modulated by a second-order modulator is

$$\begin{aligned} SNR &= \frac{1}{n_o 2\sqrt{2}} \\ &\approx \frac{\sqrt{5}OSR^{5/2}}{2\pi^2\sqrt{2}} \end{aligned} \tag{7}$$

Assuming that e_{rms} is 1 and that the input signal RMS is $1/2\sqrt{2}$, a 110 dB SNR modulator requires an OSR of at least 430 calculated from Equation 7. In the setup, the OSR is 2^9, which is the next higher integer number to satisfy 2^n, where n is an integer. This number assignment is to ensure accurate analysis when performing FFT.

Figure 8 shows the experiment setup while Table I shows the parameter settings used in the setup. The sampling frequency of the modulator is set to a unit value while other parameters are referenced to it. The OSR determines the signal bandwidth, f_{BW}, which marks the frequency range bounding the noise components used to calculate the MUT's SNR. The analog stimulus is a dual-tone signal that contains two frequency components – f_1 and f_2. The stimulus is modulated by a software second-order delta-sigma modulator into a digital bit-stream with a length of 2^{16}. The amplitude of the stimulus is set to half of the software modulator's input range to ensure stable modulator operation. The digital bit-stream generated by the software modulator is the test stimulus for the proposed DSMT. The amplitude of the digital stimulus is reduced to a quarter ($1/G$) of the modulator input range before it is applied to the MUT. The output of the MUTs is filtered by a sinc filter before FFT is performed to determine the modulator SNR. Using Equation 5 and Equation 6, the sinc filter parameters, K and M, are calculated to be 8 and 128, respectively.

TABLE II: MUTs' PARAMETERS BOUNDARIES AND NOISE UPPER LIMIT

Parameter	Boundaries
$L1$	0.98 – 1
$L2$	0.98 – 1
a	0.9875 – 1.0125
b	-a
t	-0.0125 – 0.0125
$n1$	$1/2^{13}$ (max amplitude)
$n2$	$1/2^{5}$ (max amplitude)
$nref$	$1/2^{13}$ (max amplitude)

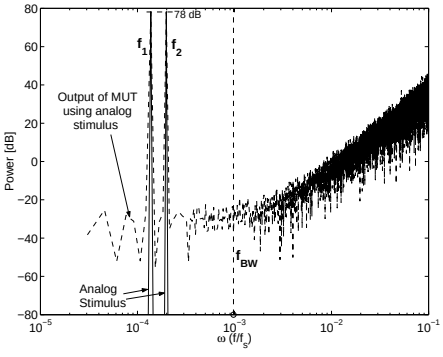

Figure 10: MUT Output Spectrum with Analog Stimulus Before Filtering

Table II shows the parameters' boundaries for emulating non-ideal MUTs. Each MUT have parameters' value ($L1, L2, a, b$ and t) delimited by the boundaries. In addition, noise components $n1, n2$, and $nref$, introduce at the outputs of the two integrators and the reference voltages of the MUT, are bounded by their upper limits. Hence, the stimulus to test the modulator is subject to such noise in this experiment setup as depicted in Figure 9. The boundaries are set so that each injected noise or deviated parameters could degrade the modulator's SNR by a maximum of 10 dB from that of the ideal modulator.

IV-B. Experimental Results

This section presents the simulation result of 500 MUTs generated according to the above mentioned criteria. Figures 10 and 11 show the output spectrums of an MUT when its input is applied with the analog and the digital stimulus, respectively. The deviated parameters and the injected noises in the MUT have caused the noise floor in the baseband of the MUT's output spectrums to rise. For an ideal modulator, the output spectrum will have a sloping down noise floor like that of the digital stimulus shown in Figure 11. The baseband is determined by the bandwidth, f_{BW} line shown in the figures. The effect of the amplitude reduction in the digital stimulus is already visible through the power reduction of the dual-tone signal from 78 dB to 66 dB as shown in Figures 10 and 11. The reduced-amplitude digital stimulus not only maintains the stability of the MUT, but also enables us to determine the SNR of the MUT by calculating the power of the MUT's noise floor within the baseband. This noise floor is significantly higher than that of the digital stimulus as shown in Figure 11.

The SNRs of the MUTs are calculated after the MUT's outputs are filtered by the sinc filter. The frequency spectrums of the filtered outputs are shown in Figures 12 and 13. Figure 13 shows that the power of the dual-tone signal in the digital stimulus and its corresponding MUT output remains 12 dB less than that in the original analog stimulus, as shown in Figure 12. This results in a 12 dB reduction in the SNR when DSMT is used. Hence, an additional 12 dB is added to the MUT SNR when the DSMT is used to performed the measurement.

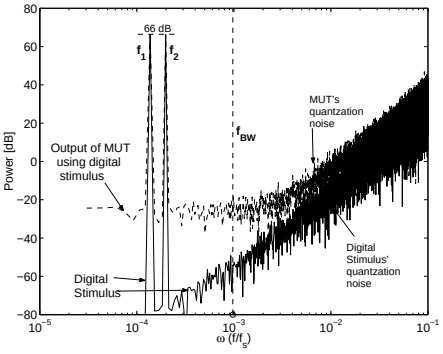

Figure 11: MUT Output Spectrum with Digital Stimulus Before Filtering

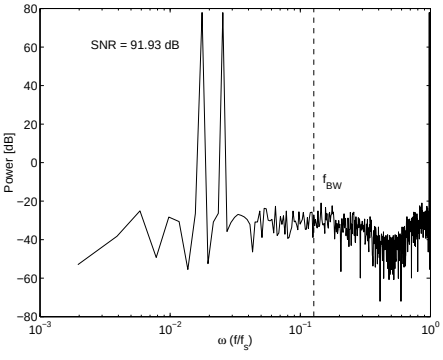

Figure 12: Filtered MUT Output Spectrum with Analog Stimulus

Figure 14 shows the histogram of the 500 MUTs' SNR, which is calculated using the conventional method in which the test stimulus is the analog signal. The 500 SNRs have a mean of 96.5 dB and a standard deviation of 5.6 dB. The SNR of the MUTs ranges from 84.2 dB to 113.8 dB. An ideal MUT has a 114 dB SNR, which is equivalent to that of a 18.7-bit resolution system.

Figure 15 shows the Histogram of the SNR measurement error of the 500 MUTs. A positive SNR measurement error denotes that the DSMT has overestimated the MUT SNR by the error amount. The measurement errors have a mean of 0.78 dB and a standard deviation of 0.86 dB. The measurement errors range from -1.67 dB to 3.4 dB. A 3 dB is equivalent to a $1/2$ least-significant-bit (LSB) of the MUT. These figures translate to a maximum measurement error of 0.57-bit resolution for an 18-bit system (110 dB). Figure 15 shows the DSMT tends to over-estimate the MUT SNR. This is due to the fact that the DfT circuitry feeds a negative noise from the reference voltages into the first integrator of the MUT. Hence, noises contributed by the reference voltages are effectively reduced at the first integrator, and the

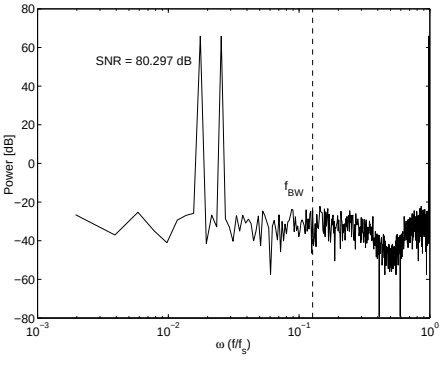

Figure 13: Filtered MUT Output Spectrum with Digital Stimulus

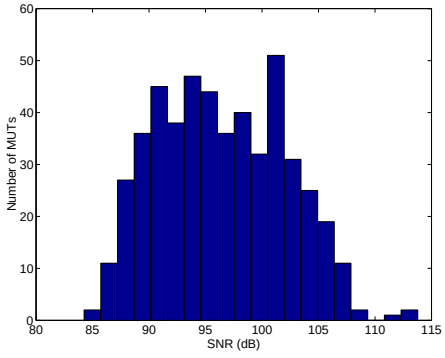

Figure 14: The SNR Histogram of the 500 MUTs

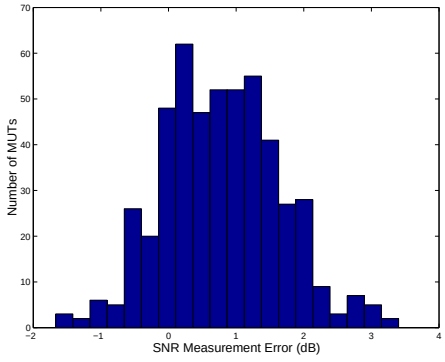

Figure 15: The Histogram of the SNR Measurement Error of DSMT

MUT's SNR measured by the DSMT is increased. However, this is true only if the noise at the reference voltage dominates the performance of the SNR. The results shows that the DSMT could closely estimate the performance of the modulator down to a maximum of error of 3 dB.

One point to note is that the additional DfT components (gain stage) included in the digitally-testable modulator are subject to noise influence and are not simulated in this work. This is because this noise component depends on the type of network used to implement the modulator. For a switched capacitor (SC) network implementation, a smaller gain stage ($1/G$) will require a capacitor with smaller capacitance, and hence, a smaller area to realize. A passive component with smaller area will introduce a larger flicker noise component. For a resistor capacitor (RC) network implementation, however a smaller gain stage will require a larger resistance to realize. As noise generated in a resistor is proportional to its value and inverse proportional its area, one can carefully consider these factors when designing the DfT sigma-delta modulator.

V. Conclusion

In this paper, we have presented a DSP-based mixed-signal BIST architecture with a digitally-testable signal digitizer. This digitizer breaks the deadlock commonly found in the mixed-signal BIST architecture where the analog stimulus generator and the analog signal digitizer function inter-dependently in performing self-characterization. The signal digitizer, a DfT delta-sigma modulator, requires only a digital stimulus to perform characterization. The test time in the measurement technique is also significantly shorter than the static linear ramp testing. As mentioned in the experiment, the DSMT requires 512 samples of filtered signal to analyze a 18-bit modulator, while static test would require 2^{18} samples. Simulations, with noise injected and parameters varied, are performed to verified the robustness of the proposed measurement technique, and hence, the proposed BIST architecture.

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