A Novel LCD Driver Testing Technique Using Logic Test Channels

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Abstract

This paper proposes a novel voltage measurement technique for LCD driver testing by the use of logic test channel of an ATE. The method is able to achieve less than 1mV error with the presence of 32mV RMS noise.

1. Introduction

Liquid crystal displays (LCD) have been widely used in electronic systems. It is not only used in portable devices, such as notebook computer, personal data assistant, and cellular phones, for its portability and low power consumption but also replacing CRT for computer monitoring for its small foot print and zero radiation hazard. Due to its popularity, LCD driver *integrated circuits* (IC) have form an important sector in the IC industry by itself. Not only its test techniques differ from that of conventional digital and analog ICs, it also requires specialized testers for testing.

A LCD driver is shown in Figure 1. Every output channel of a LCD driver IC can be regarded as a *digital to analog converter* (DAC) output. It outputs the brightness level of a pixel in analog form according to the RGB inputs. The RGB input is the output of ADCs shared by multiple output channels in time by *sample and hold* (S/H) modules. The ADC might have 4, 6, 8, or 10 bits in resolution depending on the applications. Hence, one can treat and test a LCD driver channel as a DAC.

For DAC testing, the signal level can be measured by the *precision measurement units* (PMU). However, due to its large number of output channels, it requires a significant amount of PMUs. Hence, dedicated LCD driver testers were designed and manufactured to reduce the test time and improve the test throughput. Although the dedicated testers perform well on LCD driver testing, it is still an expensive solution. In this paper, we would like to investigate a novel approach to reduce the test cost as well as the test time from a theoretical point of view.

Our approach is to utilize dual comparators in *pin electronic* (PE) circuits for voltage measurement. It allows one to use logic testers for LCD driver testing without additional investment. The proposed technique is very simply. Every PE has a dual comparator pair to compare the DUT output voltage with V_{R+} and V_{R-} to determine its logic value. Here, V_{R+} and V_{R-} are V_{OH} and V_{OL} pluses or minuses guard bands. Voltage measurement can be achieved by the same dual comparator pair. As shown in Figure 1, the output voltage V_x is compared to V_{R+} and V_{R-} which are set to the vicinity of V_x. If V_x is smaller than V_{R+} and larger

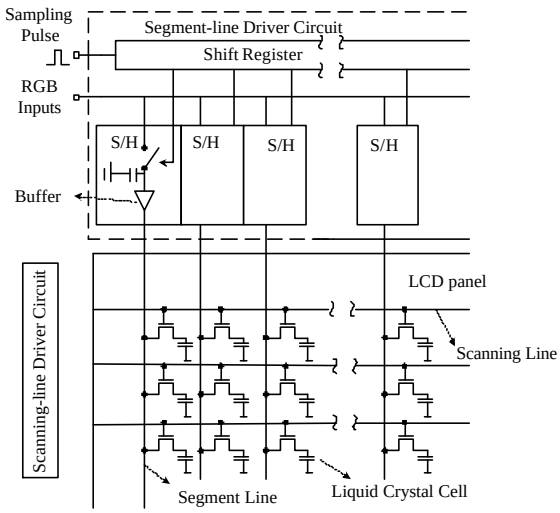

Figure 1. LCD Driver Circuit Structure

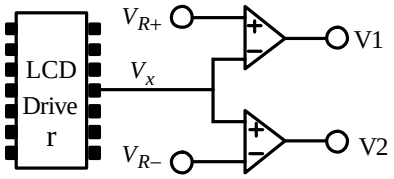

Figure 2. Dual comparator for voltage measurement

than V_{R-}, one can say that V_x is V_C with a tolerance of 0.5 ΔV_R. Here,

$$V_C = \frac{1}{2}(V_{R+} + V_{R-}) \tag{1}$$

$$\Delta V_R = V_{R+} - V_{R-} \tag{2}$$

The proposed method has the advantages as follows. It accomplishes voltage measurement by the use of digital test channel only. Second, one can set desire ΔV_R for the wanted tolerance. But, it has certain drawbacks. First, the method is affected by the noise which can be very serious if ΔV_R is small. Second, one cannot set V_{R+} and V_{R-} close enough to minimize the tolerance due to the limited accuracy. Third, it can be time consuming to adjust the reference voltage every time a new voltage value is to be measured.

In this paper, we would like to address the LCD driver testing problem, propose a novel voltage measurement methodology, analyze the technique mathematically, and verify the methodology by the simulation and experimental data in the following sections.

2. Test Methodology and ItsAnalysis

The proposed structure for LCD driver testing is shown in Figure 2. As indicated previously, the noise is the major effect that affects the accuracy of the measurement. As we know, not only V_x but also V_{R+} and V_{R-} are coupled with noise. Suppose that the noise has a normal distribution function, the relationship among V_x, V_{R+}, and V_{R-} are shown in Figure 3. Here we assume that V_i is not at the middle of V_{R+} and V_{R-}. Since V_{R+} and V_{R-} are supplied by voltage sources, their noise powers are assumed to be smaller than that of V_x. Here, s_x^2 is the variance of signal noise, s_c^2 and s_d^2 are the variances of the common mode and differential mode of the reference voltages.

Noise is often unwanted and regarded as an ill effect. The proposed method utilizes the noise effect to determine the voltage level. As Figure 3 shows, V_x can be larger or smaller than V_{R+} and V_{R-}, depending on the relative noise level. The proposed method takes multiple samples of binary outputs of the comparators (V1 and V2) and analyzes the probability of its outcomes to determine how far does V_x deviate from V_C, marked as *X* in the figure.

To simplify the mathematical analysis, we combined three noise effects into two. Here, we assume that all the noises are uncorrelated. Note that correlated noise often causes systematic errors correctable by calibration. Here, the common mode noise and signal noise are combined into one and leave the differential noise as another. The final form is shown in Figure 4.

In one sample, the input signal may located in one of the three regions, L1 ($V_x < V_{R-} < V_{R+}$), L2 ($V_{R-} < V_x < V_{R+}$), and L3 ($V_{R-} < V_{R+} < V_x$). Suppose that P_{V_x} and $P_{V_{R+}}$ are the probability density function of the input signal and reference voltages, the probability in each region, marked as P_{L1}, P_{L2}, and P_{L3}, are calculated as follows.

$$P_{Vx}(x) = \frac{1}{\sqrt{2p}\, s_c} e^{-(x-\overline{X})^2 / 2 s_c^2} \qquad (3)$$

$$P_{V_{R+}}(y) = \frac{1}{\sqrt{2p}\, s_d} e^{-(y-\overline{VR+})^2 / 2 s_d^2} \qquad (4)$$

$$P_{L1} = P_{Vx<V_{R-}<V_{R+}} = \int_{-\infty}^{V_{R-}} p_{V_x}(x) \int_{V_{R-}}^{\infty} p_{V_{R+}}(y) dy dx \qquad (5)$$

$$P_{L2} = P_{V_{R-}<Vx<V_{R+}} = \int_{V_{R-}}^{\infty} p_{V_x}(x) \int_{Vx}^{\infty} p_{V_{R+}}(y) dy dx \qquad (6)$$

$$P_{L3} = P_{V_{R-}<V_{R+}<Vx} = \int_{V_{R-}}^{\infty} p_{V_x}(x) \int_{V_{R-}}^{Vx} p_{V_{R+}}(y) dy dx \qquad (7)$$

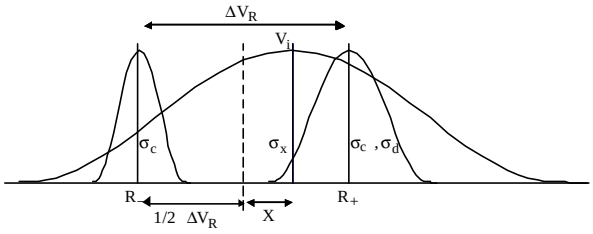

Figure 3. Noise model for the test system.

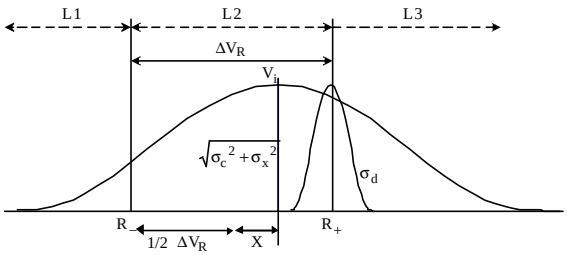

Fig. 4 The simplified noise model

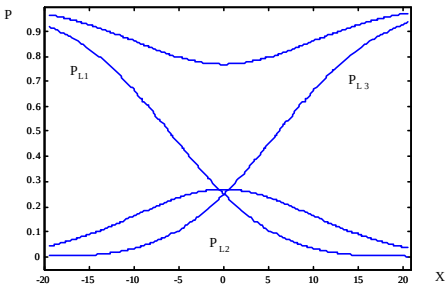

Figure 5. P_{L1}, P_{L2}, and P_{L3} v.s. *X*.

According to (5), (6), and (7), P_{L1}, P_{L2}, and P_{L3} as function of *X* are shown in Figure 5. In this case ΔV_R =20. V_x equals V_{R-} for *X= -10* and equals to V_{R+} for *X=10*. Here 1 denotes a normalized voltage value, for instance 1mV. As one can see, when X is in the negative territory, P_{L1} is greater than P_{L3}. P_{L1} will reach 1 if *X* is $-\infty$. As *X* increases, P_{L1} decreases and P_{L3} increases. P_{L2} is maximal when *X=0*, V_x located at the middle of the V_{R+} and V_{R-}. The upper most line is the summation of P_{L1}, P_{L2}, and P_{L3}. As one can see, it is not equal to 1. The reason is the presence of the differential noise s_d^2. Since we assume uncorrelated noise, it is possible that V_{R+} might be smaller than V_{R-}. Hence we have to exclude these cases from consideration. Figure 6 shows the cases of different noise figures. In the first case, four separations are used and in the second case three separations are used. Figure 5 and 6 are derived mathematically. Figure 7 shows the simulation results with 2048 samples being taken. The dashed lines are the mathematical integration results. The solid lines are the simulation results. In every sample, noises are randomly assigned according to the distribution functions.

Figure 5 shows P_{L1}, P_{L2}, and P_{L3} as function of X. It can be used in the other way around. One can build the curves or tables in advance. Suppose that X is unknown. After multiple samples being taken, P_{L1}, P_{L2}, and P_{L3} can be obtained statistically. By table lookup, one is able to find X from a set of (P_{L1}, P_{L2}, P_{L3}). Of course, the more the number of samples are taken, the more the accuracy will be.

The proposed methodology is to (1) sample the outcomes of the dual comparators, (2) obtain the probability of (P_{L1}, P_{L2}, P_{L3}), (3) look up to the pre calculated table to determine X. The technique solves all three problems mentioned earlier. First, V_{R+} and V_{R-} need not be set very close to minimize the tolerance. Second, one setting of V_{R+} and V_{R-} can be used for multiple measurement. The input need not be in the middle of V_{R+} and V_{R-}. The remaining issue is the noise effects.

It is well known that noise can be suppressed by the use of over sampling. The *signal to noise ratio* (SNR) improves 3dB by taking and averaging twice the samples. The question is how many samples are needed to obtain the required accuracy and confidence level.

3. Confidence Level Analysis

The number of samples being taken is closely related to the accuracy of the table look up. Suppose that the probability of being in a certain region is p. If one sample is ta ken, the variance is

$$s^2 = p * (1 - p) . \tag{8}$$

If n samples are taken and averages, the variance is

$$s_n^2 = \frac{s^2}{n} . \tag{9}$$

According the Central Limit Theorem, the distribution will approximate a normal distribution regardless of what the original distribution is if the number of samples is large. Here, the confidence intervals can be written as

$$Z = \frac{\overline{X} - \mu}{\sigma / \sqrt{n}} . \tag{10}$$

According to Gaussian function, a factor 3 represents 99.7% confidence level. Figure 8 shows the $3s$ interval for 64 samples being taken and averaged. The outer boundary is obtained by mathematical derivation of the possible P_{L1}, P_{L2}, and P_{L3} regions for different X's. The lines inside the regions are obtained by simulation using random data.

Of course, the more the samples are taken, the narrower the region will be. In Figure 8, one may notice that the confidence region may exceed 1 or less than 0. It is meaningless probability wise. This is due to the fact that normal distribution does not model the real case

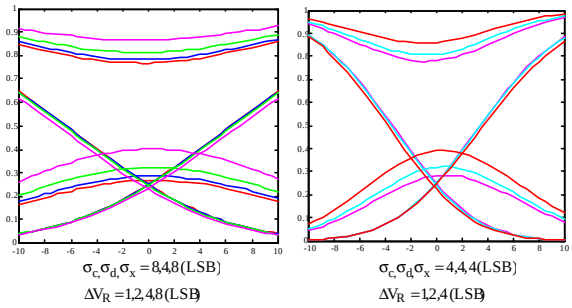

Figure 6. Two case studies.

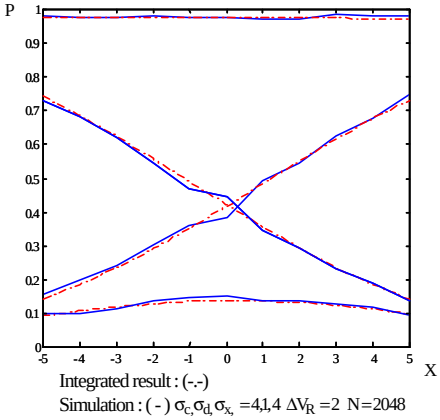

Figure 7. Simulation v.s. mathematical derivation.

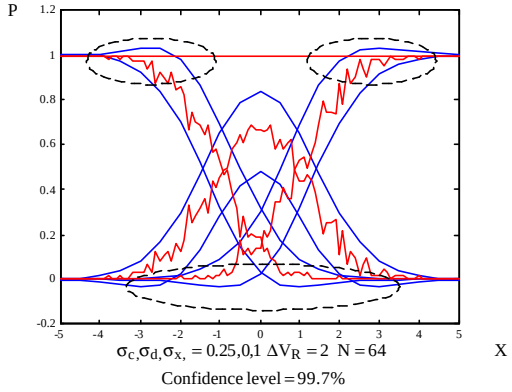

Figure 8. Simulation results

closely. For instance, if the average number of people in a room is 6 and the standard deviation is 2, there is 0.15%of the chance that there will be negative number of people in the room. We use the Fermi-Dirac distribution function to modify the Gaussian function and solve the problem. Here, we will not go into the detail. After being verified by mathematical analysis and simulation, the next step is to verify the technique via experiment.

4. Experiments - OP Based Dual Comparator

To verify the proposed methodology, we have built a dual comparator circuit on the bread board. The circuit diagram is shown in Figure 9 and the picture is shown in Figure 10. Two DACs are used to setup the reference voltages. DAC inputs are supplied by a logic analysis system and the compared outputs are sampled by the same analyzer. The log file is transferred to a *personal*

computer (PC) for data analysis. Figure 11 shows the noise waveform and Figure 12 shows the comparator outputs waveforms under the influence of noise. As one can see, V_x is not always smaller than V_{R+} and larger than V_{R-}. Such a noise effect is what we expect and what we want to utilize.

We have tested 9 conditions with different number of samples, 64, 256, 1024. Table 1 sows the case with 256 samples. Every case has been repeated 64 times to verify the consistency and obtain the statistical data. In the table, the rows represent (1) the condition index (A to I), (2) the comparison range ΔV_R in mV, (3) the input voltage level set at 1V, (4) the noise RMS value (s), (5-7) probability of P_{L1}, P_{L2}, P_{L3}, (8) the mean of the measurement error, and (9) the standard deviation of the measurement error both in mV. As one can see from the table, the error is relatively small, less than 1mV, except G. Here, noise (16.4mV) is relatively small as compare to the comparison range (32mV). In this case, we should be able to reduce the comparison range to case D (16mV).

Table 1. OP based test results

	A	B	C	D	E	F	G	H	I
ΔV_R	8	8	8	16	16	16	32	32	32
V_{in}	1V	1V	1V	1V	1V	1V	1V	1V	1V
RMS	11.6	16.4	22	11.6	16.4	22.7	16.4	22.6	31.4
P_1	0.33	0.44	0.47	0.10	0.34	0.42	0.05	0.31	0.39
P_2	0.37	0.13	0.05	0.81	0.32	0.15	0.94	0.38	0.21
P_3	0.30	0.43	0.47	0.08	0.34	0.42	0.01	0.31	0.40
ΔV_{in}	0.58	0.17	-0.02	1.04	0.00	0.00	5.73	0.11	-0.48
Std	0.48	0.27	0.30	1.16	0.37	0.28	1.63	0.29	0.35

* In mV unless otherwise specified

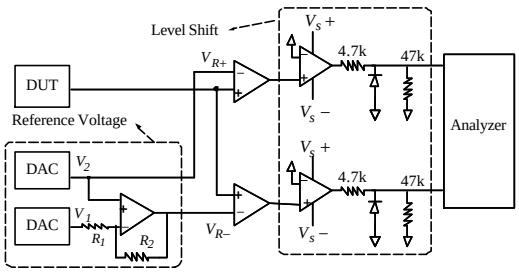

Figure 9. The OP based test circuit.

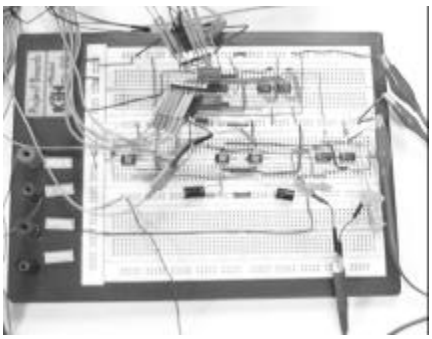

Figure 10. The OP based test circuit.

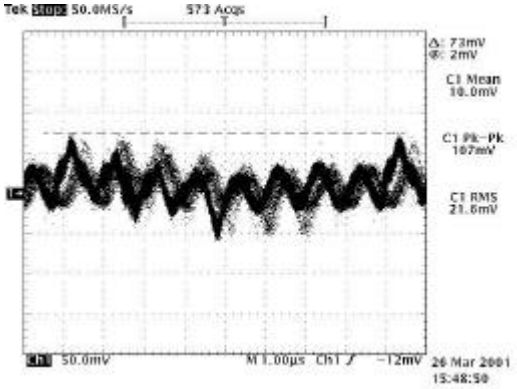

Figure 11. Noise waveform

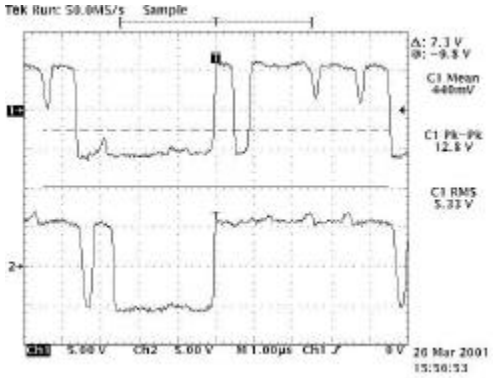

Figure 12. Comparator output waveforms.

5. Experiments – Vender PE Evaluation Kit

We have also used vender's PE evaluation kit for the experiments. Figure 13 shows the schematic diagram of the PE circuit and Figure 14 shows the picture of the evaluation kit setup.

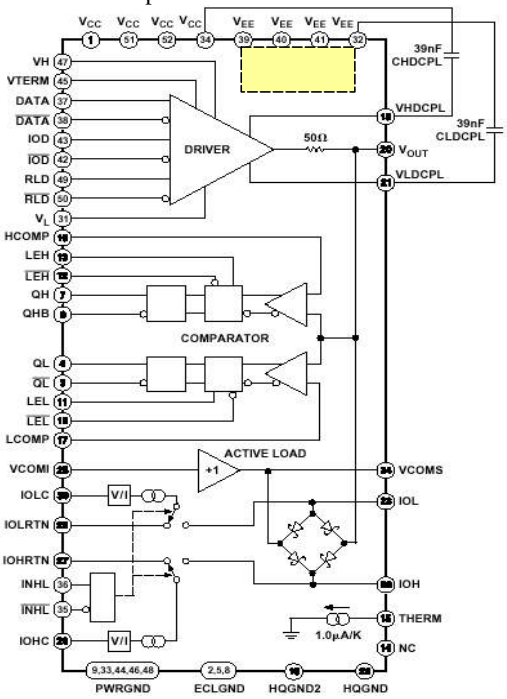

Figure 13. PE IC schematic diagram.

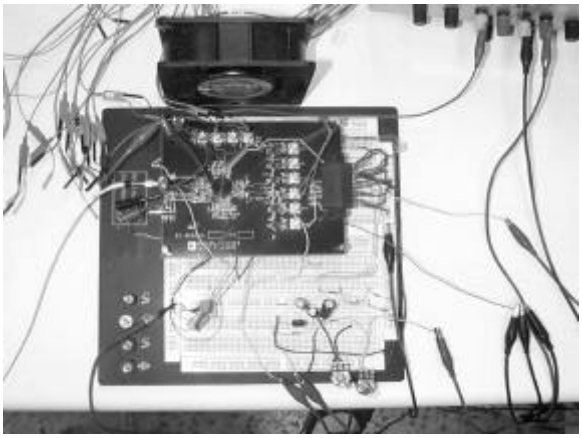

Figure 14. Picture of PE evaluation kit.

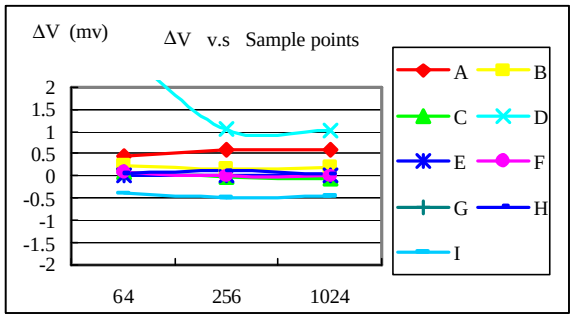

Figure 15. ΔV vs. sample points for OP based

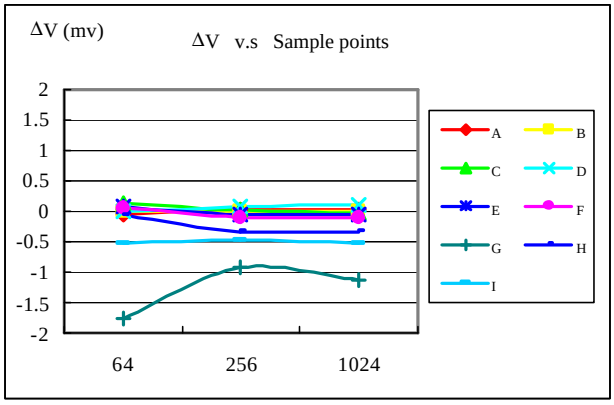

Figure 16. ΔV vs. sample points for PE

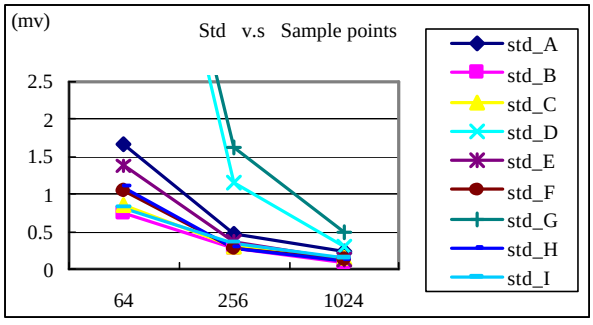

Figure 17 Std vs. sample points for OP based.

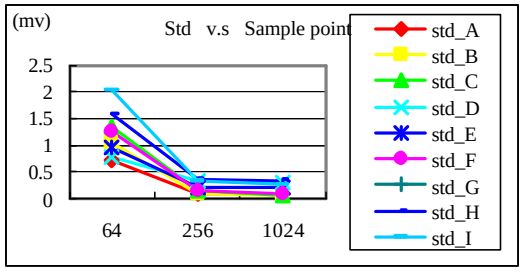

Figure 18. Std vs. sample points for PE

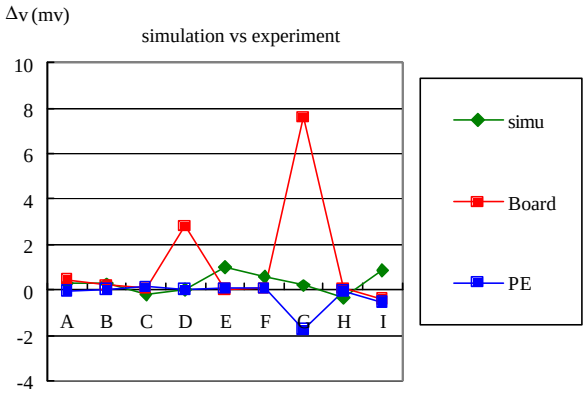

Figure 19. Simulation v.s. experimental results

6. Experimental Results and Comparisons

We have run numerous experiments on the OP based comparators and the PE evaluation kit. The data, as those shown in Table 1 are summarized in the following four figures. Basically, it shows the mean (Figure 15,16) and the standard deviation (Figure 17,18) of the measurement error v.s. the sample points.

As one can see, the mean of the error is less than 1mV with a noise up to 32mV for all cases except the one with relatively small noise as being discussed. For PE evaluation kit, the standard deviation of the error is less than 0.5mV when the number of samples is 256. For the OP based comparators, the standard deviation of the error is also less than 0.5mV except for those peculiar cases.

Figure 19 summarizes the simulation and experimental results for n=256 cases. As one can see, except D and G, which have relative low noise, all the cases match the simulation results very well. A total of 256 samples sounds a lot. However it can done in less than 1.3us using a 200MHz tester.

Figure 20 and 21 show how noise RMS value and ΔV_R affects measurement error. X axis is the ration of noise RMS value to ΔV_R. The larger the number, the larger the noise. Y axis is the measurement error in percentage of noise RMS value. This will normalize the error to the noise amplitude and ΔV_R.

In IEEE Std. 1057-1994 [4], the noise suppression is often achieved by taking and averaging multiple samples.

The effect is given as % of RMS noise. Table 2 shows the noise suppression effect of IEEE Std. 1057 and the proposed method all with 99.7% confidence level. Our data are taken from the experimental results. As Table 2 shows, our method has a slight edge in noise suppression over IEEE Std. 1057 due to the use of dual comparators. A single comparator is only a binary quantizer or 1-bit ADC. With dual comparator, we are able to transform them into an ADC with better noise suppression characteristics.

7. Conclusions

In this paper, we have proposed a novel voltage measurement technique using the dual comparators in a logic pin electronic circuit. Such a technique can be applied to LCD driver IC testing due to its large amount of output channels. The method set the reference voltages to the vicinity of the voltage to be measured. By analyzing the multiple samples of the comparator outputs, we are able to determine the voltage level accurately. The methodology has been analyzed thoroughly by statistical analysis and reassured by the simulation using random data. To further confirm the proposed technique, we build a OP based dual comparator circuit and use a vender PE evaluation kit for the experiments. The experimental results show that our technique is able to achieve very high accuracy. The mean and standard deviation of the errors are less than 1mV and 0.5mV respectively for the case when noise is 32 mV in RMS by taking less than 256 samples. Such a noise compression property can be valuable for field application where large noise is unavoidable.

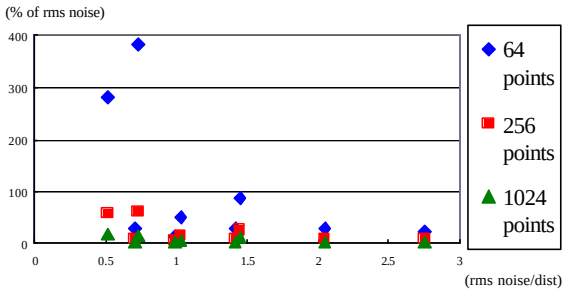

Figure 20. Error statistics for OP based.

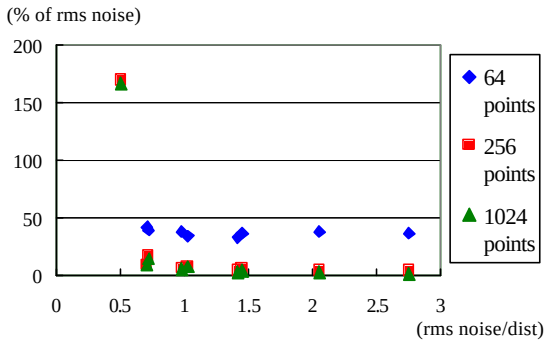

Figure 21. Error statistics for PE evaluation kit.

Table 2. Our Method v.s. IEEE Std. 1057

	IEEE 1057 test standard	Our test
Record length (samples)	Precision (% of RMS noise)	Precision (% of RMS noise)
64	45 %	37.6 %
256	23 %	7.2 %
1024	12 %	5.9 %
4096	6 %	3.4 %

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