Efficient loop-back testing of on-chip ADCs and DACs

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Abstract— This paper presents an efficient approach to testing on-chip Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs) in loop-back mode. On-chip digital signal processing units can be used to generate stimuli. With this methodology, go/no-go tests as well as characterization of the individual ADCs and DACs are possible. The proposed approach is simple and overcomes the low parametric fault coverage of conventional loop-back tests. Simulations on a Matlab model of loop-backed converters are presented to validate the feasibility of the method.

I. Introduction

The great demand for mixed-signal devices from the telecommunications, embedded systems and multi-media markets has increased the importance of research into cost-effective tests for mixed-signal devices. However, there are many limiting factors to testing analog parts in an efficient fashion. These include the large number of tests and long test times for some analog circuit specifications, as well as the high cost of analog test equipment. Another severe problem is the lack of easy accessibility to analog modules on a mixed-signal chip.

Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs) are common modules on many mixed-signal chips, since they provide the interface between the outside (analog) world and the digital circuit on the chip. In addition, many of the mixed-signal built-in self-test (BIST) schemes [1, 2] require the use of both ADCs and DACs. Thus, testing ADCs and DACs becomes a crucial part of the overall test strategy.

There are many ways of implementing tests for ADCs and DACs. One of them is to test ADCs and DACs directly (the conventional method for discrete parts). The method applies input signals and input codes to ADCs and DACs, respectively, and the outputs of these devices are measured by voltmeters and oscilloscopes. Various computations are performed on the measured data to obtain the static and dynamic characteristics of the converters. While this method provides accurate results, it requires long test times, expensive test equipment and direct accessibility to the modules.

In order to reduce these high test costs, a Hybrid Built-In Self-Test (HBIST) technique was introduced [1]. This method reuses the existing on-chip hardware and signature compaction schemes which are used in digital BIST (Fig. 1(a)). The loop-back test scheme used in transmission lines has also been proposed as a solution to the problem [3]. The approach has been shown to be effective in detecting catastrophic faults. However, losses in parametric fault coverage may be expected due to pseudo-random inputs that are different from the test inputs for ADC and DAC specifications. Fig. 1(b) shows another approach to testing ADCs and DACs [2]. In this approach a sequential test method is employed, in fact, this method is similar to the conventional method mentioned above. While one can expect better fault coverage for catastrophic and parametric faults than HBIST, a long test time is still expected .

In this paper, we propose a simple and efficient test method for on-chip ADCs and DACs that exploits loop-back test, and uses the existing digital processing units to generate input stimuli. The particular test strategy largely depends on the type of circuitry under test. Due to the demand for simplicity and tolerance to parameter variations in analog components, oversampling $\Delta\Sigma$ ADCs and DACs has gained popularity. Therefore, we focus on oversampling $\Delta\Sigma$ on-chip ADCs and DACs as the target of our new approach.

The organization of this paper is as follows. We review loop-back test methods in Section 2. The basic concepts of our method are explained in Section 3. Section 4 discusses the modeling of the loop-backed converters with Matlab and the initial simulation with SIMULINK. The equations extracted from this initial simulation are used to characterize the converters. Comparison of the solutions from the characterized equations and exhaustive simulation on Matlab model with SIMULINK are presented to validate the feasibility of our method in the following section. Finally, conclusions are drawn in the last section.

II. Review of on-chip ADC and DAC test

In communication systems, loop-back modes are generally provided for the test of the transmitter and receiver circuitry [3]. The output of a transmitter is usually connected directly to the input of a receiver. This method has been applied to test and diagnostic solutions for microprocessor and Digital Signal Processor (DSP) based boards. The inputs and outputs of each element in these boards can be tested without connecting any other components through the loop-back test [4]. While loop-back tests have been developed for components on a chip using

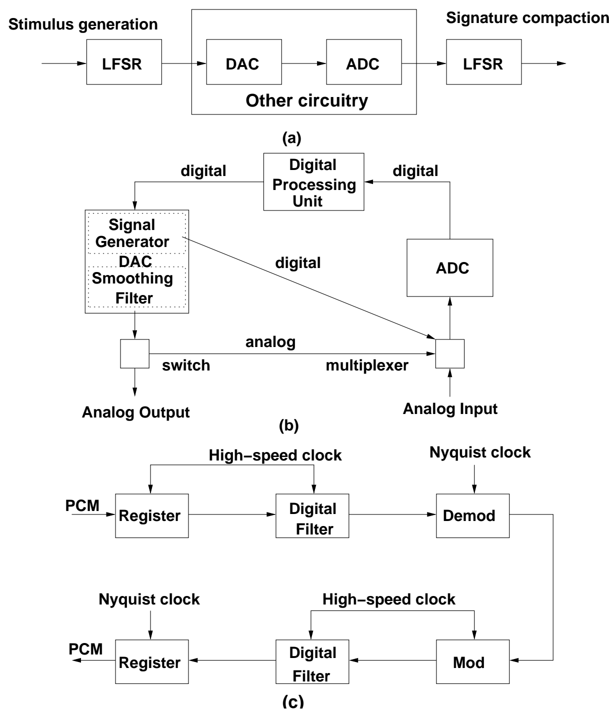

Figure 1. The various test set-up for ADCs and DACs

the on-chip ADCs and DACs [5, 6], loop-back tests for the on-chip ADCs and DACs themselves have rarely been attempted due to obstacles such as fault masking and low fault coverage.

Fault masking occurs because some faults in the DAC can be masked by other faults in the ADC. Fig. 1(c) shows the overall block diagram of the loop-back path from the input of an oversampling $\Delta\Sigma$ DAC to the output of an oversampling $\Delta\Sigma$ ADC. The behavior of each element can mask or cancel out the faulty behaviors of other elements. To prevent this, the circuits should be implemented in such a way as to reduce the possibility of fault masking. Internal monitoring nodes need to be used or suitable test vectors need to be developed in order to detect fault masking.

Input stimulus generation can also be one of the difficulties in loop-back testing. Two kinds of loop-back modes can be considered for testing oversampling $\Delta\Sigma$ converters on a chip. One is analog loop-back, which loops the output of DAC back into the input of ADC. The other one is digital loop-back, which loops the output of ADC back into the input of DAC [5, 6]. Input stimuli can be generated either from external instruments or from DSP. Most mixed-signal devices are developed based on DSP, which can emulate high cost external signal generators using DACs. Therefore, DSP-based testing of mixed-signal devices is preferred [7]. In loop-back mode, the fact that ADCs and DACs are tested at the same time should be considered in the generation of the input stimulus.

III. Loop back with monitoring

The main focus of the proposed methodology is to extract ADC and DAC characteristics from the loop-backed output responses. Both the input stimulus and the loop-backed output responses are digital. In analog loop-back mode, in which the output of the DAC is connected to the input of the ADC, there is no direct way to monitor the loop-backed analog behaviors. Furthermore, the final digital outputs of the ADC do not provide much information on the individual loop-backed converters. This results in fault masking and low fault coverage. In addition, this makes characterizing the ADC and the DAC very difficult. In fact, monitoring internal nodes can provide more information than monitoring the final digital outputs of the ADC. Thus we add the monitoring of internal nodes to the conventional loop-backed scheme. The internal nodes provide useful data which can be used to split the loop-backed output responses of the individual units. Note that the outputs of the internal node need to be digital bit streams in order to perform DSP-based testing. Details of the selection of internal nodes and the test techniques related to those nodes are explained below.

A. Internal node selection

The selection of internal nodes depends on the type of converter and the specifics of its circuitry. In the case of oversampling $\Delta\Sigma$ converters, spectral separation between the input signal and the noise introduced by quantization is possible. As mentioned earlier, the final digital outputs of the ADC do not provide much information on the individual loop-backed converters. However, the spectral density of the digital bit stream of the ADC before digital filtering shows the frequency response which can be split into individual ADC/DAC characteristics. While the in-band characteristic shows both ADC and DAC characteristics, the out-of-band characteristic shows mainly the ADC characteristic due to filtering of the out-of-band noise by the low-pass filter in the DAC, as can be seen in Fig. 2(a).

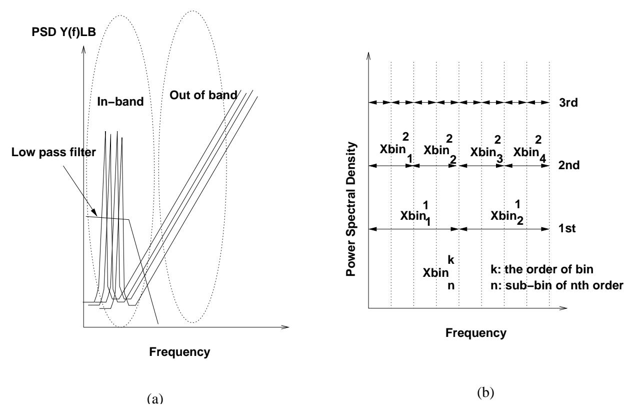

Figure 2. The frequency response of a selected internal node and frequency binning

While conventional converters are generally tested by comparing the values of corresponding inputs and outputs of a sample, oversampling $\Delta\Sigma$ converters are tested by calculating the RMS values of modulation noise and its power spectral den-

sity [13]. In the case of a second order $\Delta\Sigma$ converter, the power spectral density can be expressed as follows.

$$\begin{aligned} Y(f)_{DC} &= STF_{ADC}(N(f)_{DAC, f \le f_{LF}}) + NTF(f)_{ADC} \\ &\simeq k|4e_{rms}\sqrt{2T}sin^2(\pi f)|_{f \le f_{LF}} + \\ &\quad n_{DAC} + 4e_{rms}\sqrt{2T}sin^2(\pi f) \end{aligned} \quad (1)$$

$$\begin{aligned} Y(f)_{AC} &= STF_{ADC}(STF_{DAC}(X(f)) + N(f)_{DAC, f \le f_{LF}}) \\ &\quad + NTF(f)_{ADC} \\ &\simeq A_0\delta(f - f_0) + k|4e_{rms}\sqrt{2T}sin^2(\pi f)|_{f \le f_{LF}} \\ &\quad + n_{DAC} + 4e_{rms}\sqrt{2T}sin^2(\pi f) \end{aligned} \quad (2)$$

Here, STF stands for the signal transfer function and NTF stands for the noise transfer function. e_{rms} is $\sqrt{\frac{\Delta^2}{12}}$. Δ is the level spacing. For two-level quantization (+1V, -1V) Δ is 2. A_0 is the amplitude of a sine wave and f_0 is the fundamental frequency. The incoming signal of a digital $\Delta\Sigma$ modulator and the outgoing signal of an analog $\Delta\Sigma$ modulator are sampled at the sampling frequency $f_s = 1/T$. Equation 1 is the power spectral density function of a constant input code generated by DSP, and Equation 2 is the power spectral density function of one-tone sine input code generated by the DSP. The power spectral density of the ADC, before digital filtering the out-of-band frequency, primarily shows the characteristics of the ADC. The power spectral density within the in-band frequency shows the characteristics of both the ADC and the DAC. In our proposed method, the ADC characteristics which obtained in the out-of-band frequency are used to extract the characteristics of the DAC. Thus, more errors in the DAC characteristic than the ADC characteristic are expected.

B. Extraction of dynamic characteristics from frequency binning

In order to use the proposed technique, collecting the frequency responses of randomly generated fault-free and faulty samples is necessary. Each frequency response is classified into a certain group according to its dynamic characteristics such as signal-to-noise ratio (SNR). These classified results are used to benchmark converters to be tested. If we take every frequency into account for its classification, a large memory is required to store the boundaries of each group. Since this is not practical, splitting the frequency responses by some frequency span is introduced to reduce the required size of memory. The number of bins is determined by the bin order (n) as shown in Fig. 2(b).

$$the\, number\, of\, bins = 2^n \quad (3)$$

The frequency responses in each bin are integrated as Equation 4.

$$Xbin_k^n = \sum_{f=f_k^n}^{f=f_{k-1}^n} Y(f) \quad (4)$$

where f_k is the frequency boundary of the kth bin. The manipulation of near bins($Ybin$) is performed. These $Ybin$s are classified into an ADC or a DAC group according to their frequency.

$$Ybin_{DAC}^n(j) = \sum_{k1=1}^{k1=2^n} (b_{k1}Xbin_{k1}^n + b_{k1+1}Xbin_{k1+1}^n) \quad (5)$$

$$Ybin_{ADC}^n(j) = \sum_{k2=1}^{k2=2^n} (b_{k2}Xbin_{k2}^n + b_{k2+1}Xbin_{k2+1}^n) \quad (6)$$

In order to obtain SNR_{ADC} values corresponding to the ADC group, simulation of a stand-alone ADC is necessary. By performing the mentioned procedures with M samples, the SNR_{ADC} of the ADC group can be expressed as a function of $Ybin_{ADC}$ and classified into one of the groups (IDX_{ADC}) which are bounded by their pre-determined SNR range ΔSNR. The number of $Ybin_{ADC}$ in the group i is defined as L_i for ADC.

$$IDX_{ADC}(i) = \{Ybin_{ADC}^n(1), \ldots, Ybin_{ADC}^n(L_i)\} \quad (7)$$

The range of $Ybin_{ADC}$ (ΔIDX) in a group is determined by the minimum and the maximum $Ybin$ values of the group.

$$\Delta IDX_{ADC}(i) = MAX((IDX_{ADC}(i)) - MIN((IDX_{ADC}(i)) \quad (8)$$

The SNR_{ADC} and $Ybin_{ADC}$ values of a group are averaged and used to build SNR_{ADC} equations as a function of $Ybin_{ADC}$. The equations related to these calculations are as follows.

$$\overline{Ybin_{ADC}(i)} = \frac{\sum_{m=1}^{L_i}(Ybin_{ADC}^n(m))}{L_i} \quad (9)$$

$$\overline{SNR_{ADC}(i)} = \frac{\sum_{m=1}^{L_i} SNR_{ADC}(Ybin_{ADC}^n(m))}{L_i} \quad (10)$$

$$SNR_{ADC}(Ybin_{ADC}(j)) = \frac{\Delta SNR(i)}{\Delta IDX_{ADC}(i)} Ybin_{ADC}(j) + B \quad (11)$$

$$B = (\overline{SNR_{ADC}(i)} - \frac{\Delta SNR(i)}{\Delta IDX_{ADC}(i)} \overline{Ybin_{ADC}(i)}) \quad (12)$$

Then, SNR_{DAC} can be expressed as a function of SNR_{ADC}, SNR_{LB}, and $Ybin_{DAC}$. SNR_{LB} is obtained by simulation of loop-backed converters. Using these values, $Zbin_{DAC}$ is defined as follows.

$$Zbin_{DAC}^n(j) = Ybin_{DAC}^n(j) \frac{SNR_{LB}(j)}{wSNR_{ADC}(j)} \quad (13)$$

where w is a weight constant which is obtained by heuristic experiments. The remaining equations for SNR_{DAC} are the same except that $Ybin_{ADC}$ is replaced by $Zbin_{DAC}$

$$IDX_{DAC}(i) = \{Zbin_{DAC}^n(1), \ldots, Zbin_{DAC}^n(L_i)\} \quad (14)$$

$$\Delta IDX_{DAC}(i) = MAX((IDX_{DAC}(i)) - MIN((IDX_{DAC}(i)) \quad (15)$$

$$\overline{Zbin_{DAC}(i)} = \frac{\sum_{m=1}^{L_i}(Zbin_{DAC}^n(m))}{L_i} \quad (16)$$

$$\overline{SNR_{DAC}(i)} = \frac{\sum_{m=1}^{L_i} SNR_{DAC}(Zbin_{DAC}^n(m))}{L_i} \quad (17)$$

$$SNR_{DAC}(Zbin_{DAC}(j)) = \frac{\Delta SNR(i)}{\Delta IDX_{DAC}(i)} Zbin_{DAC}(j) + B \quad (18)$$

$$B = (\overline{SNR_{DAC}(i)} - \frac{\Delta SNR(i)}{\Delta IDX_{DAC}(i)} \overline{Zbin_{DAC}(i)}) \quad (19)$$

With these equations, the go/no-go test of loop-backed converters is possible. In addition, the SNRs of the DAC and ADC can be extracted.

IV. Model for loop-backed converters

The samples can be obtained by simulation or real measurements. Currently the samples are generated by injecting parametric faults into a Matlab model of the loop-backed system. In fact, the Matlab model with SIMULINK [10] can be simulated exhaustively. In order to obtain good benchmark data, an accurate model is a prerequisite. Considering that an oversampling $\Delta\Sigma$ modulator is typically implemented using switched-capacitors, the model should include the performance parameters of the building blocks and non-idealities, such as sampling jitter, kT/C noise, and operational amplifier parameters[9, 8]. Operational amplifier parameters include noise, finite gain, finite bandwidth, slew-rate, saturation voltage, etc. The characteristics of noise in $\Delta\Sigma$ modulators depends largely on frequency as illustrated in Fig. 3(a). The model can be built using equation-based approaches [9, 8, 12]. The details on the model will be described below.

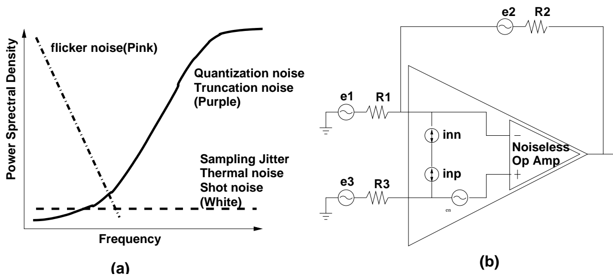

Figure 3. Noises in $\Delta\Sigma$ modulators and Op amp noise model

A. Noise and non-ideality models

The effect of clock jitter on a switch-capacitor $\Delta\Sigma$ modulator by an amount δ is expressed in (20) when a sinusoidal signal with amplitude A and frequency f_{in} is applied [9].

$$x(t+\delta) \sim 2\pi f_{in}\delta\cos(2\pi f_{in}t) = \delta\frac{d}{dt}x(t) \quad (20)$$

Switching noise in a switched-capacitor circuit is associated with thermal noise. There will typically be two switched input capacitors and a switch resistor (R) in the switched-capacitor circuit, such as a sampling capacitor (C_s) and a feedback capacitor (C_f). The noise caused by switching activities, including thermal noise, can be expressed as Equation 21 where $n(t)$ is the Gaussian probability function, k is the Boltzmann constant, and T is the absolute temperature [12]. The noise is superimposed on the input signal $x(t)$ as expressed in Equation 22 [8].

$$e_T(t) = \sqrt{\frac{kT}{C_s}}n(t) \quad (21)$$

$$y(t) = [x(t) + e_T(t)]\frac{C_s}{C_f} \quad (22)$$

Fig. 3(b) shows a typical op-amp circuit for noise analysis. The RMS noise voltage including thermal noise and flicker noise can be expressed as Equation 23 [11].

$$e_{op}(t) = \sqrt{ENB4kTR_2A + e_W^2A^2(f_{enc}ln\frac{f_H}{f_L} + ENB)}n(t) \quad (23)$$

where ENB is the equivalent noise bandwidth, $A = (R_1 + R_2)/R_1$ is the noise gain, e_W is the white voltage noise specification, f_{enc} is the voltage noise corner frequency, and f_H and f_L are the highest and the lowest frequency. Integrator non-idealities such as DC gain, bandwidth, and slew rate can be modeled by using Equation 24. Slew rate is defined as $2\pi f_{max}V_p$, where f_{max} is the maximum sine wave frequency without distortion of the integrator output and V_p is a peak voltage. If the slew rate is greater than the the change of the integrator output to a sampling period T, the output of the integrator is expressed as Equation 24.

$$v(kT+t) = H_0\frac{V_{in}(kT)}{1-e^{-T/\tau}}(1-e^{t/\tau}) + v(kT) \quad (24)$$

where $H_0 = \frac{1}{1-\alpha}$ is the DC gain, α is the integrator leakage, $\tau = \frac{1}{2\pi f_u}$ is the time constant of the integrator, and f_u is the unit gain frequency. The effect of output distortion caused by slewing can be estimated though circuit simulation, and be added to Equation 24. A saturation effect in the integrator can be modeled by inserting its model inside the feedback loop of the integrator.

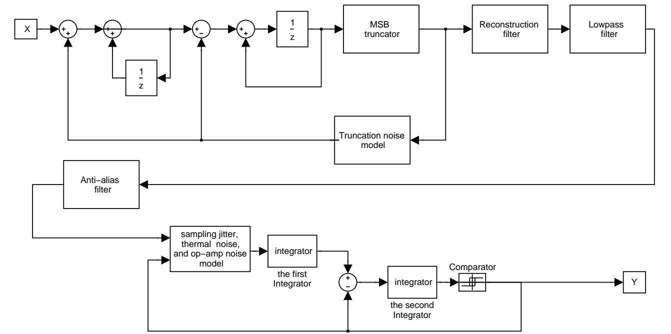

Figure 4. The Matlab model of loop-backed $\Delta\Sigma$ modulators

B. Model for loop-backed $\Delta\Sigma$ modulators

Noise and non-ideal behavior can be modeled in Matlab as shown in Fig. 5 [8]. In this sub-section, it will be explained about the block diagram of the loop-backed converter, which is modeled from the digital $\Delta\Sigma$ modulator to the analog $\Delta\Sigma$ modulator. Both modulators are 2nd order. The input signals X from the linear interpolater are summed with the feedback

signal from the truncater of the digital $\Delta\Sigma$ modulator. These signals go through the noise shaping loop, are filtered by a reconstruction filter which eliminates the truncation noise of the modulator, and smoothed by a continuous-time low pass filter. The nonlinearities caused by slewing or signal-correlated settling in a reconstruction filter can be modeled by using the values from circuit simulation. This model can be inserted between the reconstruction filter and the continuous-time low pass filter. The filtered signal is further filtered by the other low pass filter, and the re-filtered signal is the input signal to the analog $\Delta\Sigma$ modulator. This input signal and the comparator output, that is, from the 1-bit DAC, are convolved with the clock jitter and superimposed with the switching noise. For a 2nd order analog $\Delta\Sigma$ modulator, only the first integrator is modeled with the non-idealities since the distortion is mainly caused by the first integrator. The errors introduced by the second integrator are attenuated by the noise shaping loop. Fig. 4 shows the overall model including the noise models in $\Delta\Sigma$ modulators.

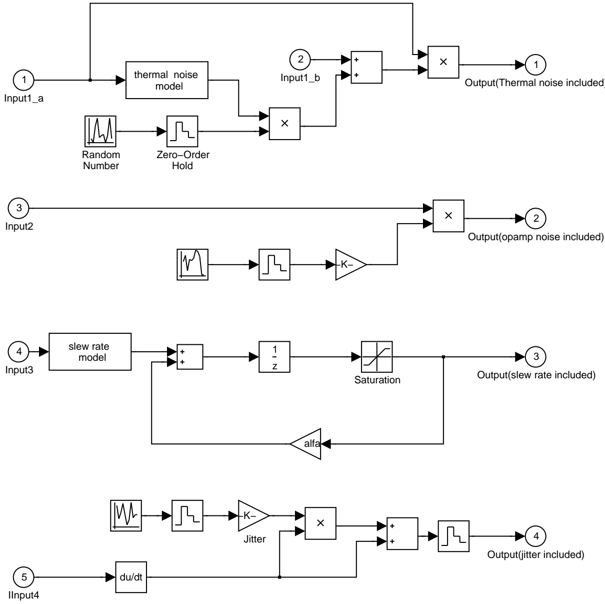

Figure 5. The Matlab model of noises in $\Delta\Sigma$ modulators

V. Simulation Results

The loop-backed converters with 2nd order $\Delta\Sigma$ modulators are modeled, which is explained in the previous section, and simulated using Matlab with SIMULINK. The modeled $\Delta\Sigma$ converters have audio bandwidths (BW=20 – 20kHz) and their oversampling ratio (OSR) is 256. The sampling frequency (f_s) is 11,264 kHz, which can be calculated by $2 \cdot BW \cdot OSR$. A 2kHz single-tone sine wave digitized to 16-bit codes is used as an input stimulus to the digital $\Delta\Sigma$ modulator. 2nd order frequency binning is used to extract ADC/DAC dynamic characteristics from the power spectral density calculated by performing an FFT on the frequency responses of loop-backed converters. Fault-free and faulty samples are generated by injecting parametric faults into the model. The extraction of equation parameters starts with $Xbin$ from power spectral density of frequency responses as shown in Fig. 6. $Xbin$ is calculated from the power spectral density data as shown in Fig. 7. $Ybin_{ADC}$ is obtained by Equation 6 based on the calculated $Xbin$. If 2nd order frequency binning is applied to the $Ybin$ calculation, 4 $Xbin$s are required. Fig. 8 (a) shows the SNR value distribution according to $Ybin_{ADC}$. The SNR_{ADC} distribution characteristic to $Ybin_{ADC}$ shows piecewise linearity. In order to express SNR_{ADC} as a function of $Ybin_{ADC}$, a pre-determined SNR range, ΔSNR, is set to 5 dB. This ΔSNR determines the $Ybin_{ADC}$ boundary of the groups (IDXs).

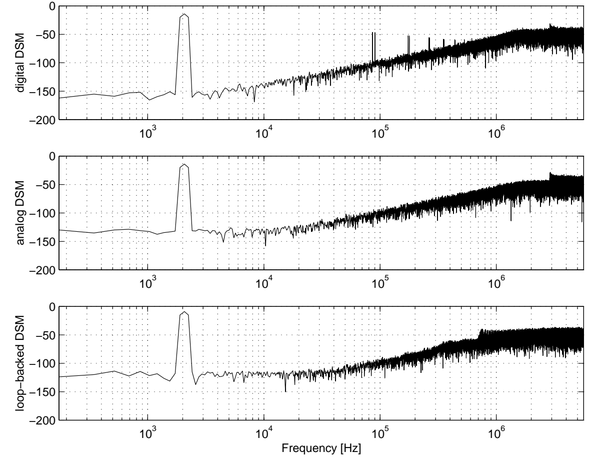

Figure 6. PSD of a digital DSM, analog DSM and a loop-backed DSM

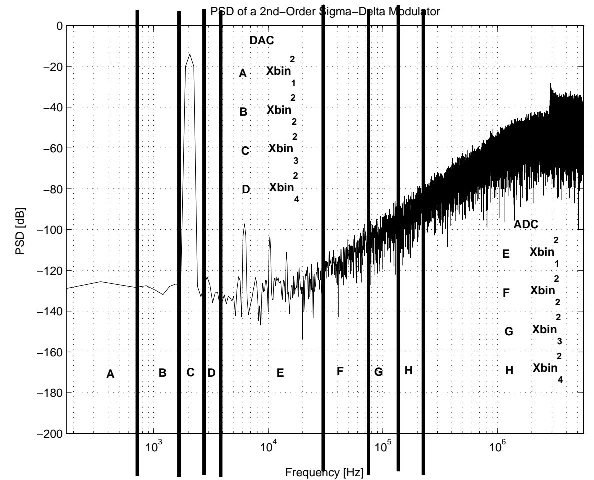

Figure 7. $Xbin$ and $Ybin$ extraction

With this extracted data, the parameters of the SNR_{ADC} equation parameters in Equation 11 are obtained. Through similar procedures, the SNR_{DAC} value distribution according

to $Zbin$, which is expressed in terms of SNR_{ADC}, SNR_{LB}, and $Ybin_{DAC}$, is obtained as shown in Fig. 8(b). The SNR_{DAC} distribution characteristic to $Zbin_{DAC}$ also shows piecewise linearity. With the same ΔSNR, SNR_{DAC} can be expressed as a function of $Zbin$. The SNR_{DAC} equation parameters in Equation 18 are obtained through a similar procedure to that for the ADC. Fig. 9(a) and (b) show comparisons between SNR from the extracted equations and from the simulation. As expected, there is some deviation between the two values. If we set the maximum acceptable value of deviation in Fig. 9 (c,d) to 25, which is a ΔSNR range, 5 dB, all ADC samples are within the range. However, 24% of DAC samples are out of range. As shown in Fig. 9 (c,d), deviation of SNR_{DAC} is worse than SNR_{ADC}. This results from the fact that the calculation of SNR_{DAC} depends on the SNR_{ADC} which already has some errors. In fact, the accuracy of the proposed method depends on the number of samples, binning order, and ΔSNR. If the number of samples is larger, binning order is higher, or ΔSNR is smaller, then the test is more accurate.

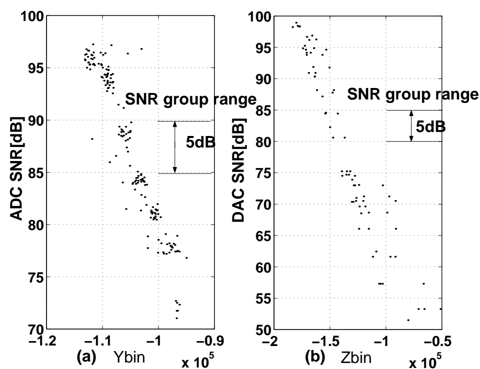

Figure 8. ADC SNR as a function of $Ybin_{ADC}$ and DAC SNR as a function of $Zbin$

VI. Conclusions

We presented a simple and efficient approach to testing on-chip ADCs and DACs. This approach exploits loop-back tests and uses the existing digital processing units to generate input stimuli. The proposed method extracts DAC and DAC performance characteristics from the overall frequency responses of the loop-backed converters and provides go/no-go tests and dynamic characterization. Results of detailed simulations show that the SNR values calculated from the extracted equations have errors 1 – 3dB (about 1 bit in resolution). We plan to extend this approach to testing other types of converters.

Acknowledgements

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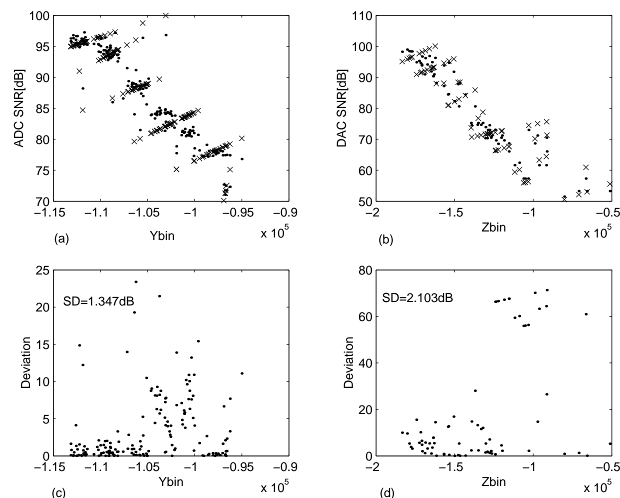

Figure 9. SNR (calculated) vs. SNR (simulated) and the SNR deviation in converter characteristic extraction

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