Standard Cell Libraries with Various Driving Strength Cells for 0.13, 0.18 and 0.35 μm Technologies

Masanori Hashimoto Kazunori Fujimori Hidetoshi Onodera
Dept. Communications and Computer Engineering, Kyoto University

Abstract— We developed standard cell libraries for three technologies(0.13, 0.18 and 0.35μm) using an automatic layout generation tool that we have developed. The developed libraries are as competitive as manually-designed libraries in layout density and speed. We verify the functionalities of all cells and the speed of basic combinational cells on the fabricated chips. The libraries are currently public to educational organizations in Japan.

I. Introduction

In current SoC/ASIC designs, cell-base design methodology is widely used. High-quality cell libraries are crucial for designing high-performance circuits. Recently cell-base design with various driving strength cells is discussed and it is found that a rich library in driving strength improves circuit performance close to transistor-level optimized circuits[1, 2, 3]. We develop cell libraries including a plenty of driving strength variation for 0.13, 0.18 and 0.35μm technologies. We provide two libraries whose cell heights are different in 0.13 and 0.35μm processes: one is for high-speed design and the other is for low-power design. The functionalities of there libraries are verified by the measurement of the fabricated chips.

II. Layout Generation

We have developed a cell layout generation system, which is called VARDS, and use it for library generation[1]. VARDS generates cell layouts from grid-base symbolic layouts managing design rules. The features of VARDS are:

1. process-portable layout generation
2. to generate various driving-strength cells easily (cell height, transistor sizes inside a cell)
3. to generate phase shift mask
4. to cope with a process whose Tr. and wire pitches are different.

The third and fourth features are mainly developed and implemented to generate 0.13 and 0.18μm cell libraries.

III. Library Specification and Performance

Table I lists the cell varieties of our libraries in logical function and driving strength. The number of cells in each 0.18 and 0.35 μm library set is 310. The organization of each library in logical function and driving strength is the same. For 0.13μm process, we generate only basic cells, and the number of cells is 38. The principal features of our libraries are:

- The driving strength range is wide from x0.5 to x16 and it advances the flexibility to various, load conditions, i.e. very small load to huge #fanout load, which is essential and indispensable requirement for high-performance circuits, especially in DSM technologies[3].
- Small driving cells(x0.5) is so effective to reduce power dissipation[2]. Small increase step in driving strength enables fine tuning in delay and power optimization.
- Two types of high-driving strength cells are prepared: one is composed by parallel cells and suitable for high-speed design. The other is constructed in the serially-connected structure with a tapering ratio and it is desirable to compact and low-power design.

TABLE I
Variation in Functionality and Driving-Strength

Functionality	Driving-Strength
INV, BUF	005, 010, 015, 020, 030, 040, 050, 060, 080, 120, 160
NAND2, NAND3, NOR2, NOR3, AOI21 AOI22, AOI211, OAI21, OAI22, OAI211	005, 010, 015, 020, 030, 030S, 040, 040S, 060, 060S, 080, 080S
NAND4, NOR4	005, 010, 015, 020, 030, 040, 040S, 060, 060S, 080, 080S
AND2, AND3, OR2, OR3	005, 010, 015, 020, 030, 040, 040S, 060, 080, 080S
AND4, OR4	005, 010, 015, 020, 030, 040, 040S, 060, 080
XOR2, XNOR2	005, 010, 020, 030, 040, 060, 080
HAD1, FAD1, MUX2, TINV, TBUF	010, 020, 030, 040, 060, 080
DF, DFR, DFSR, DFN, DFNR, DFNSR	010, 020, 040, 060, 080, 120, 160

"010" represents the standard driving strength. The cells labeled "S" are composed by parallel connection.

The cell height and PMOS/NMOS ratio, which are the basic specification of standard cell libraries, are shown in Table II. We develop high-speed and low-power libraries for 0.13 and 0.35μm processes whose cell heights are different. The cell height of the high-performance(HP) library is fourteen interconnect pitches and that of the low-power(LP) library is nine interconnect pitches.

We show the basic performance of the developed 0.35μm libraries in Table III. To make a comparison, Table III also lists the performance of the library generated by a commercial module generator(MG Lib.) and that of the commercial library special to its process (Fab Lib.). The information of Fab Lib. is restricted, then the only parameters we know are listed. Our layout generation tool VARDS can cope with the difference between wiring and transistor pitches, and hence the

TABLE II
Basic Specification of Cell Libraries

	0.35(HP)	0.35(LP)	0.18	0.13(HP)	0.13(LP)
Cell Height(int. pitch)	14	9	12	14	9
PN Ratio(PMOS/NMOS)	1.23	1.00	1.33	1.23	1.00

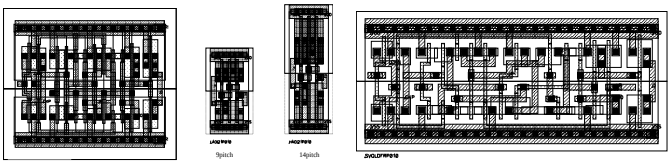

Fig. 1. Examples of Cell Layouts. From the left, DFP010 in 0.18μm process, AOI21P010 with different cell heights in 0.35μm process, and DFRP010 in 0.13μm process.

interconnect pitches of the developed libraries is the same with Fab Lib.. Also the area of D flip-flop with reset is the same with that of Fab Lib., which reveals that the layout density of our library is so competitive. Table III also shows the delay difference between HP and LP libraries. The difference in the case of FO1 comes from PMOS/NMOS ratio, and the delay difference in the case of 200μm-length interconnect load reveals that HP library is effective to reduce delay in large-scale high-speed designs.

To demonstrate performance difference between HP and LP libraries, we design a 32-bit RISC processor core using the 0.35μm libraries. The design constraints are 100MHz and 130MHz, and we compare delay, circuit area, and the sum of transistor widths, where the sum of transistor widths directly corresponds to power consumption. The circuit is designed by a commercial logic synthesis tool and a P&R tool. After P&R, we tune driving strength of each instance according to the P&R results. The results are shown in Table IV. In the case of 100MHz design, our library reduces area by 6% and total transistor width(power dissipation) by 25%. HP library realizes 130MHz design, although LP and MG Libs. can not satisfy design constraints.

IV. Verification

We design TEG circuits to verify our libraries for every process. The chip micro-graphs are shown in Fig. 2. The TEG circuits consist of two groups: one is to verify logical function, and the other is to evaluate cell delay. The TEG chip of 0.13μm process aims only to evaluate cell delay. We first explain TEG for logical verification. We construct chains that consist of serially-connected combinational cells and check whether signal transition propagates through the chain, where the input pins except the pin we want to examine are fixed to high or low such that the signal transition will occur. The designed circuit covers all combinational cells and its all input-output combinations. Flip-flops(DFP040, DFRP040, DFSRP040, DFNP040, DFNRP040, DFNSRP040) are examined solely, i.e. all input signals are given independently and observe their outputs. We build dividers using the rest of FFs and check the divider behavior. Tri-state buffers and inverters are tested whether enable inputs allow/stop signal propagation. As for cell delay evaluation, we construct ring oscillators using basic combinational cells and evaluate those oscillation frequency.

TABLE III
Performance Comparison(0.35μm technology)

	HP Lib.	LP Lib.	MG Lib.	Fab Lib.
Cell height	1.56	1	1.31	1
Int. pitch	1	1	1.07	1
Tr. width(NMOS)	1.82	1	1.31	-
DFR Area	1.56	1		1
INV delay (FO1)	0.91	1	0.99	-
(FO1, int. 200μm)	0.77	1	0.91	-

TABLE IV
Design Results of RISC Processor Core

Constraint	Metric	HP Lib.	LP Lib.	MG Lib.
100MHz	Area(mm^2)	1.62	1.11	1.18
	Tr. width(mm)	393.4	212.8	284.2
130MHz	Area(mm^2)	1.74	impossible	impossible
	Tr. width(mm)	424.5	-	-

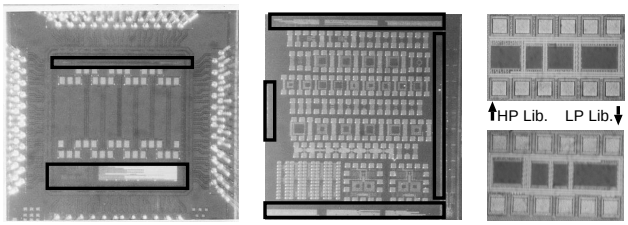

Fig. 2. Chip Micro-graphs. From the left 0.18μm chip (2.8mm square), 0.35μm chip (4.8mm square), and two blocks in 0.13μm chip ($360\times230\mu$m^2).

The library TEG chips of 0.18μm and 0.35μm processes are measured by HP83000 LSI tester. We confirm that all combinational cells and FFs work correctly. We also observe that cell delay of basic combinational cells is within process variation range that is announced from Fabs.. The chip of 0.13μm technology is measured using a probe card with twelve needles. We confirm that the measured cell delay and power dissipation are close to the simulation results.

V. Conclusion

We develop standard cell libraries that are rich in driving strength for 0.13, 0.18 and 0.35μm technologies. We verify from the measurement results that all cells in three libraries work correctly. Now the developed libraries are open to universities in Japan and several chips designed with our libraries are already taped out.

Acknowledge

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