

# DESIGN OF A DIGITAL CDMA RECEIVER

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**Abstract-**In this work, an attempt has been made to design a Digital Signal Code Division Multiple Access Receiver using VHDL [1] [2] and synthesize using Mentor Graphics tools. The receiver is designed for a maximum of three users as per the design specification given for the contest. The novelty of this design is that it uses four independent processes to achieve the concurrent operation for the entire functionality. The simulation and synthesis are carried out using Mentor Graphics' FPGA tools and an optimized circuit in terms of area and timing is brought out.

## 1. INTRODUCTION

The enhancement in performance obtained from a DS-Spread-Spectrum signal through the processing gain, and the coding gain can be used to enable many DS spread spectrum signals to occupy the same channel bandwidth provided that each signal has its own pseudorandom (signature) sequence. Thus, it is possible to have several users transmit messages simultaneously over the same channel bandwidth. This type of digital communication in which transmission/reception has its own distinct signature code for transmitting over a common channel is called CDMA. A receiver, which uses CDMA technology as per the specifications, is designed using VHDL and results are obtained for the simulation and logic synthesis.

## 2. SYSTEM FUNCTIONALITY

The system uses the data (signals) sent by the transmitter, whose characteristics are already known. The transmitter receives 3 digit inputs and mixes them to generate one output using CDMA technique. The receiver receives the mixture and decodes the signal and extracts one preferable datum. A perfect synchronization clock for both the transmitter and the receiver is assumed. CDMA does the data extraction using Pseudo Noise code (PN code), which is a sequence of randomly appearing ones and zeros, but the appearing frequency of both ones and zeros are almost the same. The PN code of 127 bits is used for the inner product calculation, which is also called "convolution" or "matched filtering".

## 3. RECEIVER DESIGN

The receiver design is divided into four different modules, viz., the PN code generation module, counter module, synchronous signal generation module and receiver output module, as shown in Fig. 1, and are designed using process statements. A synchronous clock is applied to all the modules while the RESET signal initializes all the values. A brief explanation of various modules is given below.

*The PN code generation Module (Process):* - The PN codes are generated in this module using the linear shift back registers. These codes are generated on the raising clock edge and on receiving the SYNCIN signal, which is activated by the SYNCOUT signal of the transmitter. After a period of 127 clock cycles, the process waits for the next SYNCIN signal for the PN code regeneration. Thus it keeps in synchronous with the transmitter data. If the design requires a change in PN code, a different design can be modeled for the PN generation without effecting the other processor blocks, a consequence of using independent processes.

*Counter Module:* - The Counter module (Process) starts the counter with the start of SYNCIN signal and for further regeneration it depends upon the next SYNCIN signal thus keeping track of the input signals.

*Synchronous Signal Generation Module:* - This module keeps track of the SYNCIN signal (SYNCOUT signal from the transmitter) and gives stimuli for all other modules for functioning for a period of 127 cycles after which all other processes wait for the next stimuli. This process is independent in nature.

*Receiver Output Module:* -The function of this Module (process) is to process on the RVIN data upon receiving stimuli from the Sync signal. The PN code is convolved with the received data and after a period of 127 cycles the output (DOUT) is assigned a value according to the channel output requirement and the VALID signal is made high. The processing of the data is done for the three channels and one of the values is assigned according to the channel selection. If the number of users is increased, then new PN code

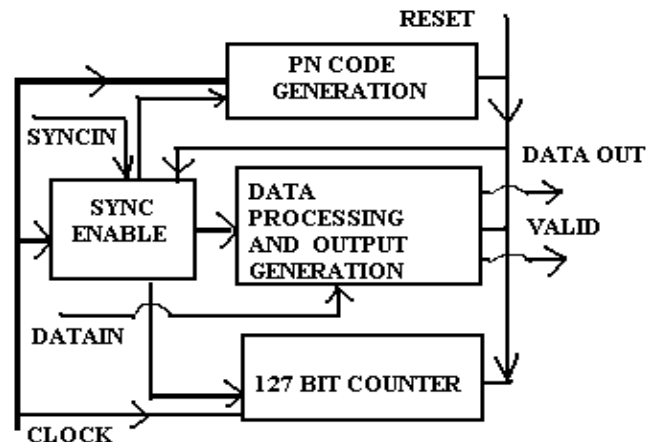


Fig-1 System Architecture

generators can be introduced and respective channel processing for the channel data can be achieved easily with small changes in code. Here the novelty lies in the ease with which new channels can be added.

The technique used in the present design is simple. The entire design is divided into four different process statements and each is run concurrently thus making four different modules work in tandem. The Simulation was carried out using ModelSim simulator (Mentor Tools). Accuracy of the results was verified by applying data out of the transmitter to the receiver. Figure 2 and Fig-3 show the start and end of the simulation for the transmitter's input of (data-in) '000'. The valid signal is high after 127 clock cycles and the data-out is 0, thus verifying the design. The synthesized RTL and technology schematics are shown in the Fig-4 and Fig-5 respectively.

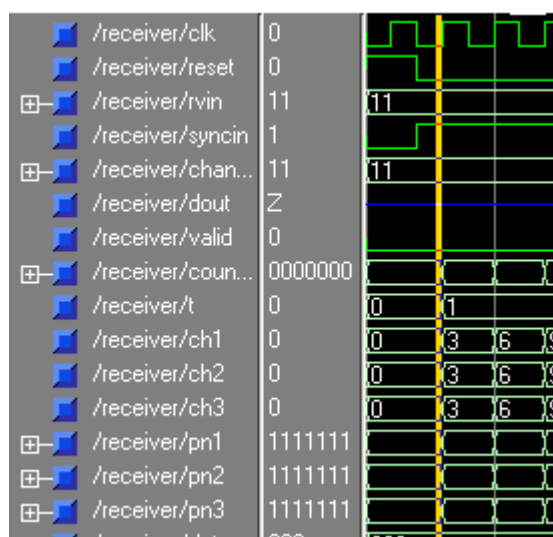


Fig-2 Simulation start point

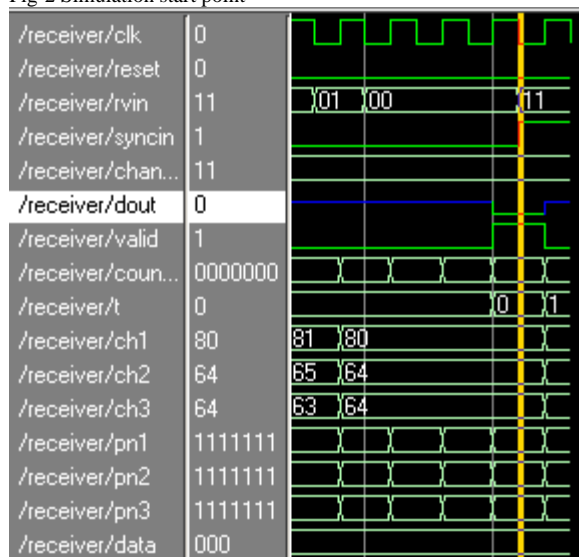


Fig-3 Simulation end point

### 8. SYNTHESIS

Vdd = 2.5 V, Maximum clock frequency = 77.2 MHz  
 DYNAMIC POWER CONSUMTION =1.35W (approximately)

\*\*\*\*\*  
 Device Utilization for 2s15cs144 (XILINX -SPARTAN2)  
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Resource	Used	Avail	Utilization
IOs	9	86	10.47%
Function Generators	291	384	75.78%
CLB Slices	146	192	76.04%
Dffs or Latches	128	672	19.05%

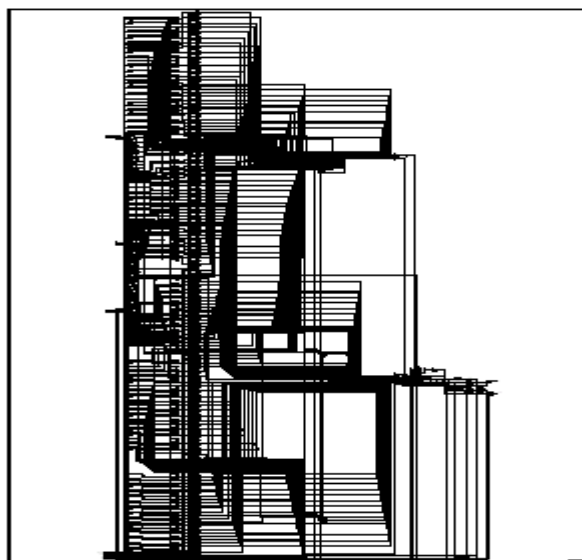


Fig-4 RTL Schematic

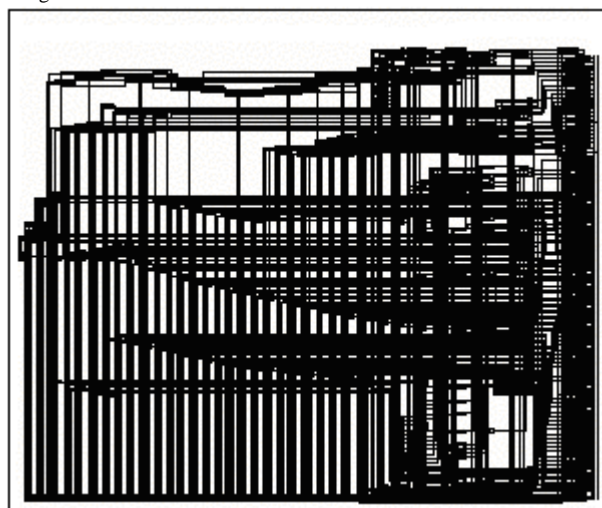


Fig-5 Technology Schematic

### 9. RESULTS AND CONCLUSIONS

The results, as shown in Figs. 2 and 3, show that the design meets the specifications given. The design has been implemented on Xilinx's Spartan-2 series FPGA with good utilization as indicated by the results. The dynamic power consumption has been estimated to be 1.35 W.

### 10. REFERENCES

- [1] Perry – 'Digital Design using VHDL'
- [2] Heinkel : 'VHDL Reference'