

Low-Power Digital CDMA Receiver

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Abstract -The advanced design task of the digital CDMA receiver are presented in this report. A biased number system and architecture is used to reduce the switching activity to reduce power consumption. Carry-save adder tree is used to speed up the summation of 127 data (3 bits) in the synchronization and data extraction process. Verilog HDL is used to describe this system and design compiler of Synopsys is used to synthesize our design. Design results show that it can work at 155MHz (Chip rate) with 9913 Gate counts by using Compass 0.35 um CMOS Cell library.

I Introduction

Fig.1 shows an CDMA communication system. It consists of Transmitter and Receiver. The task of this design is to design the Receiver. The transmitter receives data from three channels, and then it mixes the 3 data to generate one output. The CDMA Receiver receives the transmitted data from Transmitter and then it decodes the signal and extracts one preferable datum. In this system, it was assumed that a perfect synchronized CLOCK is used for both the transmitter and the receiver.

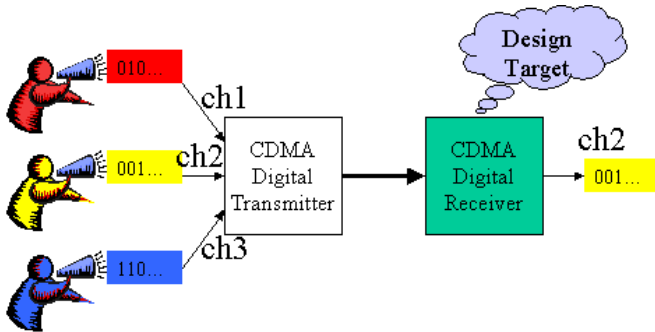


Fig.1 The design target of the digital CDMA system.

Fig.2 shows the block diagram of this system. The functions of the Transmitter are provided by the design committee (only VHDL version). According to the function, we rewrite the function by using Verilog HDL. The transmitter includes 3 kinds of PN code generators (for channel 1, 2 and 3), 3 kinds of sending data generator, and 3 EXOR gates for each transmitting channel. Each PN generator output is exclusive Ored with the corresponding sending datum, and then those signals are summed up to generate 2 bits width TXOUT output signal. The TXOUT signal is generated synchronizing with the CLOCK rising edge. Since the length of the PN code is 127, it takes 127 cycle to send 1 bit datum on each channel. In the standard design task, in order to indicate the timing of the PN code starting point, the synchronizing signal SYNCOUT is asserted. In this

advanced design task, there is no such SYNCOUT/SYNCIN signal between Transmitter and Receiver. Thus, the receiver shall have a mechanism to find out the starting point of PN sequence.

The receiver gets the 2 bits input RVIN from the transmitter's TXOUT. Since the signal RVIN is composed by the mixture of CH1, CH2, and CH3 sending data, preferred channel data has to be extracted from the RVIN signal according to the 2 bits width CHANNEL inputs (00: don't care; 01: CH1; 10: CH2, and 11: CH3). Then the extracted data will be the output of the DOUT pin. After knowing the starting point of the PN code, 127 data are received and the inner product calculation with the PN code, which is generated in the receiver according to the CHANNEL input, is calculated. If the result of the inner product is a large positive value, the sending datum is identified as '0' and if it is a large negative value, the sending datum is identified as '1'.

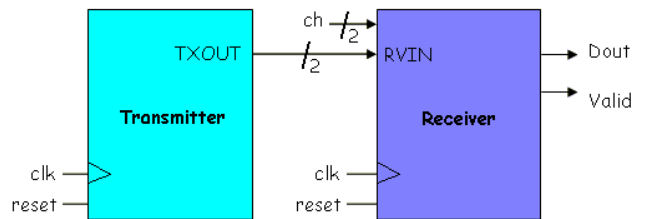


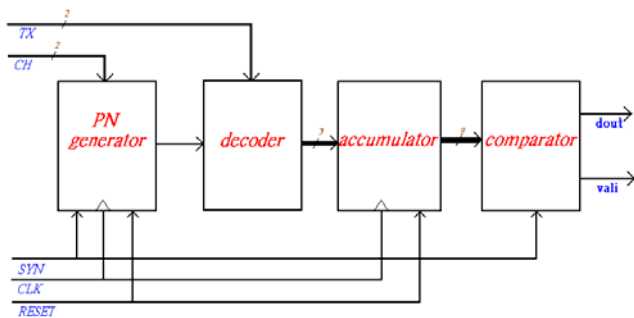
Fig.2 The block diagram of the advanced design task.

II. Architecture Design

We have designed two versions of the CDMA receiver. One (CDMAI) is with SYNCOUT/SYNCIN signal (Syn) between Transmitter and Receiver (standard version of the design task). Fig.3 shows the circuit diagram of the CDMAI. The circuit design of the PN code generator is shown in Fig.4. The decoder does the correlation between input data and PN code. The correlated outputs are sent to the accumulator (127 times) to do the inner products. Then the outputs are compared with predetermined value (40 and -40) to extract the data. Due to the Syn signal provided by the transmitter, this design is rather simple.

The second version of the CDMA receiver (CDMAII) is the one without SYNCOUT/SYNCIN signal. Fig.5 shows the circuit diagram of a pipelined version of CDMAII. To find out the starting point of PN code sequence, in the beginning of the transmission, we need to compare the incoming signal in every chip time. To speed up the summation of the 127 data of 3 bits, we use carry-save adder (CSA) tree to process

the summation in parallel. A Carry propagation adder (CPA) is used to get the final results. Then the results are compared with two predetermined values to extra the data. In two's complement number system, when the number is changed from positive number to negative number (or vice versa), the switching activity of the data is very high. This is due to the change of MSB bits from all 0s to all 1s. In the correlation operation, if the PN code or synchronization is not matched, the results are usually bouncing around zero. To reduce the switching activity in two's complement system, we use the biased number system that is, we add a +3 to the data in the decoder so that the range of the data is changed from (-3, +3) to (0, 6). Thus, all the results are positive number and the switching activity is reduced. Also, in our design, gated clock is used so that after synchronization, many part of the receiver is working at date rate (fs) not the chip rate (127*fs). The PN codes of the three channels are stored in a ROM so that the code can be dumped in parallel. CDMAII-1 is the version without pipelining. CDMAII-2 is the version that we put pipelining registers before comparator to reduce glitches and enhance speed and CDMAII-3 is the version shown in Fig.5. It has four pipelined stages so the clock rate can be over 155 MHz.



CDMA I architecture

Fig. 3 The circuit diagram of the CDMAI

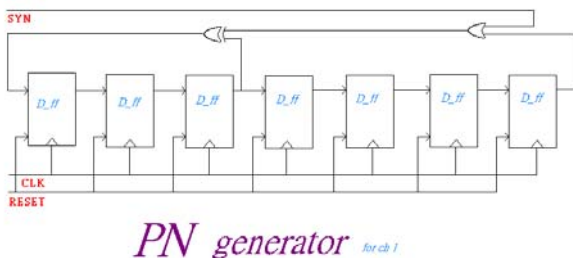


Fig.4 127 length PN code generators.

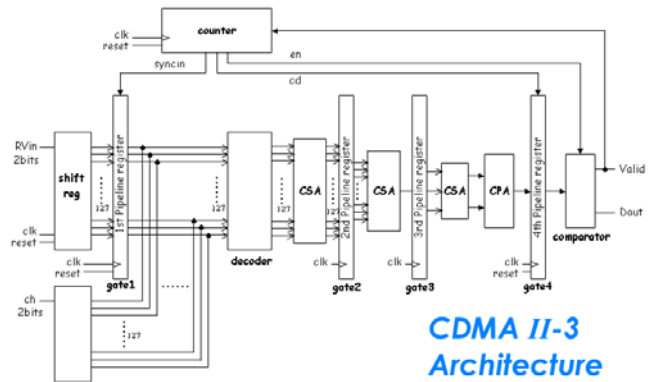


Fig.5 The circuit diagram of CDMAII-3

III. Implementation Results

Verilog HDL is used to describe this system and design compiler of Synopsys is used to synthesize our design by using Compass 0.35 um CMOS Cell library. Design results are summarized in Table 1. For CDMAI, it only use 508.95 gate counts and can work at 333.3 MHz (chip rate, delay time is 2.01 ns). For CDMAII-3, it use 9913 gate counts and can work at 155 MHz (Chip rate).The design is also ported to Xilinx FPGA. The simulation results after synthesis is shown in Fig.6. The simulation results are correct for all the test bench.

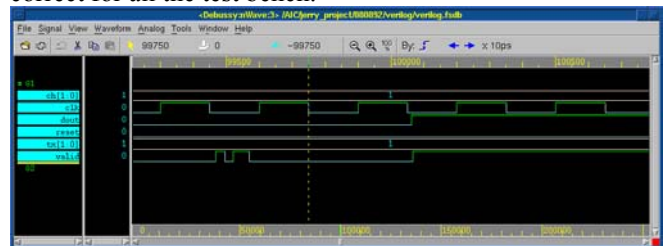


Fig.6(a) Simulation results of the CDMAI system.

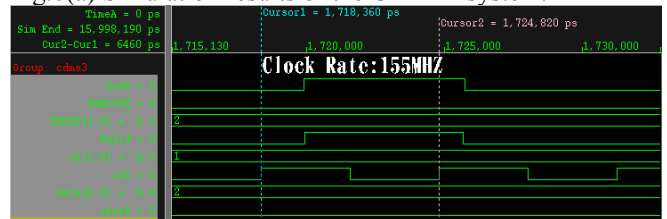


Fig.6(b) Simulation results of the CDMAII-3system.

Table 1 Design summary

System	Gatecount	Clock(MHz)	Power(mW)	Normalized
CDMAI	508.95	333.3	24.11	4.26
CDMAII-1	12044	75.76	110.90	23.16
CDMAII-2	9613	100.00	70.57	17.54
CDMAII-3	9913	155.00	72.95	11.31
2-XOR	N/A	※1754.38	N/A	1

※We take the reciprocal of the delay time of the XOR gate.