

# Floorplanning with Power Supply Noise Avoidance \*

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**Abstract—** With today's advanced integrated circuits (ICs) manufacturing technology in deep submicron (DSM) environment, we can integrate entire electronic systems on a single chip (SoC). However, without careful power supply planning in layout, the design of chips will suffer from mostly signal integrity problems including IR-drop,  $\Delta I$  noise, and IC reliability. Post-route methodologies in solving signal integrity problem have been applied but they will cause a long turn-around time, which adds costly delays to time-to-market. In this paper, we study the problem of power supply noise avoidance as early as in floorplanning stage. We show that the noise avoidance in power supply planning problem can be formulated as a constrained maximum flow problem and present an efficient yet effective heuristic to handle the problem. Experimental results are encouraging. With slight increase of total wirelength, we achieve almost no IR-drop requirement violation and 46.6% of improvement on  $\Delta I$  noise constraint violation compared with a previous approach.

## I. INTRODUCTION

With the advent of further technology scaling, circuits which contain more functionality are operating at higher frequencies, currents, and power. The lower supply voltage brings down the power dissipation in general, but at the same time brings down noise margin of the devices as well. As a result, many effects that were less important in the previous technology of designs have become major factors in correct functionality and performance of these dense chips. In today's new interconnect-centric paradigm [9, 7], power delivery and dissipation, timing, signal integrity, and reliability have become as important, or more important, as die area, which was a prime concern for previous technologies.

During manufacturing, the number of silicon failures are caused by signal integrity problems, such as IR-drop,  $\Delta I$  noise, and electromigration. IR-drop and  $\Delta I$  noise may cause circuits' incorrect functioning and timing requirements mismatch, while electromigration may cause the damage of circuits' lifetime. These problems are on the rise due to the lack of existing design tools and methodologies to address these issues effectively. Therefore, as [14] pointed out, the ability to design the chip, the package, and the surrounding system concurrently becomes a primary advantage. A packaging technique utilizing flip chip bonding (Controlled Collapsible Chip Connection, C4) has been developed from IBM for decades to manufacture VLSI quickly and cost effectively [12, 8]. Nowadays C4/flip-chip technology is more widely used in microprocessor and high-performance ASIC manufacturing than wire-bonded technology. Even the technology minimizes on-chip voltage fluctuations, difficulty still lies in the interaction of two independent functional blocks that share a power source [11].

Post-floorplanning or post-route power supply synthesis have been applied to generate satisfactory power supply, trying to meet the requirements of different components in SoC design. Due to reduced power supply voltage, tighter noise margin and DC voltage drop, the task has been difficult. Among the approaches of handling/estimating power delivery [15], the planning of mesh power rail followed by hierarchical power/ground (P/G) networks designs is still a major method to design high performance IC [6, 3, 18]. Nevertheless, as [13] pointed out, power supply synthesis after floorplanning or routing stage cannot guarantee high-quality power supply under limited routing resources. In many cases, when the circuit block locations and sizes are fixed, the constraints such as voltage drop and current density are so tight that there is no feasible power network design capable of keeping power supply noise within a specified margin. There

has been a large amount of research in floorplanning and extended interconnect-driven floorplanning works. However, most of these approaches ignored power supply planning. The resultant floorplans may suffer from serious local hot spots and insufficient power supply in some regions. Liu *et al.*[13] integrated power supply planning and floorplanning but failed in the attention of possible power supply noise hazard in floorplanning stage.

High-performance ICs require a robust power delivery network with nominal supply voltage fluctuations. We formulate the noise avoidance in power supply planning problem as a supply-demand problem for power delivery with side constraint for power supply noise requirement. We use a constrained network flow model to represent this problem and handle it with a modified max-flow algorithm. We have incorporated our algorithm into a floorplanning algorithm for integrated floorplanning and power supply planning. (This design can be applied to any floorplanner as well.) Experimental results are encouraging. Comparing with a traditional floorplanner with no power supply planning at all [17] and a floorplanner with power delivery planning for avoiding hot spots [13], we obtain floorplans in a fixed die area but significantly better in terms of meeting the IR-drop requirements and minimizing the violations of  $\Delta I$  noise constraint imposed by the circuit blocks. This design can augment the P/G distribution network design and can be an alternative solution other than decoupling capacitance (decap) allocation [19] in power supply noise avoidance.

The rest of the paper is organized as follows. Section II describes the floorplan design with power supply noise considerations and problem definition. The network model and algorithm for power supply noise avoidance are presented in Section III. Section IV shows our approach for floorplanning with power supply noise avoidance. Experimental results and concluding remarks are stated in Section V.

## II. FLOORPLANS WITH POWER SUPPLY NOISE CONSIDERATIONS

In traditional VLSI design, as [8, 4] pointed out for power supply noise analysis, the resistive IR drop occurs mostly on the chip and the inductive  $\Delta I$  noise only occurs on the package. IR drop is an effect caused by wire resistance and current drawn off of the P/G grids. However, as we move into DSM design, the inductive component of wire impedance  $j\omega L$  becomes comparable to  $R$ . The  $\Delta I$  noise, also referred to as simultaneous switching noise (SSN) or ground bounce, is caused by changes in current through various parasitic inductors. C4 has been developed to manufacture VLSI quickly and cost effectively [12, 8]. The major advantage of the technology is, after packaging, that the uniform- and low- inductive/resistive power is fed across the face of the die, minimizing on-chip voltage fluctuations that lead to improved voltage tolerances, resulting in improved on-chip frequencies. Nevertheless, the technology still suffers the problem of power delivery in mainly two effects mentioned above.

The primary difficulties occurred in DC and inductive induced voltage drop during planning power supply in layout design [11]. Firstly, components in an IC share a common power source that supplies voltage and current to transistors. The transistors draw current when they turn on and off. The power source must be designed such that "clean" voltage and current supplies are uniformly available to all transistors. IR-drop can have a significant impact on a design. Secondly, the interaction of two independent functional blocks that share a power source causes inductive induced voltage drop problem. Illustrated in Fig. 1(b), the voltage fluctuation of block C and its subsequent load on the power bus affect the power supply voltage seen by block D and vice versa. If block D experiences a reduced supply voltage, it exhibits a higher than normal delay and might not function properly. So obviously the positions of blocks are important variables in noise avoidance, meaning floorplanning will affect the quality of power de-

\*This work was partially supported by the National Science Foundation under grant CCR-0244236.

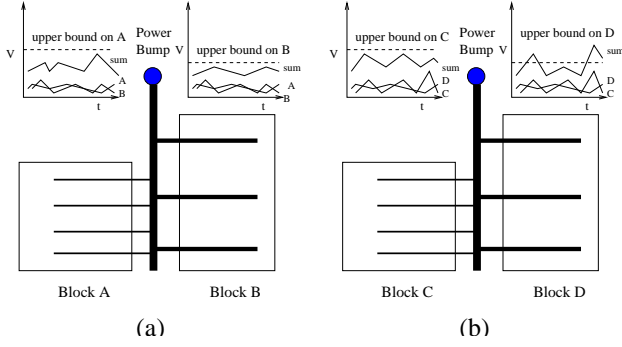


Fig. 1.  $\Delta I$  noise constraint illustration when sharing power sources. Two examples of two blocks with a power supply bump. The V-t curves are voltage fluctuations for blocks and the superposition seen in power supply bump. (a) The power supply bump is clean since the voltage fluctuations of two blocks are within the upper bound on  $\Delta V$  for both blocks. (b) The power supply bump is noisy since the voltage fluctuations of block C and D exceeds the upper bound on  $\Delta V$  for block D.

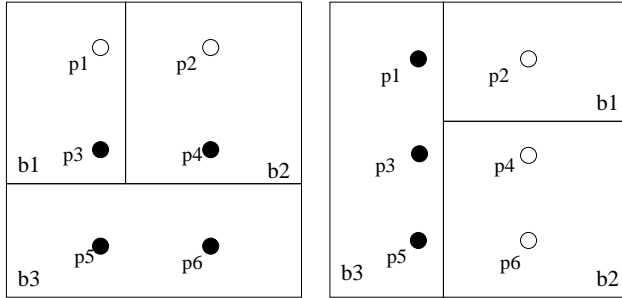


Fig. 2. Floorplanning affects power supply planning and noise avoidance.

livery. In Fig. 2, there are two floorplans with the same area but different relative position of blocks in area-array design. Block  $b_3$  can get four power supply bumps to deliver power on the left floorplan while it can possibly only get three power supply bumps on the right one. That block may suffer from insufficient power and noise constraint violation, thus fail to function normally. Next we will introduce the models of the constraints in our problem formulation.

### A. IR-drop Requirement

If the wire resistance is too high or the cell current is larger than predicted, an unacceptable voltage drop may occur, which causes the supply voltage to be lower than required. Similar to [5], the following equation gives the effective resistance (R) for pad transfer metal from a block to the power supply bump with  $C1$  and  $C2$  being constants derived from simulation, where  $dist(b, p)$  is the distance between block and power supply bump.

$$R = C1 + C2 * dist(b, p)$$

Using  $I_{avg}$  as the average DC current for the block, we can obtain voltage drop as  $I_{avg} * R$ . Here we try to bound the resistance between a block and its power sources so that blocks can obtain sufficient power to alleviate IR-drop effect. If some blocks can not obtain enough power to meet power requirement, the violation of IR-drop constraint is occurred.

### B. $\Delta I$ Noise Constraint

In general, the SSN voltage should be less than some peak voltage for a circuit to operate properly [16]. Here we define this peak voltage as the upper bound on  $\Delta V$  for a block, assuming given from intellectual property(IP) block manufacturer. Let  $x_{ij}$  be the amount of power

units delivered from power supply bump  $p_i$  to block  $b_j$ ,  $\delta(x_{ij}) = 1$  if  $x_{ij} > 0$ ,  $= 0$  otherwise,  $(\frac{dI}{dt})_j$  be the maximum rate of current change during transition at block  $b_j$ , which is assumed given from IP provider,  $L_i$  be the parasitic inductance for power supply bump  $p_i$ , which is described in technology file,  $L_{ij}$  be the effective wire inductance from power supply bump  $p_i$  to the center of block  $b_j$ <sup>1</sup>,  $S_j$  be the set of all power supply bumps that connect to block  $b_j$ , and  $\Delta V_j$  be the upper bound on  $\Delta V$  for block  $b_j$ ,  $pr_j$  be the transient switching probability for block  $b_j$ . We define the parasitic voltage drop from package to power supply bump  $p_i$  as

$$\Delta V_{package} = \sum_h \delta(x_{ih}) L_i \frac{pr_h (\frac{dI}{dt})_h}{\sum_{k \in S_h} \delta(x_{kh})}$$

We sum up all the  $pr L \frac{dI}{dt}$  values from  $p_i$  to all the blocks which the power supply bump delivers power to. This is to reflect the sharing of power sources by adding all the inductive induced voltage drop associated with the power sources. Also each  $L \frac{dI}{dt}$  value is divided by the number of power supply bumps which deliver power to each block in the set  $S_h$  ( $\sum_{k \in S_h} \delta(x_{kh})$ ) due to the sharing of power demand, here we simplify the sharing to be equally divided by the power supply bumps, not very realistic though. We also define the inductive induced voltage drop from power supply bump  $p_i$  to circuit block  $b_j$  as

$$\Delta V_{wire} = L_{ij} \frac{pr_j (\frac{dI}{dt})_j}{\sum_{k \in S_j} \delta(x_{kj})}$$

The summation of these two parts for each  $p_i$  and  $b_j$ , which is the total  $\Delta I$  noise induced voltage drop, should be less than or equal to the upper bound on  $\Delta V$  for block  $b_j$ .

$$\Delta V_{package} + \Delta V_{wire} \leq \Delta V_j$$

Block  $b_j$  can work properly only when the inductive induced voltage drop from package to  $p_i$  and from  $p_i$  to  $b_j$  do not exceed this bound.

### C. Problem Formulation

The goal of this paper is to find out the power delivery distribution with power supply noise minimization. Here we try to satisfy the demand of power for every block and avoid possible power supply noise during floorplanning.

**Problem 1** Given a floorplan of  $n$  blocks  $b_1, \dots, b_n$  and their minimum power requirements  $d_1, \dots, d_n$ , respectively, and given a set of  $m$  power supply bumps  $p_1, \dots, p_m$  and the maximum power they can deliver  $s_1, \dots, s_m$ , respectively, find a feasible solution such that each circuit block  $b_j$  obtains  $d_j$  units of power from power supply bumps, and each power supply bump  $p_i$  delivers  $s_i$  units of power or less. Meanwhile, the power delivery assignment needs to meet the  $\Delta I$  noise constraint:

$$\left[ \sum_h \delta(x_{ih}) L_i \frac{pr_h (\frac{dI}{dt})_h}{\sum_{k \in S_h} \delta(x_{kh})} \right] + \left[ L_{ij} \frac{pr_j (\frac{dI}{dt})_j}{\sum_{k \in S_j} \delta(x_{kj})} \right] \leq \Delta V_j, \text{ for each } p_i, b_j \text{ s.t. } \delta(x_{ij}) = 1$$

where those symbols are defined in section II.B.

## III. POWER SUPPLY PLANNING WITH NOISE AVOIDANCE

In order to handle the power supply planning problem along with noise constraint to be met, we need to develop reasonable and efficient strategies to deal with the constraint. In this section, we define feasible power supply region to consider IR-drop requirement, then introduce the construction of special network for power supply planning with noise avoidance. In preserving the advantage of polynomial time max-flow algorithm, we also develop an effective heuristic to deal with  $\Delta I$  noise constraint.

<sup>1</sup>Since effective wire inductance is very hard to extract, we assume that it is proportional to the distance between the block and power supply bump for simplification.

## A. Feasible Power Supply Region

We try to bound the resistance between a block and its power sources to reflect IR-drop effect. Given the current and the upper bound on  $\Delta V$  for a block, we can derive a region which is an expansion of the block in all four directions by a distance  $r$ . Such a region is referred to as the *feasible power supply region* for the block. Only the power supply bumps within the feasible region of a block can deliver power to the block.

## B. Constrained Network Formulation

To solve the problem, we construct a special network graph and run a modified max-flow algorithm [2] to obtain the solution. The graph consists of two kinds of vertices besides the source  $s$  and the sink  $t$ : the circuit block vertices  $B = \{b_1, b_2, \dots, b_n\}$  and the power supply bump vertices  $P = \{p_1, p_2, \dots, p_m\}$ . To simplify the presentation, we use the same name for a vertex and for the corresponding circuit block or power supply bump interchangeably.

The network graph  $G = (V, E)$  is constructed as follows. There is an edge from the source  $s$  to every power supply bump vertex and there is an edge from every circuit block vertex to the sink  $t$ . The edge capacity from the source  $s$  to a power supply bump vertex  $p_i$  is  $s_i$ , which is the maximum power that can be delivered by  $p_i$ . The edge capacity from a circuit block vertex  $b_j$  to the sink  $t$  is  $d_j$ , which is the minimum power that is required by  $b_j$ . There is an edge from  $p_i$  to  $b_j$  if  $p_i$  is inside the feasible power supply region of  $b_j$ . If such an edge exists, the edge capacity is set to  $\infty$ . We can state the problem formally as follows.

$$\text{Maximize } v$$

subject to

$$\sum_{j:e_{ij} \in E} x_{ij} - \sum_{j:e_{ji} \in E} x_{ji} = \begin{cases} v & \text{for } i = s \\ 0 & \text{for all } i \in V - \{s, t\} \\ -v & \text{for } i = t \end{cases} \quad (1)$$

$$\left[ \sum_h \delta(x_{ih}) L_i \frac{pr_h \left( \frac{dI}{dt} \right)_h}{\sum_{k \in S_h} \delta(x_{kh})} \right] + \left[ L_{ij} \frac{pr_j \left( \frac{dI}{dt} \right)_j}{\sum_{k \in S_j} \delta(x_{kj})} \right] \leq \Delta V_j, \text{ for each } p_i, b_j \text{ s.t. } \delta(x_{ij}) = 1 \quad (2)$$

We refer to a vector  $x = \{x_{ij}\}$  satisfying (1) as a flow and the corresponding value of the scalar variable  $v$  as the value of the flow.  $x_{ij}$  is the amount of power units delivered from  $p_i$  to  $b_j$ ,  $\delta(x_{ij}) = 1$  if  $x_{ij} > 0$ ,  $= 0$  otherwise. The rest of the symbols are defined in section II.B. Any flow from the source to the sink in the network assigns power delivering from a power supply bump to a circuit block. We have a theorem as follows.

**Theorem 2** A max flow in the network graph corresponds to a power supply planning solution which maximizes the amount of power delivered from the power supply bumps to the circuit blocks. A feasible solution exists if and only if all edges from the source to the circuit block vertices are saturated.

This theorem guarantees to solve power supply planning problem without the constraint we introduced. As can be seen in the problem definition, the side constraints are non-linear, so it may be treated as NP-hard or approximately NP-hard problem. Therefore we can not use min-cost max-flow/min-cut or maximum bipartite matching algorithms to optimally solve this problem. In the following subsection, we introduce an efficient yet effective algorithm to minimize the violations of  $\Delta I$  noise constraint and still obtain maximum flow.

## C. Priority\_Augmenting\_Path Algorithm

In this section, we describe a priority-based heuristic to deal with power supply noise constraint in max-flow algorithm. In Ford-Fulkerson method[10], we try to find any augmenting path to increase the flow. However, randomly pick feasible augmenting path may cause serious violations for noise constraint in power delivery planning. Fig. 3 shows the constraint violation example when not carefully augmenting the flow. Due to this observation, we implement an efficient algorithm to decide the order of finding augmenting paths based on the priority assigned on the edges between power supply bumps and blocks in our network.

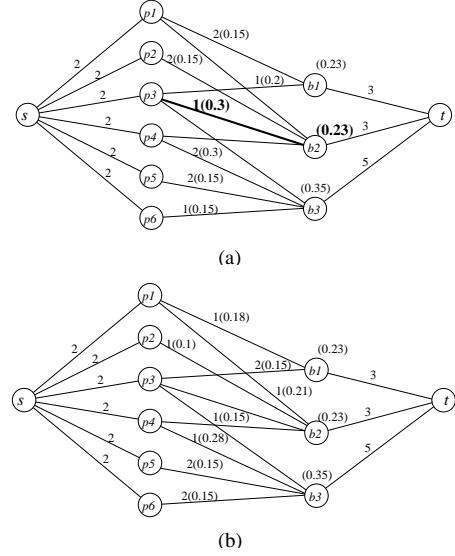


Fig. 3. Numeric examples include two max-flow solutions of the network graph obtained from Fig. 2, the floorplan on the right hand side. Those number are calculated from technology and given IP parameters. (a) The solution with randomly choosing augmenting path. The darker numbers and edge show that there is a  $\Delta I$  noise constraint violation. The number on the edge is the amount of flow on that edge. The number inside the parentheses on the edges between power supply bumps and blocks is the amount of inductive induced voltage drop on that edge. The number inside the parentheses above the block node is the upper bound on  $\Delta V$  for the block. For example,  $e(p_1, b_1)$  has 0.15mV for inductive induced voltage drop, which does not exceed  $\Delta V_1 = 0.23$ mV. But for  $e(p_3, b_2)$ , it has 0.3mV, which exceeds  $\Delta V_2 = 0.23$ mV, indicating a violation. (b) The solution using the algorithm in section III.C. There is no  $\Delta I$  noise constraint violation.

Intuitively, we will choose a path or edge with low inductive induced voltage drop or large  $\Delta V$  for the block to augment the flow. The reason for low inductive induced voltage drop is obvious: we want to deliver power via low voltage drop to blocks; the reason for large voltage tolerance of blocks on inductive induced voltage is that delivering power to small  $\Delta V$  blocks is harder due to cleaner power supply requirement. We assign the cost first to reflect the rough inductive induced voltage drop without the effect of sharing power demand of the block. The cost for edge  $e_{ij}$  from  $p_i$  to  $b_j$  is  $c_{ij} = \left( \frac{dI}{dt} \right)_j * (L_i + L_{ij})$ . We then assign priority values for the edges between  $p_i$  and  $b_j$  as follows. Note that for forward and backward direction of edges, we should assign different priority values so that the preferred augmenting path can be found. For forward direction, the priority value  $P_{ij} = \frac{c_{ij}}{N_j} + \frac{1}{\Delta V_j}$ ; for backward direction, the priority value  $Q_{ji} = \frac{N_j}{c_{ij}} + \Delta V_j$ , where  $N_j$  is the current number of power supply bumps which deliver power to block  $b_j$ .  $N_j$  needs to be updated whenever we obtain an augmenting path and augment the flow since the intermediate flow solution has been modified.

During the process of finding augmenting path, we can use the priority values to select a preferred path. In this way, finding augmenting path which minimizes the violations of noise constraint can be accomplished. The Priority\_Augmenting\_Path algorithm is shown below.

### Algorithm Priority\_Augmenting\_Path

```

begin
 $x := 0$ ;
while  $G(x)$  contains a directed path from  $s$  to  $t$  do
  Identify an augmenting path  $U$  from  $s$  to  $t$ 
  base on priority value of the edges;
   $v := \min\{r_{ij} : e_{ij} \in U, i, j \in V\}$ ;
  Augment  $v$  units of flow along  $U$ ;
  Update  $G(x)$  and  $N_k, k \in B$ ;
end

```

TABLE I  
COMPARISON OF OUR APPROACH WITH [17] AND [13] ON MCNC  
BENCHMARKS. THE RUNTIME AND WIRELENGTH DATA ARE DESCRIBED  
IN SECTION V.

data	bl#	Traditional Floorplanner [17]		PSP Floorplanner [13]		Ours	
		ir-drop vio(%)	noise vio(%)	ir-drop vio(%)	noise vio(%)	ir-drop vio(%)	noise vio(%)
apte	9	0	54	0	54.6	0	3.9
xerox	10	0	61	0	63.2	0	9.1
hp	11	27.3	66	0	61.4	0	7.3
ami33	33	31.3	48	3.1	47.4	3.1	10.1
ami49	49	4.1	61	0	45.5	0	7.6
avg.		12.54	58	0.62	54.2	0.62	7.6

In the algorithm,  $x$  is the flow vector,  $G(x)$  is the residual network,  $r_{ij}$  is the residual capacity for edge  $e_{ij}$ , and  $\nu$  is the residual capacity of the augmenting path  $\bar{U}$  [2]. From our observation and analysis, the runtime of the algorithm is within a small approximate ratio to Edmonds-Karp max-flow algorithm [10].

#### IV. FLOORPLANNING WITH POWER SUPPLY PLANNING AND NOISE AVOIDANCE DESIGN

Our floorplanning algorithm with power supply planning and noise avoidance is based on the Wong-Liu floorplanning algorithm [17]. In this paper, instead of optimizing total wirelength and chip area [17], we propose to perform power delivery planning and power supply noise avoidance design with respect to the current floorplan being considered and in result to obtain a much better floorplan with less power supply noise constraint violations. We choose to optimize the floorplan in fixed die context in this paper, but our approach can also comply with the objective of minimizing chip area in floorplanning.

For the cost function evaluation, we use  $\phi = \alpha A + \beta W + \gamma P$  for floorplanning with power supply planning and noise avoidance, where  $A$  can be either total area of the packing or fixed die penalty if using fixed die implementation, which is zero if the area of floorplan is within the fixed die and is the difference between the area of current floorplan and fixed die area otherwise,  $W$  is total wirelength estimation, and  $P$  is the power supply cost penalty, which is positive if the current floorplan cannot find max-flow solution and/or obtain the violations of power supply noise constraint. The coefficients  $\alpha$ ,  $\beta$ , and  $\gamma$  are weighting parameters and can be changed due to the importance of the terms.

#### V. EXPERIMENTAL RESULTS AND CONCLUDING REMARKS

We have tested our approach on some MCNC building blocks benchmarks. All experiments were carried out on 650MHz+ Pentium-III processor. As in [13], the minimum power required by a circuit block and the max rate of current change during transition at a circuit block are roughly proportional to its area. The power supply bumps are in area-array structure. (In fact, our approach can be applied to other equivalent structures.) The values of parasitic and wire inductance and other technology parameters are from ITRS'97 roadmap [1], .18 $\mu$ m. As for bump pitch, we use the scaling number from [5]. We set all  $pr_j$  for all blocks to be 1 to consider the extreme case, assuming all blocks are switching at the same time. In order to show the effectiveness of our approach, we implement the algorithm in [13] and check for the power supply noise constraint violations at the end. In [13], the cost function for power supply cost part does not include  $\Delta I$  noise constraint violations.

Table I shows the comparison between the floorplans obtained by our approach, those obtained by a traditional floorplanner in [17] without any power supply planning consideration, and those obtained by the floorplanner in [13] with only supply-demand power supply planning consideration during the annealing process. All the floorplans obtained are within a fixed die area with 7% dead space. The IR-drop requirement violation percentage is the number of blocks which obtain insufficient power due to IR-drop effect divided by total number of blocks.  $\Delta I$  noise constraint violation percentage is the number

of power supply bump-block edge constraint violation normalized by the number of total power supply bump-block edge in the network. The floorplans obtained by applying our approach have much less IR-drop violation, over 50% improvement on  $\Delta I$  noise constraint violations and less than 5% of total wirelength increase in average compared with the floorplan obtained in [17]. We also obtain 46.6% improvement on  $\Delta I$  noise constraint violations compared with [13]. It takes roughly 1 hour to solve for *ami33*, which is comparable to [13].

In conclusion, we have presented an approach to further strengthening the power supply planning with constraints which consider the power supply noise avoidance. The efficient yet effective priority-based heuristic we have introduced ensures the polynomial time max-flow algorithm for this difficult problem and experimental results look encouraging. With slight increase of total wirelength, we can obtain big improvement on IR-drop and  $\Delta I$  noise constraint violations in floorplanning stage.

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