A Low Power CMOS Circuit with Variable Souce Scheme (VSCMOS)

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Abstract— This paper proposes a method to reduce the standby leakage current of MOSFET by controlling the voltage of the source node. The method allows to use a low threshold device for high performance speed and low power dissipation in both active and standby periods. This method can be easily applied for conventional ASIC library circuits because no additional processes, circuits, or devices except slight modification for the body contact cell are required.

I. Introduction

For mobile applications, low power consumption is one of the most important requirements. For low power consumption at active operation, without degrading operation speed, lowering both the power supply voltage and the threshold voltage ($V_{\rm th}$) of MOSFET is one of the most effective methods. At the same time, the standby power consumption should be taken into consideration because the standby leakage current of a low $V_{\rm th}$ MOSFET is relatively large. The standby leakage current increases because the drain-source current ($I_{\rm ds}$) in the subthreshold region is determined by the gate-source voltage ($V_{\rm gs}$) and other paramters. The $I_{\rm ds}$ of MOSFET in the subthreshold region is expressed by the following equation:

$$I_{\rm ds} = I_{\rm o} \exp(\frac{V_{\rm gs}\ \ln 10}{s}), \qquad (1)$$

where s is the 's-factor' which is expressed by the following equation:

$$s = \frac{kT}{q}(1 + \frac{C_{\rm d}}{C_{\rm ox}}) \ln 10. \qquad (2)$$

The value $C_{\rm ox}$ is the gate oxide capacitance and $C_{\rm d}$ is the depletion capacitance between the body and channel area. To reduce the threshold voltage without increasing the leakage current, the 's-factor' should be lowered. One method to decrease $C_{\rm d}$ is to supply a body bias $V_{\rm sb}$. The reverse bias between the body and source-channel-drain area increases the width of the depletion region and reduces $C_{\rm d}$. $V_{\rm th}$ and the standby leakage current can be adjusted to meet both operation speed and standby leakage current requirements. To implement this method, however, process parameters have to be modified and controlled accurately, and process variation must be minimized, which is expensive and difficult. There are several circuit techniques to solve this problem. Multi threshold CMOS (MTCMOS) [1, 2, 3] uses p-MOSFETs or n-MOSFETs with high threshold voltage as switch devices in charge path from the power supply or in the discharge path to ground. These switch devices are turned on or off during functional operations or standby periods, respectively. Another approach implements variable threshold CMOS (VTCMOS) [4, 5, 6] to control the body voltage of MOSFETs. The body voltage of p-MOSFETs is lowered and that of n-MOSFETs is raised during normal functional operations while they are raised and lowered during standby periods, respectively. These techniques are implemented for various applications, but they have their own problems. The MTCMOS approach requires additional processes and masks to make MOSFETs with different values of $V_{\rm th}$ within one wafer. Further, appropriate size tuning of the high $V_{\rm th}$ MOSFET and the data holding circuits during standby periods are required. If the internal state has to be preserved during standby periods, it should be stored with additional circuits [3, 7]. The VTCMOS, in the twin-well process, controls the voltage of the substrate which is connected to all of the circuits on the chip. This may generate noise for other circuit blocks such as analog circuits, memory, or I/O macros [8]. The large electric field in the channel area causes reliability problems. In order to improve these drawbacks, a variable source CMOS (VSCMOS) technique controls the source nodes of MOSFETs which are connected to the ground (GND) line and the power supply (VDD) line during the standby periods.

II. Variable Source CMOS Circuit

Figure 1 shows the block diagram of the VSCMOS inverter. VSCMOS circuits use MOSFETs with one common threshold voltage. The source nodes of the p- and

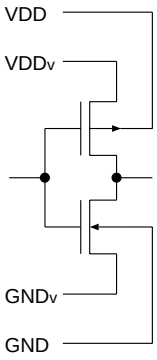

Fig. 1. VSCMOS inverter block diagram

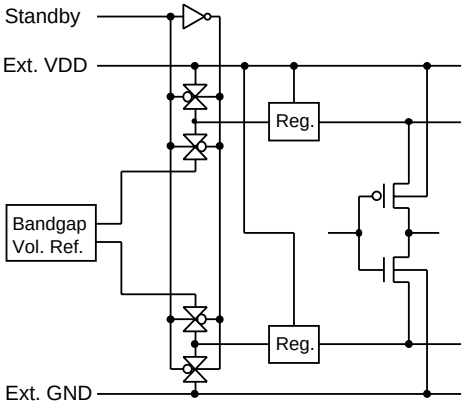

Fig. 3. VSCMOS Circuit (I)

n-MOSFETs are connected to virtual VDD (VDDv) and virtual ground (GNDv), respectively. The VDDv and GNDv are kept at the same level as VDD and GND during active periods, while they are lowered and raised during standby periods, respectively. Further, with this method, VDD and GND can be modified to achieve active low power. Even for a p-substrate twin-well process, the substrate level is not controlled in this circuit. Thus, it doesn't cause any problems for other circuits which operate even during standby periods. In standby mode in a VSCMOS circuit the electric field around the drain diffusion area is not so high as in a VTCMOS circuit because the body is not biased against the gate and drain. Therefore, the reliability of the device in VSCMOS is better than that in VTCMOS. This electric field causes leakage current from drain to substrate, too. Figure 2 shows the drain current (I_{di}) and source current (I_{si}) versus V_{gs} for two n-MOSFETs of different sizes. This figure shows that I_{di} is almost the same as I_{si} when V_{gs} is not negative. For negative V_{gs}, however, I_{di} doesn't decrease due to the effect of GIDL. The GIDL is caused by the large electric field between the drain and body as well as by V_{gs}. These undesired phenomena which may be caused by VTCMOS circuits can be avoided with VSCMOS circuits.

III. Circuit Implementations

If VDDv and GNDv are supplied independently of the VDD and GND with dedicated pins, the control of VDDv and GNDv is simple. No additional circuit such as regulator or voltage reference is not required on the chip. As for single power supply chip, however, some additional circuits are required. Several circuits to implement VSCMOS are described here, based on the p-substrate twin-well process. In Figure 3, the external VDD and external GND are fed into the n-well and substrate of the MOSFET directly while the source nodes of the MOSFETS are connected to their own regulator. The bandgap voltage reference generates voltage levels for standby periods. The standby signal switches the output level of both regulators. Figure 4 shows another example with a charge pump circuit. In this circuit, the source level of the p-MOSFET is connected directly to the external VDD, while the voltage of the n-well is raised during standby

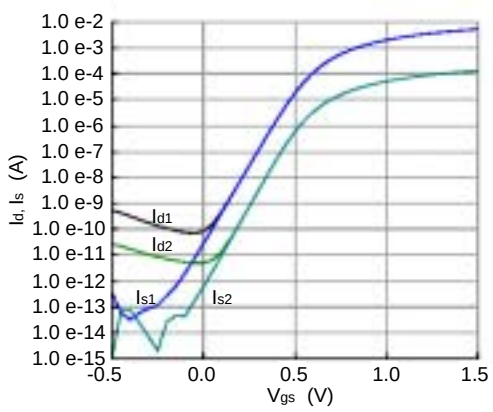

Fig. 2. MOSFET Drain and Source Current Versus Gate Voltage

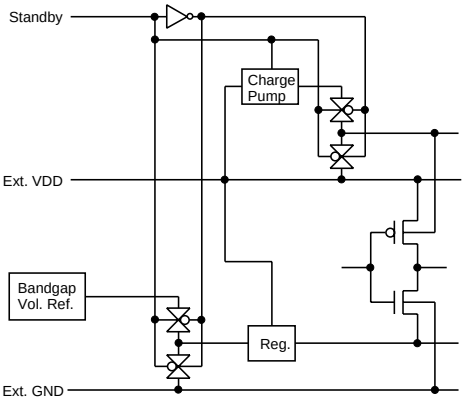

Fig. 4. VSCMOS Circuit (II)

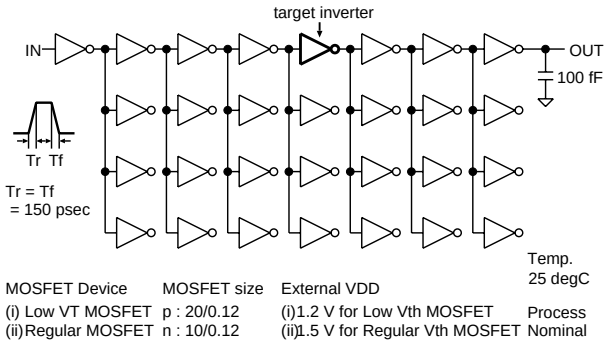

Fig. 5. VSCMOS evaluation circuit (I)

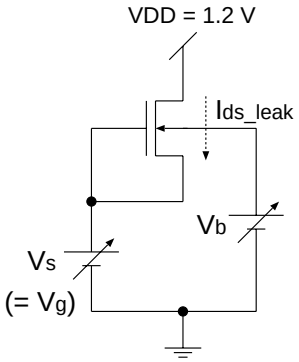

Fig. 7. VSCMOS evaluation circuit (II)

periods. The voltage of the n-well can be controlled without any effect on the other circuit blocks. In most of the applications, the external voltage is higher than the internal VDD due to the restriction of the I/O buffer operation voltage, the noise margin, and so on. In such cases, internal voltage references and regulators are used to generate internal VDD with the external VDD. To apply VSCMOS to this case, two more regulators or one regulator and one charge pump circuit are appended. Thus, VSCMOS circuit can easily be implemented with the conventional circuit.

IV. Evaluation

Figure 5 shows an evaluation circuit and simulation condition of the VSCMOS. These inverters are implemented as VSCMOS circuit with low $V_{\rm th}$ or regular $V_{\rm th}$ MOSFETs. The external VDD is 1.2 V for the low $V_{\rm th}$ MOSFETs and 1.5 V for regular $V_{\rm th}$ MOSFETs. Static leak current and the operation speed of the target inverter which is located at the middle of the circuit are compared for two different values of $V_{\rm th}$. Figure 6 shows the simulation result of standby leakage current of VSC-

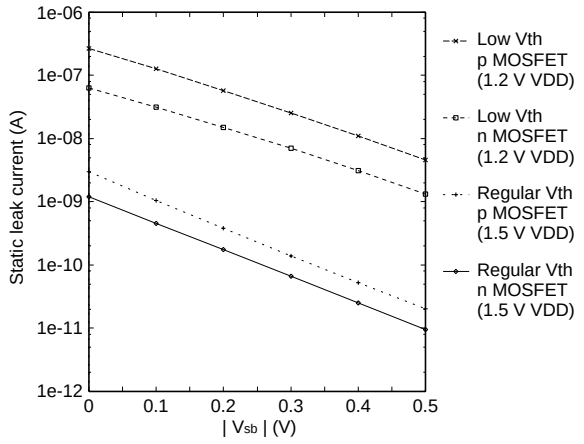

Fig. 6. VSCMOS evaluation result (I)

MOS inverter. In this simulation, the voltage of the body is fixed. Thus, $|V_{\rm sb}|$ shows the amount of source voltage shift from the fixed body voltage. The top two lines are for p-MOSFET and n-MOSFET with low $V_{\rm th}$, respectively, while the bottom two lines are for those with regular $V_{\rm th}$. This figure shows the static leakage current of the low $V_{\rm th}$ MOSFET at 0.5 V $|V_{\rm sb}|$ is lowered down to the same level as that of regular $V_{\rm th}$ MOSFET at 0.0 V $|V_{\rm sb}|$. The operation speed of the target inverter was checked for both the low $V_{\rm th}$ device and the regular $V_{\rm th}$ device. The following table shows these results.

Table Target Inverter Operation Performance

	Delay (ps)		Slew (ps)	
	Rise	Fall	Rise	Fall
Low $V_{\rm th}$ MOSFET (1.2 V)	27.54	25.84	51.67	43.98
Regular $V_{\rm th}$ MOSFET (1.5 V)	33.32	30.78	58.41	50.00

From this table, it can be seen that the operation speed (both delay and slew) of the circuit with low $V_{\rm th}$ MOSFETs at 1.2 V is faster than that of the circuit with regular $V_{\rm th}$ MOSFETs at 1.5 V. The active power consumption of the circuit with low $V_{\rm th}$ device is lower than that of the circuit with regular $V_{\rm th}$ because VDD for the low $V_{\rm th}$ circuit is 80 % that of the regular $V_{\rm th}$ circuit. From these results, the VSCMOS circuit with low $V_{\rm th}$ devices keeps standby power, and improves the active power and operation speed compared with conventional circuits with regular $V_{\rm th}$ devices. Figure 7 shows another evaluation circuit. In this figure, the gate node of the n-MOSFET is connected to its source node. With this circuit, $I_{\rm ds\_leak}$ $(= I_{\rm off})$ versus $V_{\rm s}$ $(V_{\rm g})$ can be evaluated while controlling $V_{\rm b}$. Figure 8 shows the results of this simulation. The value of $V_{\rm s}$ shows the shift voltage level of the source node. These results show that $I_{\rm ds\_leak}$ $(= I_{\rm off})$ decreases to 1/30 or less for 0.5 V $V_{\rm s}$ shift from 0.0 V to 0.5 V for any value of $V_{\rm b}$. The same amount of $I_{\rm ds\_leak}$ is achieved for about 1.0 V $V_{\rm b}$ shift. Thus, the shift of the source potential of the MOSFET is more effective than that of body

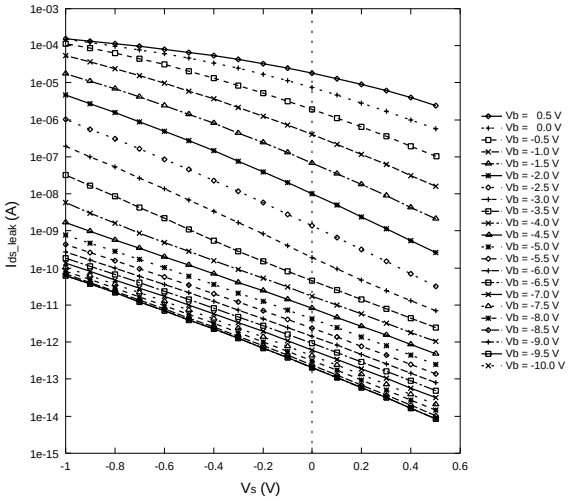

Fig. 8. VSCMOS evaluation result (II)

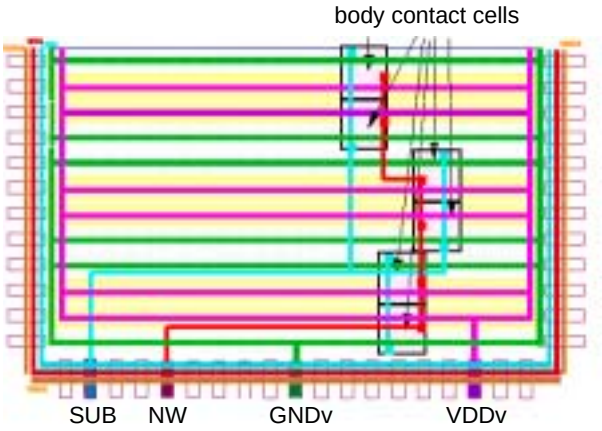

Fig. 9. VSCMOS VDD GND distribution

potential. Figure 9 shows an example of power distribution in an ASIC layout. In most ASIC libraries, substrate and n-well contacts are not included in circuit cells but in the contact cells which are shown as body contact cells in this figure. Therefore, with minor modifications to this body contact cell, the source node, substrate node, and n-well node can all be wired out as the external signals or internal control signals which should be controlled by regulators or charge pump circuits independently. This means that it is easy to apply VSCMOS design methodology to existing ASIC circuits.

V. Conclusion

The VSCMOS circuit which controls the source voltage of the MOSFET effectively reduces standby leakage current. The voltage of substrate is not controlled in order not to cause any problems for other circuits. The reliability of the devices is improved because of the weaker electric field between the substrate and channel area. This method requires neither MOSFET devices with different threshold voltages nor triple-well structures, which reduces process costs. This enables designers to use low $V_{\rm th}$ devices for high speed and low power applications. Further this method requires little modification to the existing circuits in order to apply it to the conventional ASIC library circuits. For the LSIs with single power supply, low power voltage regulator for VDDv and GNDv is key factor to implement this method.

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