# Design Methodology of Low-Power CMOS RF-ICs

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**Abstract This paper presents design methodology for CMOS RF-ICs in the 2-GHz band. After describing RF transceiver architectures, it introduces some low-voltage, low-power CMOS front-end circuits that use an LC-tank folding technique. Finally, it presents a 1-V, 12-mW image-rejection receiver in the 2-GHz band.**

## I. Introduction

Wireless communications by cellular telephone has progressed through first-generation analog, second-generation digital, and third-generation wideband systems, and the direction of research at present is toward high-speed transmission and high-speed mobility for a fourth-generation system. Recently, there has also seen much activity in the development of short-range wireless communications systems, such as Bluetooth in the 2.4-GHz band and wireless LANs in the 2.4- and 5-GHz bands. We can therefore see a foundation evolving for ubiquitous communications. Regarding semiconductor devices, silicon devices are becoming viable in the main wireless bands from 800 MHz to 5 GHz. CMOS devices can also be found in an applicable range, as CMOS transistors have attained high-frequency capability through fine-processing technology.

In recent years, research on CMOS RF transceivers and circuits has been very active [1-9]. Furthermore, several transceiver architectures, such as direct-conversion, wideband intermediate frequency (IF), and low-IF configurations, have been exploited for single-chip integration [1-3]. The alleviation of RF specs in Bluetooth has prompted development of single-chip RF transceivers.

Section II describes architectures for single-chip transceivers. Section III presents a design methodology for low-voltage CMOS RF front-end circuits. Section IV presents an image-rejection receiver for 2-GHz applications.

## II. Single-Chip RF Transceiver Architectures

Traditionally, superheterodyne receivers (SHRs) have been used in wireless transceivers. For channel selection, SHRs need external IF filters, whose center- and cutoff-frequencies are fixed depending on the system. The IF filters are bulky and add costs to transceivers. The demand for smaller and less expensive transceivers has stimulated exploitation of new architectures suitable for single-chip radios. Furthermore, multi-standard transceivers that use flexible filtering for channel selection are recently demanded, which means SHRs are not suitable for this application.

Most transceivers suitable for single-chip integration have direct-conversion, wideband IF, or low-IF configurations. In all of these configurations, channel selection can be done with on-chip active filters. A generic direct-conversion transceiver is shown in Fig. 1. It is also called the zero-IF architecture, and as the name implies, image response does not exist, while DC offset and second-order distortion become new problems [1]. Therefore, DC offset cancellation and high-linearity receiver front-end circuits are indispensable. Potentially, the direct-conversion configuration can be applied to any wireless

system. Figure 2 shows a block diagram of a wide-band IF receiver [2], which has a high IF ranging from 100 to 200 MHz. Therefore, image signals are rejected using an external RF bandpass filter and image-rejection mixers based on Weaver's architecture [10]. Because this combination can make image-rejection high [2], the wideband IF receiver can also be applied to any wireless systems. Figure 3 shows a block diagram of a low-IF receiver [3]. Because image signals are in-band signals, image rejection is performed by only image-rejection mixers. The principle of the image-rejection mixer is the same as that of the wideband IF receiver. However, image signal cancellation can be done in the digital domain because of the low IF. The low-IF configuration can be applied only when image-rejection specs can be set low, for example, in Bluetooth or GSM with IF=100 kHz [3] (The adjacent signal is the image signal). Low power consumption is the key to expanding the use of CMOS single-chip transceivers because more active circuits are necessary for IF and baseband analog-signal processing.

Since 2000, a number of product announcements for CMOS RF transceivers have focused on Bluetooth, and many papers in this regard have been presented [5-7]. At present, however, the main objective is to achieve a one-chip configuration, and power consumption is still large, 100 mW or greater. Figure 4 shows a block diagram of a RF transceiver for Bluetooth using an another low-IF configuration in the receiver. The image-rejection mixer uses an IF-band polyphase filter [11] to cancel the image signal, thereby providing only the desired signal at the output of the mixer.

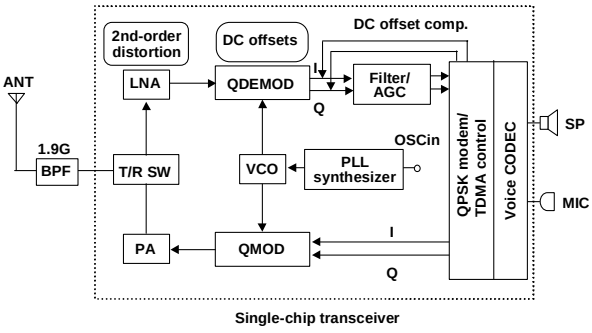



**Fig. 1 Direct-conversion transceiver.**

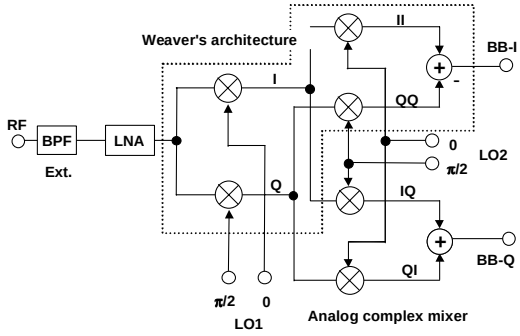
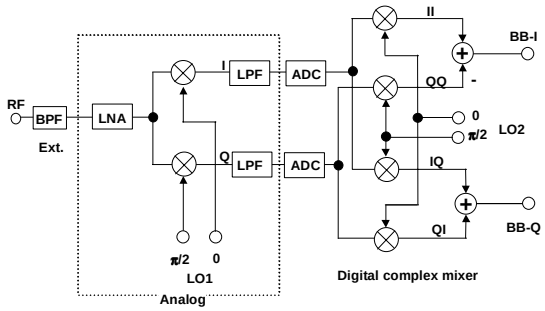



**Fig. 2 Wideband-IF receiver.**




**Total NF = 8.2 dB, Image rejection = 32.2 dB**

**Fig. 3 Low-IF receiver.**

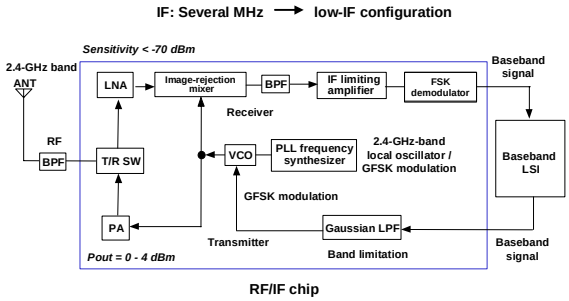



**Fig. 4 Low-IF transceiver for Bluetooth.**

## III. 0.5 to 1-V RF Circuits Using an LC-Tank Folding Technique

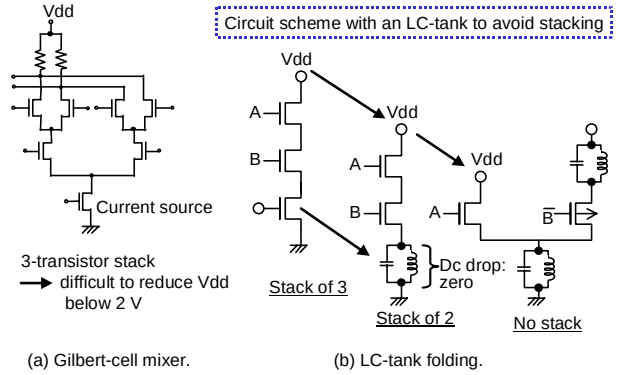
Inside the above RF transceivers, a power amplifier (PA) is an energy conversion device that achieves low-power consumption through its high-efficiency operation. In the case of short-range communications, a small PA output is sufficient (about 1 mW in Bluetooth), but this means that power consumption in the other RF circuits will be much larger. Because a RF circuit is an analog circuit, current consumption must be held constant to maintain characteristics.

Low-voltage operation is therefore an effective means of reducing power consumption here.

This section describes 2-GHz receiver front-end blocks that can operate at extremely low voltages down to 0.5 V [4]. They are a low noise amplifier (LNA), a down-conversion mixer, and a voltage-controlled oscillator (VCO) fabricated by 0.2-μm fully-depleted CMOS/SIMOX technology, which is one of the thin-film Silicon-on-insulator (SOI) technologies. The 0.5-V operation results from using two circuit techniques. One is an LC-tank folded Gilbert cell, and the other is the use of undoped MOSFETs in the VCO core and buffers for the mixer and VCO. SOI devices have excellent RF performance even at voltages below 1 V because of reduced capacitance in the drain region and the higher values of transconductance per unit drain current, compared to bulk-CMOS technologies. Moreover, fully-depleted CMOS/SIMOX technology allows us to make undoped (depletion) MOSFETs with no process steps added to the normal SIMOX process, thereby enabling low-voltage operations.

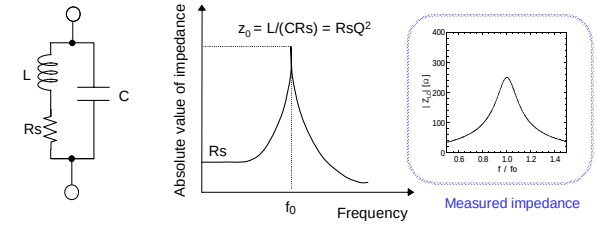
In order to lower supply voltage, the stacking of transistors must be avoided. The Gilbert-cell mixer in Fig. 5(a), which is most commonly used for the mixer, normally has a stack of three transistors. Therefore, the minimum supply voltage is around 2 V.

We propose using an LC tank instead of the current source, which can make the dc drop zero. The LC tank acts as a current source at around its resonant frequency because the impedance is high enough. Figure 5(b) shows the concept of the LC-tank folding. First, the LC tank connected to the ground replaces the transistor current source. At this stage, two transistors are still stacked. Next, the series-connected circuit is folded at the node between two transistors. As a result, the stacking of MOSFETs can be avoided. Figure 6 shows characteristics of the LC tank. At the resonant frequency, the impedance of the LC tank attains the peak value of $RsQ^2$. Stacking four-layer interconnections for the spiral inductor, the measured peak impedance is about 250 Ω as shown in Fig. 6(b). Figure 7 shows a schematic of the proposed folded mixer. Using LC tanks having resonant frequency of about 2 GHz, the RF input pair (M1 and M2) is folded. Although current paths are doubled compared to the Gilbert cell, the total current can be decreased by optimizing the size of the nMOSFETs and pMOSFETs because their dc operating points can be independently changed. Complementary source followers with undoped FETs are used for the output buffers.




(a) Gilbert-cell mixer. (b) LC-tank folding.

**Fig. 5 Stacking of transistors.**




(a) Equivalent circuit of LC-tank (b) Impedance of LC-tank

**Fig. 6 LC-tank circuit.**

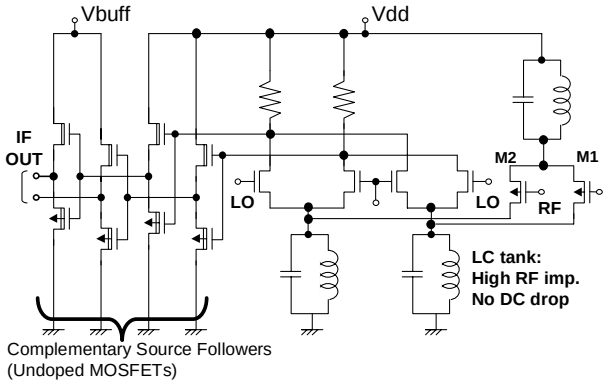



**Fig. 7 LC-tank folded mixer.**

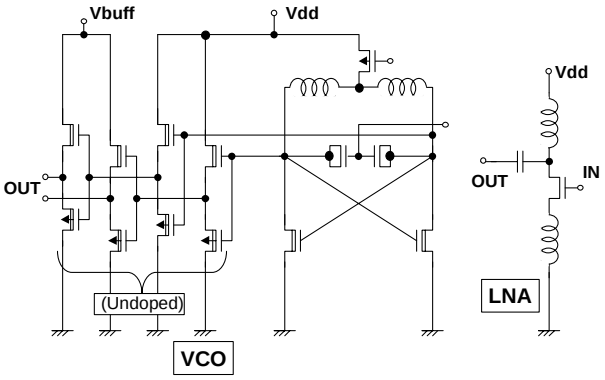



**Fig. 8 Schematics of the VCO and LNA.**

Figure 8 shows schematics of the VCO and LNA. The undoped nMOSFETs are also used in the cross-coupled transistors of the VCO to lower the supply voltage to 0.5 V. The LNA has a source inductor to lower the noise figure at 50-Ω input impedance.

At 2 GHz, the 50-Ω noise figure and associated gain of the LNA are 3.5 dB and 10 dB, respectively, at a supply voltage of 1 V. The LNA dissipates 10 mA at 1-V supply. Figure 9 shows the measured single sideband (SSB) noise figure and conversion gain of the mixer at supply voltages of 1 and 0.5 V. The IF is fixed at 170 MHz. The current dissipations of the core circuit and the final buffers are respectively 19 and 11 mA at 1-V supply. At a local frequency of 2 GHz, conversion gains of 6.7 dB at 1 V and 1.5 dB at 0.5 V are obtained, while the SSB noise figures are 16.1 dB (1 V) and 19.5 dB (0.5 V). The 2-GHz-band VCO can oscillate at voltages below 1 V.

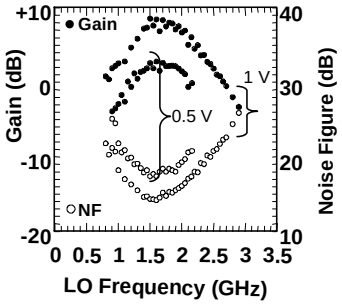



**Fig. 9 Noise figure and conversion gain of the mixer.**

Figure 10 shows the phase noise of the VCO at 1-V supply. The phase noise at 1 MHz offset is at about -110 dBc/Hz. The supply current is 7 mA at 1-V supply. The final buffers consume 3 mA. The total current dissipations of these RF front-end circuits are 36 mA at 1 V and 18 mA at 0.5 V. Currents in the final buffers are ignored because they are only for the measurement.

Using the above circuit techniques, we can build 1-V front-end circuits suitable for short-range wireless systems like Bluetooth.

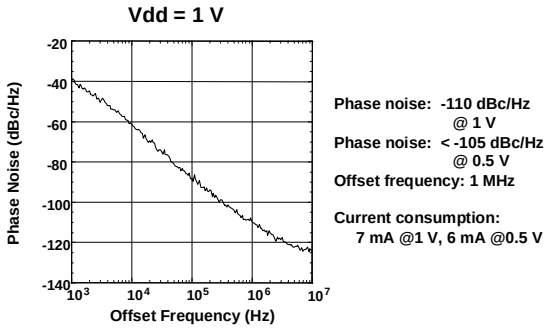



**Fig. 10 Phase noise of the VCO.**

## IV. 1-V Image-Rejection Receiver

The LC-tank folding technique is applied to a low-voltage image-rejection receiver [8]. Figure 11 shows a block diagram of the low-IF image rejection receiver. It consists of an LNA, a quadrature mixer using the LC-tank folding, and local oscillator (LO) and IF three-stage polyphase filters. The quadrature mixer is shown in Fig. 12. Different from the mixer in Fig. 7, an NMOS single-to-balance converter is used, whose differential outputs are AC-coupled to I/Q mixing cores. To improve balance characteristics, the combination of a transistor current source and an LC-tank is used. The I/Q mixing cores are combined at nodes A and B to save the silicon area occupied by the LC-tanks. Furthermore, this configuration can improve quadrature characteristics of the LO signals, thereby providing high image rejection. A photomicrograph of the image-rejection receiver implemented by 0.2-μm CMOS/SIMOX is shown in Fig. 13. The receiver has the image rejection

ratio (IRR) of 49 dB, as shown in Fig. 14, and consumes 12 mW at a 1-V supply. The total receiver noise figure (NF) is 10 dB with the LNA noise figure of 3.1 dB.

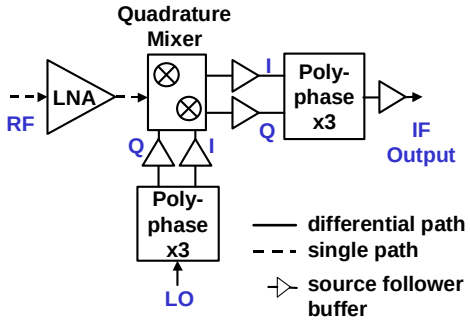



**Fig. 11 Image-rejection receiver.**

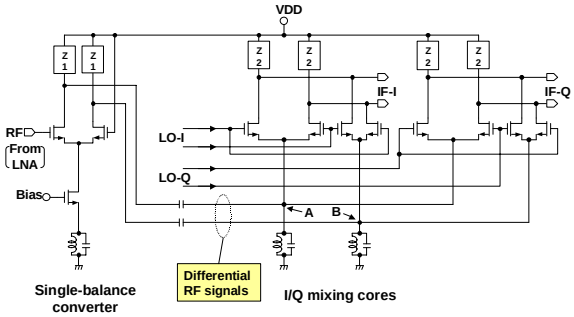



**Fig. 12 Low-voltage quadrature mixer.**

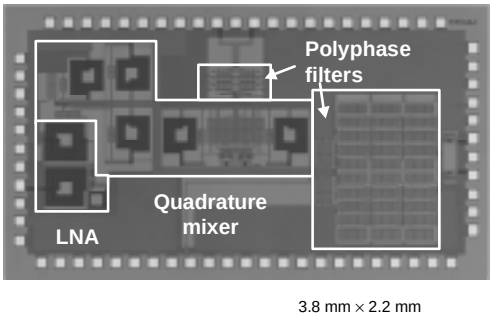



**Fig. 13 Photomicrograph of the image-rejection receiver.**

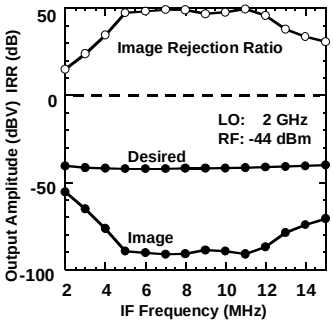



**Fig. 14 Image-rejection characteristics.**

## V. Conclusion

Design methodology for CMOS RF-ICs in the 2-GHz band was described. First, transceiver architectures suitable for single-chip implementation were introduced. Then, low-voltage, low-power CMOS RF circuits using the LC-tank folding technique were discussed. Finally, a 1-V, 12-mW image-rejection receiver in the 2-GHz band was presented.

These technologies are very effective for a short-range low-power radio communication like Bluetooth. Furthermore, “RF System on a Chip" with a single power supply would be feasible in coexistence with digital baseband circuits.

## Acknowledgments

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