On Improving FPGA Routability Applying Multi-level Switch Boxes

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Abstract— In this paper, we propose a new FPGA switch box design style — the extended switch boxes. An extended switch box is multi-level in nature. It consists of a kernel and extension(s) connected to the kernel, while many conventional switch boxes only consist of the kernel part and are referred to as single-level switch boxes. We show that with a much reduced total number of manufactured switches in the chip, this new design has a guaranteed complete mappability from any global routing to a feasible detailed routing of the entire FPGA chip. The interesting results seem to open a new avenue for designing FPGA routing structures.

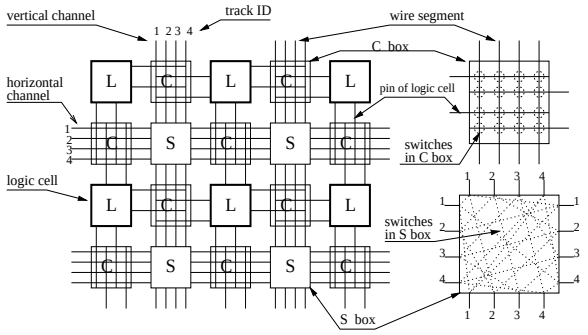

Fig. 1. The architecture of a 2D-FPGA.

I. Introduction

A typical 2*D*-FPGA architecture is shown in Fig.1. It consists of The functional blocks (or logic cells) are marked by L, which are separated by vertical and horizontal channels. There are W (called channel density) prefabricated parallel wire segments running between each pair of adjacent L-cells in both vertical and horizontal channels. The wire segments in a vertical (or horizontal) channel are aligned into W vertical (or horizontal) tracks; each track within a channel is assigned an integer in $\{1, \ldots, W\}$ as its track ID. There are C-boxes in the channel between adjacent L-cells. A Switch Box (S-box), located at each intersection of a vertical and horizontal channels, contains programmable switches to connect wire segments running from its surrounding C-boxes. The S-boxes in Fig.1 are 4-way. A k-way S-box with W terminals on each side is denoted by (k, W)-SB.

When an FPGA is used to realize a specified Boolean function, the pins used to realize the Boolean function are partitioned into groups (called nets). Then the pins in each group are connected together to form a real net by using available wire segments and switches in both C-boxes and S-boxes; different nets are disconnected. The latter process is referred to as a routing. Conventionally, the routing process is divided into two subsequent steps, global routing and detailed routing. In this paper, we simply use the term of global routing to specify the connection topologies for all nets. The detailed routing decides the exact assignment of wire segments and switches used to materialize the complete routing. As the connectivity within C-boxes is complete, the routability of the entire chip is fully dependent on the structure and connectivity of the S-boxes [1, 2, 3, 4, 7, 8, 9, 11, 12, 10]. Routability justification of an FPGA chip is always a tough job which is done usually by experiments as the results are router and benchmarks dependent.

In order to complete a detailed routing for the entire chip, the notion of a so-called greedy routing architecture has been addressed [9, 10, 12]. The approach starts the detailed routing from a pre-specified S-box. Then routings of adjacent C-boxes are determined and serves as the predetermined side(s) of other neighboring (and unmapped) S-boxes. This process is repeated (propagated) until the entire chip routing is done. Depending on the propagation order (e.g., either spiral or snake-like [9, 10, 12]), the process can be decomposed into a sequence of h-side predetermined k-way S-box design problems for $k = 3, 4$ and $0 \leq h \leq k$. An h-side predetermined (k, W)-SB B is said to be *mappable with the h-side track fixed* if for each k-way global routing GR with density at most W, all nets in GR can be realized in B simultaneously such that if a net N in GR joins terminals of some predetermined sides, then these terminals are reserved for N only. We simply call *mappable* if $h = 0$.

With this design scheme, we need to study the following two problems.

Problem (1) *Design a (k, W)-SB which is mappable with h-side track fixed, and contains the minimum number of switches.*

(2) *Design a greedy routing structure so that on replacing the S-boxes in an FPGA by proper mappable with h-side track*

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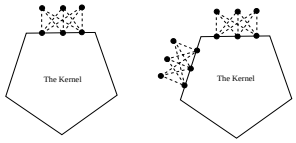

Fig. 2. The extended S-box architecture.

fixed S-boxes, the FPGA chip is perfect mappable and contains the minimum number of switches.

In this paper, we focus on Problem (1) only. To judge a S-box, [2] introduced the so called *flexibility* of a S-box which is the maximum number of switches joining one terminal in the S-box. Thus, it is desirable to design S-boxes which are mappable with h-side track fixed S-box, and have the minimum number switches as well as the minimum flexibility.

In [12], the authors designed an optimum mappable with 1-side track fixed $(3,W)$-SB with $\frac{W^2}{2}+2W$ switches. In [8], the authors proposed h-side predetermined $(4,W)$-SB (which is mappable with the h-side track fixed) with $\frac{3}{2}W^2+3W, \frac{7}{2}W^2+2W, 5W^2+W$ switches and flexibilities $W+3, 3W, 3W$, respectively for $h=1,2,3$. A 4-side predetermined $(4,W)$-SB is the switch box with all possible switches and hence it has $6W^2$ switches of flexibility $3W$.

The S-box family constructed in [8] can be shown to be optimum and mappable. However, in this paper, we will show that it is possible to further improve upon those "optimum" S-boxes should we be allowed to adopt a different design style. The goal of this paper is to design S-boxes to replace the h-side predetermined k-way S-boxes proposed in [8] with (1) fewer number of switches; (2) smaller flexibility; and (3) easy to detailed-route. Our idea is to design a S-box with two levels.

In Section 2, we provide the architecture of h-side extended k-way S-box for any $0 \le h \le k$. According to this architecture, we are able to provide workable h-side predetermined 4-way S-boxes ($0 \le h \le 4$) in Section 3, and compare them with the h-side predetermined 4-way S-box presented in [8]. Section 4 is a conclusion.

II. The extended switch box architecture

Let k,h be integers such that $0 \le h \le k$. Let W be any positive integer. A (k,W)-*kernel* is simply a (k,W)-SB. A 1-*side extension* of a (k,W)-kernel K is a set of W terminals each of which is connected to some of the terminals in a side of K. The new S-box so formed is called a 1-*side extended* (k,W)-*SB*. If the terminals in an extension is connected to every terminal in a side of S, it is called a *full extension*. An *h-side extended* (k,W)-*SB* is a S-box obtained by attaching h 1-side extensions to h different sides of a (k,W)-kernel. Fig.2 shows the structures of a 1-side full extended 5-way S-box and a 2-side full extended 5-way S-box. Full extended S-box has high routability.

Theorem 1 *An h-side fully extended (k,W)-SB is mappable with the h-side track fixed if and only if the kernel is mappable.*

Proof. Let B be an h-side fully extended (k,W)-SB with kernel K. For any global routing GR with density at most W, if GR is mappable with the h-side track fixed in B, then the detailed routing induces a detailed routing of GR in K. On the other hand, if there is a detailed routing of GR in K, then this detailed routing can be easily extended to an h-side track fixed detailed routing to B as B has h-side full extension.

This completes the proof. ∎

We usually have a full extension to ensure the mappability. By Theorem 1, the problem of designing extended S-boxes becomes the problem of designing mappable kernels. In [5], for any fixed integer $k>1$, we have constructed a mappable (k,W)-kernel with $O(W)$ switches. Combine with Theorem 1, we have the general result about the extended S-boxes.

Theorem 2 *Let k,h be integers such that $0 \le h \le k$. Let W be any positive integer. There is a h-side extended (k,W)-SB with $hW^2+O(W)$ switches, which is mappable with the h-side track fixed.*

We note that an h-side extended (k,W)-SB is a replacement of h-side predetermined (k,W)-SB in FPGAs.

III. The extended 4-way switch boxes

We describe two families of $(4,W)$-SBs which will be used as the kernels in our extended 4-way S-boxes.

A conventional (k,W)-SB can be modeled by a graph. Label the terminals on the i-th side by $v_{i,1},\ldots,v_{i,W}$, for $i=1,\ldots,k$. An edge $v_{i,j}v_{p,q}$ represents a switch joining the j-th terminal on the i-side and the q-th terminal on the p-th side. Then a (k,W)-SB is a k-partite graph $((V_1,\ldots,V_k),E)$ with vertex partition $(V_1,\ldots,V_k)$ where $V_i=\{v_{i,j}|j=1,\ldots,W\}, i=1,\ldots,k$, E is the set of switches.

We have developed a reduction design technique in [5], that is, for any fixed k, any (k,W)-SB can be built by combining some small S-boxes. Let $SB_1=((V_1,V_2,\ldots,V_k),E_1)$ and $SB_2=((U_1,U_2,\ldots,U_k),E_2)$ be a (k,W_1)-SB and a (k,W_2)-SB, respectively. The disjoint union of SB_1 and SB_2, denoted by SB_1+SB_2, is a (k,W_1+W_2)-SB $((V_1\cup U_1,V_2\cup U_2,\ldots,V_k\cup U_k),E_1\cup E_2)$, where all the unions are disjoint unions.

In [6], we have designed the following optimum or near optimum mappable $(4,W)$-SB $H(W)$ with at most $19W/3$ switches.

$$H(W)=\begin{cases} hH_6 & \text{if } W=6h,\\ (h-1)H_6+H_7 & \text{if } W=6h+1,\\ hH_6+H_2 & \text{if } W=6h+2,\\ hH_6+H_3 & \text{if } W=6h+3,\\ hH_6+H_4 & \text{if } W=6h+4,\\ hH_6+H_5 & \text{if } W=6h+5. \end{cases}$$

Where H_i (see Fig. 3) is a mappable optimum $(4,i)$-SB for $i=1,2,3,4,5$, and a mappable $(4,i)$-SB for $i=6,7$.

Now we propose to use $H(W)$ as a $(4,W)$-kernel in our h-side extended $(4,W)$-SBs. Let $ES(W,h)$ be the h-side full extension of $H(W)$. Fig. 4 shows the general structure of

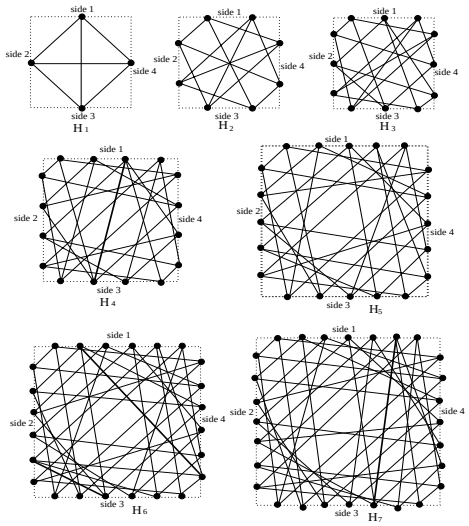

Fig. 3. A family of mappable 4-way S-boxes.

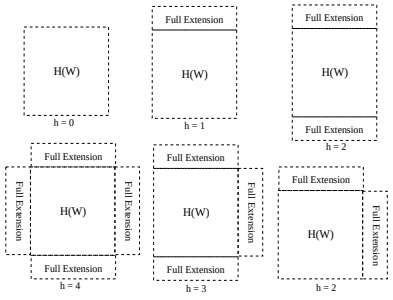

Fig. 4. $ES(W,h)$ for $h = 0,1,2,3,4$.

$ES(W,h)$ and Fig. 5 provides the family of $ES(3,h)$ for $h = 0,1,2,3,4$. The following theorem is a consequence of Theorem 1.

Theorem 3 *$ES(W,h)$ is a mappable with the h-side track fixed. $ES(W,h)$ contains at most $hW^2 + 6.\overline{3}W$ switches, and the flexibility is at most $W+4$.*

Comparisons of $ES(W,h)$ and the h-side predetermined $(4,W)$-SB $G(W,h)$ in [8] is given in Table I, for $h = 0,1,2,3,4$.

4-way S-boxes are widely used in industry. We have provided a family of better S-boxes than the h-side predetermined S-boxes proposed in [8] in terms of the number of switches. Moreover, since $H(W)$ consists of some H_6s and at most one H_i for $i = 2,3,4,5,7$, we can design an efficient detailed routing algorithm for $H(W)$ and hence for $ES(W,h)$. This is an useful observation as the mapping of global routings to detailed routings has been shown to have no efficient algorithm in general.

If the nets in a global routing are 2-pin nets, the authors in [4] designed the following $(4,W)$-SB $U(W)$, which contains $6W$ switches, and is mappable for 2-pin net global routings.

$$U(W) = \begin{cases} hH_2 & \text{if } W = 2h, \\ hH_2 + H_1 & \text{if } W = 2h+1. \end{cases}$$

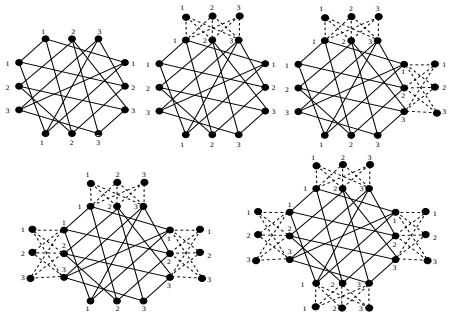

Fig. 5. $ES(3,h)$ for $h = 0,1,2,3,4$.

TABLE I
COMPARISONS OF $ES(W,h)$ AND $G(W,h)$

h	$\lvert ES(W,h)\rvert \leq$	$\lvert G(W,h)\rvert$[8]	F_s of $ES(W,h)$	F_s of $G(W,h)$
0	$6.\overline{3}W$	NA	4	NA
1	$W^2 + 6.\overline{3}W$	$1.5W^2 + 3W$	$W+3$	$W+3$
2	$2W^2 + 6.\overline{3}W$	$3.5W^2 + 2W$	$W+3$	$3W$
3	$3W^2 + 6.\overline{3}W$	$5W^2 + W$	$W+4$	$3W$
4	$4W^2 + 6.\overline{3}W$	$6W^2$	$W+4$	$3W$

For FPGAs in which only 2-pin net global routings are concerned, we propose the h-side extended S-box, $ES_U(W,h)$ to be the h-side full extension of $U(W)$. Fig. 5 actually shows also the family of $ES_U(3,h)$ for $0 \leq h \leq 4$. Again from Theorem 1 we have the following result.

Theorem 4 *$ES_U(W,h)$ is mappable with the h-side track fixed for 2-pin nets global routings. The number of switches in $ES_U(W,h)$ is at most $hW^2 + 6W$, and the flexibility is $W+3$.*

IV. CONCLUSIONS

This is probably the first work giving the theoretic justification for designing multi-level (or multi-staged) S-boxes for improving FPGA mappability. In this paper, we have investigated the problem of optimum S-box designs for achieving a perfect mapping upon the entire chip. Such a mapping can be achieved using the greedy routing structure that can construct an optimum routing on the entire chip from local optimum routings around individual S-boxes.

To achieve such a goal, we have proposed a novel notion of extended switch box architecture which consists of a kernel and an extension level. Applying the reduction design technique for S-boxes, we can design all types of mappable S-boxes with significantly reduced number of switches and switching flexibilities. In particular, we have obtained a family of 4-way S-boxes which is the best in any aspect compared to other known 1-level S-boxes. These S-boxes can be used in the conventional FPGA chip (as shown in Fig.1.) to achieve a perfect mappability on the entire chip applying the greedy routing schemes.

It is quite interesting to see that by adopting the proposed extended S-box design style, the switch density of an S-box can be significantly reduced in achieving the same routability compared to the conventional single-level based S-box designs. The results seem to point out a new avenue for designing new FPGA routing structures breaking beyond the conventional boundary between S-boxes and connection boxes (e.g. by merging the extension level of the proposed extended S-box with the neighboring connection boxes). Meanwhile, the trade-offs between the number of manufactured switches and signal path delays attributed to the multi-level structures would be an important issue too. This will be our future focus of investigation.

We also note that the two-level construction of S-boxes provides more freedom for designers. We may not need full extension if we do not want perfect mappability, this way we will have various S-boxes for various purpose. We also point out that it is important to investigate Problem (2).

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