BBE: Hierarchical Computation of 3-D Interconnect Capacitance with BEM Block Extraction*

Taotao Lu ,Zeyi Wang ,XianLong Hong Dept. Of Computer Science and Technology, Tsinghua University Beijing 100084, P.R. China

email lutt98@mails.tsinghua.edu.cn

Abstract— Fast and accurate interconnect parasitic parameter extraction has become increasingly critical for verification and analysis in VLSI today. In this paper, a fast hierarchical extraction approach based on Boundary Element Method (BEM) is presented for 3-D parasitic capacitance computation. Hierarchical partition of the 3-D field creates many parts which are called 3-D BEM blocks. After combining all the 3-D BEM blocks, the capacitance matrix for a given set of nets can be computed by applying the boundary conditions. Numerical results shows that this method performs many times faster than the 3-D field solver, with equal accuracy.

I. INTRODUCTION

With advancing IC technology, feature size has decreased very quickly. The clock frequency is the key determinant of performance for most IC. The interconnect is a dominant factor in system delay and signal integrity [6]. For timing verification, parasitic parameter extraction is the most critical step, which is needed to be fast and accurate enough in full chip verification.

Currently, none of the full chip extraction tools can guarantee high accuracy. They use the 2-D or quasi-3D model to compute the capacitance based on the geometrical characteristics of the interconnects[3][5][7]. These methods are fast but inaccurate, especially for the coupling capacitance as the interconnect structures become more and more complex.

The field solver with numerical methods can guarantee high accuracy whatever the complexity of the interconnect. But they are slow. Many acceleration methods have been published these years[2][12][13]. However, almost all kinds of field solvers use the flat extraction method. Hierarchical methods have been widely used in VLSI design, such as the hierarchical placement and route, etc. But in parasitic parameter extraction, almost all of the tools invoke the flat extraction methods. That is because the parasitic parameters are always relative to the environment of the interconnects[4]. The advantage of the hierarchical method can't be used in the extraction. [8][11] presented one hierarchical extraction method in 2-D cross section using the macromodel in the extraction of the in-

terconnect capacitance. This proved that it is feasible to use hierarchical methods in parameter extraction. However, [8] and [11] only compute the capacitance of the 2-D cross section. Such a method cannot guarantee high accuracy of computation for 3-D interconnect structures which are more complex than 2-D cross sections.

In this paper, a hierarchical extraction method for 3-D interconnect capacitance, called BBE, is presented. In the BBE method, the 3-D structure is partitioned into several blocks that are called 3-D BEM blocks when using Boundary Element Method (BEM). When solving the Laplace equation in the 3-D BEM block, the Boundary Capacitance Matrix (BCM), which is a new concept presented in this paper, is computed instead of the Real Capacitance Matrix (RCM) because there is not enough boundary conditions to get the RCM in the BEM block. Every 3-D BEM block can be combined with its adjacent one to form the BCM of a bigger field. After combination of all the BEM blocks, the BCM can be turned into the final capacitance matrix after applying all the boundary conditions. Such an method based on 3-D BEM block is a hierarchical approach, which can be used for the large size computation easily.

The rest of this paper is organized as follows. In section 2, the 3-D capacitance extraction is introduced briefly. In section 3, the Boundary Capacitance Matrix is introduced together with the Real Capacitance Matrix. In section 4, one hierarchical method using 3-D BEM block is presented to compute the capacitance of the real layout. Some numerical results are listed with some discussions in section 5. Finally the conclusion is given.

II. INTRODUCTION OF 3-D CAPACITANCE EXTRACTION

The parasitic capacitance extraction can be turned into solving the Laplace equation with mixed boundary conditions. In 3-D domain $\Omega = \bigcup_{k=1}^{M} \Omega_k, (k = 1, ..., M)$, the electrical potential distribution is governed by the Laplace equations with three types of boundary conditions, which are the Dirichlet Boundary condition (DBC on Γ_u), Neumann Boundary condition

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(NBC on Γ_q) and Interface Boundary condition (IBC on Γ_I).

$$\begin{cases} \varepsilon_k \nabla^2 u = \varepsilon_k (\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + \frac{\partial^2 u}{\partial z^2}) = 0 & on\Omega_k, (k = 1, \dots, M) \\ u = \overline{u} & on\Gamma_u \\ q = \frac{\partial u}{\partial \mathbf{n}} = \overline{q} = 0 & on\Gamma_q \\ \varepsilon_a \cdot \frac{\partial u_a}{\partial \mathbf{n}_a} = \varepsilon_b \cdot \frac{\partial u_b}{\partial \mathbf{n}_b}, u_a = u_b & on\Gamma_I \end{cases}$$
(1)

Usually, the coupling capacitance C_{ij} between conductor *i* and *j* is:

$$C_{ij} = -Q_i/V_{ji} \tag{2}$$

where V_{ji} is the voltage between conductor *j* and *i*, and Q_i is the induced charge of conductor *i* which can be obtained from:

$$Q_i = \int_{\Gamma_i} \boldsymbol{\varepsilon} \cdot \frac{\partial \boldsymbol{u}}{\partial \mathbf{n}} d\Gamma \tag{3}$$

where Γ_i is the surface of conductor *i*, ε is the dielectric's permittivity, $\partial u/\partial \mathbf{n}$ is the normal intensity of electrical field which can be obtained by solve the Laplace equation Eq.(1).

III. BOUNDARY CAPACITANCE MATRIX (BCM) AND REAL CAPACITANCE MATRIX (RCM)

Usually there is coupling capacitance between each two conductors. So there is one capacitance matrix with size $n \times n$ among *n* conductors. This matrix is called "**Real Capacitance Matrix(RCM)**" in this paper. One new concept called "**Boundary Capacitance Matrix(BCM)**" is presented here in the hierarchical computation of 3-D capacitance using BEM.

A. Introduction of Boundary Capacitance Matrix(BCM)

Using BEM, the Laplace Equation Eq.(1) can be transferred into the Direct Boundary Integration Equation(DBIE)[1] in the 3-D field Ω as follows:

$$0.5u + \int_{\partial \Omega_k} q^* u d\Gamma = \int_{\partial \Omega_k} u^* q d\Gamma, \quad (k = 1, 2, \dots, M)$$
(4)

where $u^*(s,t) = \frac{1}{4\pi r(s,t)}$ is the fundamental solution of the Laplace equation. **n** is the outward normal direction on the boundary. $q^* = \partial u^* / \partial \mathbf{n}$. $\partial \Omega_k$ is the boundary of *k*th dielectric domain Ω_k .

To solve the Eq.(4), the boundary $\partial \Omega_k (k = 1, ..., M)$ should be divided into boundary elements. If the element interpolation function is constant, the Eq.(4) can be written by:

$$0.5u_{i}^{k} + \sum_{j=1}^{N_{k}} u_{j}^{k} \int_{\Gamma_{j}^{k}} q^{*} d\Gamma = \sum_{j=1}^{N_{k}} q_{j}^{k} \int_{\Gamma_{j}^{k}} u^{*} d\Gamma, \quad (i = 1, \dots, N_{k}) \quad (5)$$

where, Γ_j^k is the *jth* boundary element on $\partial \Omega_k$. u_j^k and q_j^k is the potential and the flux on Γ_j^k . After computation of the integration in Eq.(5), it can be written as:

$$\sum_{j=1}^{N_k} H_{ij}^k u_j^k = \sum_{j=1}^{N_k} G_{ij}^k q_j^k, \ (i = 1, \dots, N_k, \ k = 1, \dots, M).$$
(6)

where $H_{ij}^k = \begin{cases} \int_{\Gamma_j^k} q^* d\Gamma & \text{when } i \neq j \\ \int_{\Gamma_j^k} q^* d\Gamma + 0.5 & \text{when } i = j \end{cases}$ and $G_{ij}^k = \int_{\Gamma_j^k} u^* d\Gamma$.

Eq.(6) can be written in the the matrix form as follows:

$$HU = GQ \tag{7}$$

If the matrix G is nonsingular, let

$$C = G^{-1}H \tag{8}$$

This matrix *C* contains all the boundary elements on three kinds of boundary: Γ_u , Γ_q and Γ_I in Eq.(1).

Those variables on the boundary Γ_I can be eliminated using the IBC. So the matrix *C* can be transferred into matrix C_m which only contains the elements on boundary Γ_u and Γ_q . Such a matrix C_m is called the **Boundary Capacitance Matrix(BCM)** of the field Ω . Then according to Eq.(7), the following formula is obtained:

$$C_m U_m = Q_m \tag{9}$$

where U_m is the potential vector of those elements on Γ_u and Γ_q , and Q_m is the flux vector on them.

B. Computation of BCM

B.1 BCM of the 3-D Field with Single Dielectric

In the 3-D field with single dielectric, there are only two kinds of boundaries: DBC and NBC. The matrix *C* in Eq.(8) only contains those elements on boundary Γ_u and Γ_q . So this matrix *C* is exactly the BCM of the field.

B.2 BCM of the 3-D Field with Multi Dielectrics

In the field with multi dielectrics, those variables in the boundary with IBC should be eliminated.



Fig. 1. 3-D fields with two dielectrics

First, let's consider one simple example with only two dielectrics as shown in Fig.1. Using BEM, the Eq.(4) is satisfied in both fields with dielectric 1 and 2 separately. In dielectric 1, the following formula can be obtained based on BEM:

$$\begin{bmatrix} C1_{iner,iner} & C1_{iner,int} \\ C1_{int,iner} & C1_{int,int} \end{bmatrix} \begin{bmatrix} U1_{iner} \\ U1_{int} \end{bmatrix} = \begin{bmatrix} Q1_{iner} \\ Q1_{int} \end{bmatrix}$$
(10)

where the subscript *int* denotes the nodes in the interface, and the subscript *iner* denotes the others. Similarly, in dielectric 2,the following formula is obtained:

$$\begin{bmatrix} C2_{iner,iner} & C2_{iner,int} \\ C2_{int,iner} & C2_{int,int} \end{bmatrix} \begin{bmatrix} U2_{iner} \\ U2_{int} \end{bmatrix} = \begin{bmatrix} Q2_{iner} \\ Q2_{int} \end{bmatrix}$$
(11)

On the interface of two dielectrics, the boundary condition IBC should be satisfied, which means:

$$\begin{cases} U1_{int} = U2_{int} \\ \varepsilon_1 Q1_{int} + \varepsilon_2 Q2_{int} = 0 \end{cases}$$
(12)

We multiply both side of Eq.(10) by ε_1 , and multiply both side of Eq.(11) by ε_2 . Using Eq.(12),we can get:

$$\begin{bmatrix} C1_{iner,iner} & 0 & C1_{iner,int} \\ 0 & C2_{iner,iner} & C2_{iner,int} \\ \epsilon_1 C1_{int,iner} & \epsilon_2 C2_{int,iner} & \epsilon_1 C1_{int,int} - \epsilon_2 C2_{int,int} \end{bmatrix}$$

$$\begin{bmatrix} U1_{iner} \\ U2_{iner} \\ U1_{int} \end{bmatrix} = \begin{bmatrix} Q1_{iner} \\ Q2_{iner} \\ 0 \end{bmatrix}$$

$$(13)$$

Eliminating the $U1_{int}$ in Eq.(13), we can obtain:

$$CmU = Q \tag{14}$$

$$Cm = Z1 - Z2 \bullet Z3^{-1} \bullet Z4 \tag{15}$$

$$Z1 = \begin{bmatrix} C1_{iner,iner} & 0\\ 0 & C2_{iner,iner} \end{bmatrix}$$

$$Z2 = \begin{bmatrix} C1_{iner,int}\\ C2_{iner,int} \end{bmatrix}$$

$$Z3 = [\varepsilon_1 C1_{int,int} - \varepsilon_2 Cm2_{int,int}]$$

$$Z4 = [\varepsilon_1 C1_{int,iner}, \varepsilon_2 C2_{int,iner}]$$
(16)

and $U = \begin{bmatrix} U1_{iner} \\ U2_{iner} \end{bmatrix}$, $Q = \begin{bmatrix} Q1_{iner} \\ Q2_{iner} \end{bmatrix}$. Eq.(15) is the BCM of the 3-D field with two dielectrics.

In the field with multi dielectrics, the BCM can be obtained similar as in the field with two dielectrics.

C. From BCM to RCM

The BCM obtained by BEM is satisfied as follows:

$$\begin{bmatrix} C_{dd} & C_{dn} \\ C_{nd} & C_{nn} \end{bmatrix} \begin{bmatrix} U_d \\ U_n \end{bmatrix} = \begin{bmatrix} Q_d \\ Q_n \end{bmatrix}$$
(17)

where the subscript *d* denotes the nodes with DBC, and the subscript *n* denotes the nodes with NBC. Then the boundary conditions should be used. Normally, in the boundary with NBC, the flux is set to 0. In Eq.(17), let $Q_n = 0$. Then

$$C_{nd}U_d + C_{nn}U_n = Q_n = 0 \tag{18}$$

$$U_n = -C_{nn}^{-1}C_{nd}U_d \tag{19}$$

In Eq.(17), we get:

$$C_{dd}U_d + C_{dn}U_n = Q_d \tag{20}$$

Put Eq.(19) into Eq.(20), then:

$$[C_{dd} - C_{dn}C_{nn}^{-1}C_{nd}]U_d = Q_d$$
(21)

Let $C = C_{dd} - C_{dn}C_{nn}^{-1}C_{nd}$, which contains only the elements on Γ_u . The nodes which belong to the same conductor can be condensed into only one node. So this matrix can be changed into the Real Capacitance Matrix.

Therefore, if the BCM of the whole field can be computed, the RCM will be obtained easily using the boundary condition NBC. In the next part, one hierarchical capacitance extraction approach is presented based on it.

IV. HIERARCHICAL COMPUTATION APPROACH USING 3-D BEM BLOCK

One 3-D field can be partitioned into several sub-regions through many different ways. Then the computation of the whole 3-D field can be turned into that of the 3-D sub-regions. Those sub-regions are called 3-D BEM blocks when it is solved by BEM.

In this section, one fast approach is presented to compute the RCM of the whole 3-D field using the 3-D BEM blocks. It has following four steps:

step1. Hierarchical partition of the 3-D field into 3-D BEM blocks.

step2. Computation of the BCM in each BEM block.

step3. Hierarchical combination of the BCM in all the BEM blocks.

step4. Computation of the RCM from the BCM.

A. Hierarchical Partition of the 3-D field

Currently, the 3-D interconnect structure is usually generated by the 2-D geometries from the layout and the design process technology[14]. 2-D geometries include the information of interconnect, such as the shape, the layer number, etc. The process technology is used to describe the cross-section structure, such as the thickness of the interconnect, the thickness of the oxide, etc. The 3-D interconnect structure can be generated with the geometry and process technology as shown in Fig.2.



Fig. 2. Generation of 3-D structure by combination of 2-D geometries and process technology in Real Layout

Currently, almost all the interconnect structure is the layer structure. The whole 3-D field can be divided into several parts in the high direction according to the process technology. For each layer, all the 2-D interconnect geometries can be divided into $m \times n$ blocks, as shown in Fig.3.



Fig. 3. Partition of the 2-D interconnect geometry in one layer

The geometries of interconnect are clipped by all the blocks. For each block, one 3-D structure can be generated according to the corresponding process technology of the layer. Such a 3-D structure forms one 3-D BEM block. After the partition of the 2-D interconnect geometries of all the layers, the 3-D BEM blocks are generated.

B. Organization of the Partition

In order to get a convenient and effective partition, the hierarchical binary tree is invoked to make the organization as shown in Fig.4.



Fig. 4. Hierarchical organization of the partition

One hierarchical binary tree can be built for the partition. If we use the full binary tree, the original region should be divided into 2^n parts, where the *n* is the depth of the tree. Each leaf of the tree stands for one block of the original region. Thus, each leaf can build one 3-D BEM block with the process technology. Using BEM, the BCM of each BEM blocks can be computed. Then the BCM of each non-leaf node of the tree is the combination of the BCM of its two children node. Finally, the BCM of the root node is obtained, the whole computation is completed. This proceed can be easily implemented using the Postorder Traversal of the binary tree. Next, it will be presented on how to combine the BCM of two adjacent 3-D BEM blocks.

C. Combination of 3-D BEM blocks

Let's consider one field Ω which is partitioned into only two BEM blocks Ω_1 and Ω_2 as shown in Fig.5.



Fig. 5. One field cut into two BEM blocks Ω_1 and Ω_2

When combining two BEM blocks, the boundary condition IBC should be satisfied on the interface of two BEM blocks. In our partition, we have an assumption first: **Two sides of the interface always have the same physical property.** That means the permittivities of two sides of the interface are always same. This assumption can be guaranteed easily in the partition.

The BCM of the two 3-D BEM blocks is supposed to be Cm1 and Cm2. The subscript *i* denotes those nodes in the interface which should satisfy the boundary condition IBC, and *d* denotes those with boundary condition DBC, and *n* denotes those with boundary condition NBC. The BCM Cm1 satisfies follows:

$$\begin{bmatrix} Cm1_{dd} & Cm1_{dn} & Cm1_{di} \\ Cm1_{nd} & Cm1_{nn} & Cm1_{ni} \\ Cm1_{id} & Cm1_{in} & Cm1_{ii} \end{bmatrix} \begin{bmatrix} U1_d \\ U1_n \\ U1_i \end{bmatrix} = \begin{bmatrix} Q1_d \\ Q1_n \\ Q1_i \end{bmatrix}$$
(22)

where the subscript dd means the interaction of the elements with the boundary condition DBC and DBC. And the subscript dn, di, etc, has the similar meaning. The BCM Cm2 satisfies the following:

$$\begin{bmatrix} Cm2_{dd} & Cm2_{dn} & Cm2_{di} \\ Cm2_{nd} & Cm2_{nn} & Cm2_{ni} \\ Cm2_{id} & Cm2_{in} & Cm2_{ii} \end{bmatrix} \begin{bmatrix} U2_d \\ U2_n \\ U2_i \end{bmatrix} = \begin{bmatrix} Q2_d \\ Q2_n \\ Q2_i \end{bmatrix}$$
(23)

According to the boundary condition IBC and our assumption, the following should be satisfied:

$$\begin{cases} U1_i = U2_i \\ Q1_i + Q2_i = 0 \end{cases}$$
(24)

Putting Eq.(24) into Eq.(22) and Eq.(23), we can get:

$$\begin{bmatrix} Cm1_{dd} & Cm1_{dn} & 0 & 0 & Cm1_{di} \\ Cm1_{nd} & Cm1_{nn} & 0 & 0 & Cm1_{ni} \\ 0 & 0 & Cm2_{dd} & Cm2_{dn} & Cm2_{di} \\ 0 & 0 & Cm2_{nd} & Cm2_{nn} & Cm2_{ni} \\ Cm1_{id} & Cm1_{in} & Cm2_{id} & Cm2_{in} & Cm1_{ii} - Cm2_{ii} \end{bmatrix} \begin{bmatrix} U1_d \\ U1_n \\ U2_d \\ U2_n \\ U1_i \end{bmatrix} = \begin{bmatrix} Q1_d \\ Q1_n \\ Q2_d \\ Q2_n \\ 0 \end{bmatrix}$$
(25)

Eliminating the $U1_i$ of Eq.(25), we can obtain:

$$CmU = Q \tag{26}$$

$$Cm = D1 - D2 * D3^{-1} * D4 \tag{27}$$

$$D1 = \begin{bmatrix} Cm1_{dd} & Cm1_{dn} & 0 & 0\\ Cm1_{nd} & Cm1_{nn} & 0 & 0\\ 0 & 0 & Cm2_{dd} & Cm2_{dn}\\ 0 & 0 & Cm2_{nd} & Cm2_{nn} \end{bmatrix}$$

$$D2 = \begin{bmatrix} Cm1_{di}\\ Cm1_{ni}\\ Cm2_{di}\\ Cm2_{ni} \end{bmatrix}, \quad D3 = [Cm1_{ii} - Cm2_{ii}]$$

$$D4 = \begin{bmatrix} Cm1_{id} & Cm1_{in} & Cm2_{id} & Cm2_{in} \end{bmatrix}$$

$$U = \begin{bmatrix} U1_{d}\\ U1_{n}\\ U2_{d}\\ U2_{n} \end{bmatrix} Q = \begin{bmatrix} Q1_{d}\\ Q1_{n}\\ Q2_{d}\\ Q2_{n} \end{bmatrix}$$

$$(28)$$

The Eq.(26) is just the BCM of the combination with BEM block Cm1 and Cm2.

D. Flow of the Algorithm

The global program flow of the hierarchical approach to compute the capacitance for real layout is shown as in Fig.6.

V. NUMERICAL RESULTS

In this section, the BBE method is used to analyze one simple 3-D structures first whose results are compared with those in [9] and [10]. Then, 89 3-D cases cut from the real layout are used to depict the performance of BBE method, whose computational results are compared with the 3-D field solver software "RAPHAEL".

A. One Simple 3-D structures

The structure is shown in Fig.7. The size of every straight line is $1 \times 1 \times 13$, the gap between conductor 3 and 4, as well as conductor 5 and 6, is 3. The distance between the straight line and the border is 4. The size of the cross section of every bend is 1×1 , other geometric parameters of the bends are shown in Fig.8. Counted from the bottom, the thickness of every



Fig. 6. Flow of the program



Fig. 7. One simple 3-D structure.



Fig. 8. Top view of the layer with bends in Fig. 11, a=b=13, S1=3.5, S2=3.

dielectric layer is 1, 1, 2, 1, 1, 1 and 1. All length parameters above are in unit of mm. The relative permittivity of every layer is 2, 3, 3, 4, 4, 5 and 5.

We have calculated the capacitance matrix by BBE method, and the corresponding results of SpiceLink and ODDM are provided by [10]. Only $C_{11}, C_{22}, C_{44}, C_{66}$ are listed in Table I. The discrepancy among the results obtained with three methods is within 2%. In the BBE method, 8×8 partition is applied. In Sun Unltra-Sparc 20, the CPU time and memory size used by these methods are shown in Table I. BBE method is about 300 times faster than SpiceLink, and about 30 times faster than ODDM. The memory used by BBE is similar than that used by ODDM, which is much smaller than that used by SpiceLink.

TABLE I

CAPACITANCE FROM THE SPICELINK. ODDM AND BBE									
	C_{11}	C_{22}	C_{44}	C_{66}	Time(s)	Mem(MB)			
SpiceLink	0.669	1.29	1.54	2.53	1327	75.9			
ODDM	0.680	1.29	1.52	2.54	122	2.7			
BBE	0.673	1.33	1.58	2.52	3.7	2.52			

B. 89 Cases From the Real Layout

89 3-D cases from the real layout are tested. All the tests run on Sun Ultra E450, 233MHz. We compute the Real Capacitance Matrix in each cases. The capacitance reference value is calculated by "RAPHAEL", whose results are often regarded as the golden value by industry.

The average result is shown in Table.II. The computation time is of extraction about 15 nets together in average. The numerical results show that BBE is much faster than the normal field solvers. And its accuracy are as high as the field solver. Therefore, it can be used well in full-chip extraction with field solution accuracy.

 TABLE II

 TIME AND ACCURACY COMPARISON OF BETWEEN BBE AND RAPHAEL

Raphael	BBE Avg. Time		BBE Diff.			
Time(s)	Time(s)	Speed-up	Avg.	Max.	Std*.	•
32082	12	2674	2.4%	6.5%	3.5%	•

*Std. means the Standard Deviation.

VI. CONCLUSION

In this paper, a hierarchical approach, BBE is presented for capacitance extraction. The following key features are used:

- Hierarchical partition of the 3-D domain.
- The generation of BCM in each BEM block.
- The combination of BCM to get the final RCM.

The numberical results show that it is very suitable to use the hierarchical method in the fast RC extraction with high accuracy in large scale design. Furthermore, it is possible to take the Reuse technology while using BEM blocks in the hierarchical approach, which is possible to make full-chip extraction.

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