Temperature-Independence-Point Properties for 0.1μm-Scale Pocket-Implant Technologies and the Impact on Circuit Design

K. Hisamitsu, H. Ueno, M. Tanaka, D. Kitamaru, M. Miura-Mattausch, [1]H. J. Mattausch,
[2]S. Kumashiro, [2]T. Yamaguchi, [2]K. Yamashita, and [2]N. Nakayama
Graduate School of Advanced Sciences of Matter, [1]Research Center for Nanodevices and Systems,
Hiroshima University, 1-3-1, Kagamiyama, Higashi-Hiroshima, 739-8526, Japan
[2]Semiconductor Technology Academic Research Center,
3-17-2, Shin-Yokohama, Kanagawa, 222-0033, Japan

Abstract— The temperature-independence point (TIP) of the drain current for MOS transistors in a 0.1μm-scale pocket-implant technology is gate-length (L_g) dependent and has different magnitudes for n-MOSFET and p-MOSFET. Circuits such as ring-oscillators have a TIP, lying between the values for n- and p-MOSFET. The circuit TIP is close to the n-MOSFET TIP for long L_g and gets closer to the p-MOSFET TIP for short L_g. The reason is the different temperature dependence of electron and hole mobility as a function of L_g. Due to the high field effect, oscillation periods of ring-oscillators with short L_g hardly improve, when the supply voltage is raised beyond the TIP. Therefore, an advantageous supply-voltage (V_{DD}) choice for pocket-implant technologies is near the TIP of circuits, allowing a favorable combination of short switching delay and minimized temperature dependence. By designing the $V_{th,p}$ closer to $V_{th,n}$, not only the low power dissipation, due to the reduction of the TIP, but also the suppressed TIP fluctuation can be realized.

I. Introduction

It has been observed that the delay characteristics of ring-oscillators for different temperatures cross at certain applied voltages (V_{DD}). We call the voltage point, at which the temperature dependence vanishes, the temperature-independence point (TIP). The importance of the TIP has been recognized since long time for analog designs, where minimized temperature dependence is often desired. The TIP is generally expected to occur at the rather high voltage of 1.2V [1]. An instability concern for low-voltage LSIs with a V_{DD} lower than 1.2V has thus recently been raised, because such LSIs would have to operate in the region of a positive temperature coefficient [2]. Fig. 1 compares oscillation periods of ring-oscillators fabricated with two different gate lengths (L_g) in a 0.1μm technology for various temperatures. As can be seen in Fig. 1 the TIP is in general small enough to relieve instability concerns for low-voltage designs contrary to the previous result [2].

However, two additional features are obvious from our measurement:

1) The ring-oscillator TIP for short L_g is higher than that for long L_g.
2) Contrary to long L_g, the oscillation period is hardly improved under the $V_{DD} >$ TIP condition for the short L_g.

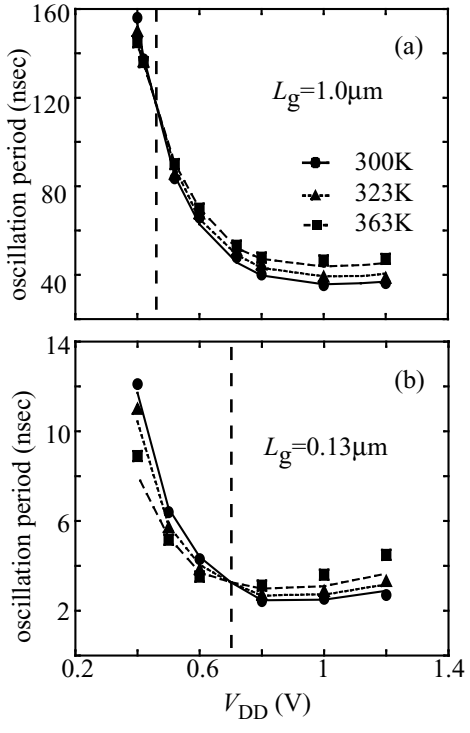

Fig. 1. Measured (symbols) and simulated (lines) oscillation period of a ring-oscillator with 31 inverter stages. (a) $L_g = 1.0\mu$m, (b) $L_g = 0.13\mu$m. The vertical lines indicate the TIP.

Since the TIP-variation as a function of L_g is undesirable for circuit design, we have analyzed the TIP properties of a ring-oscillator together with those of n- and p-MOSFETs by measurements and simulation for a 0.1μm-scale CMOS technology with pocket-implants [3]. We report here that the origin of the TIP variation with L_g is a different temperature-dependence of n- and p-MOSFETs as a function of L_g. This is caused by a different temperature dependence of electron and hole mobility. The saturation of the oscillation period for increasing V_{DD} is also explained by the mobility characteristics.

II. Characteristics of the Temperature-Independence Point (TIP)

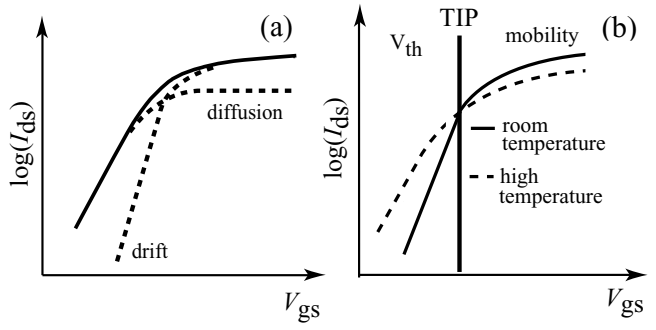

Fig. 2. (a) Drift- and diffusion components of I_{ds} as a function of the gate voltage (V_{gs}); (b) Schematic temperature dependence of *I-V* characteristics. A region with minimized temperature dependence and a temperature independence point (TIP) exist due to the different signs of the temperature coefficients of the current components.

The source-drain current (I_{ds}) of MOSFETs is well known to consist of a drift-component (I_{ds}(drift)) and a diffusion component (I_{ds}(diff)), which have different temperature coefficients and are dominant in different operating regions [4]. I_{ds}(diff) dominates in the sub-threshold and weak-inversion region, as shown in Fig. 2a. It has a positive temperature coefficient due to the bandgap narrowing, and therefore induces a threshold-voltage (V_{th}) decrease with increasing temperature. On the other hand, I_{ds}(drift) dominates in the main part of the linear region as well as in the saturation region and has a negative temperature coefficient. The reason is a carrier mobility decrease with temperature due to an increased phonon scattering. Consequently, the overall temperature dependence of I_{ds}, schematically shown in Fig. 2b, has an intermediate region of minimized temperature dependence.

V_{th} of n- and p-MOSFET ($V_{th,n}$, $V_{th,p}$) are designed to be 0.17V and 0.30V for long $L_g = 1.0\mu$m as well as 0.30V and 0.38V for short $L_g = 0.13\mu$m at room temperature. Fig. 3a and b show the temperature dependence of the I_{ds}-V_{gs} characteristic of n- and p-MOSFET for $L_g = 1.0\mu$m at V_{ds}=1.0V. Fig. 4a and b show this temperature dependence for $L_g = 0.11\mu$m. The TIP is clearly observed for all cases, but occurs at different V_{gs} values. It ranges 0.45V – 0.57V for n-MOSFETs and 0.68V – 0.71V for p-MOSFETs for changed L_g. Lines show the simulation results with the drift-diffusion model for circuit simulation HiSIM (Hiroshima-university STARC IGFET Model) [5, 6], which reproduce the measured temperature and L_g-dependence of the TIP with good accuracy. Fig. 5 shows extracted TIP with the help of HiSIM and measured V_{th}. It is seen that TIPs are at about a factor 2 to 2.5 above V_{th}. Fig. 6 summarizes the L_g-dependence of the TIP for n- and p-MOSFET as well as the ring-oscillator. The analyzed ring-oscillator circuits consist of 31 inverter stages with a width (W_g) of 5μm and 10μm for n- and p-MOSFETs. The reproducibility of the oscillation period with HiSIM is demonstrated in Fig. 1. The increase of the MOSFET TIP with decreasing L_g for both MOSFET types is attributed mainly to the V_{th}-increase due to

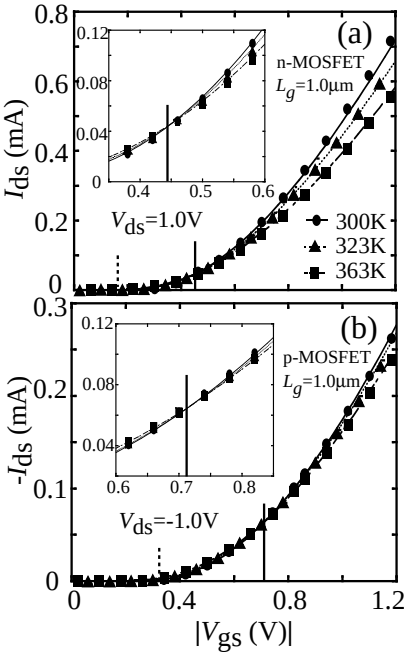

Fig. 3. Temperature dependence of the *I-V* curves of (a) n-MOSFET ($W_g = 5\mu$m) (b) p-MOSFET ($W_g = 10\mu$m) as a function of the gate voltage (V_{gs}) for $L_g = 1.0\mu$m. Measured data (symbols) and simulated data with HiSIM (lines) are shown. The vertical solid and dashed lines indicate the TIP and $V_{th}(T = 300\text{K})$, respectively.

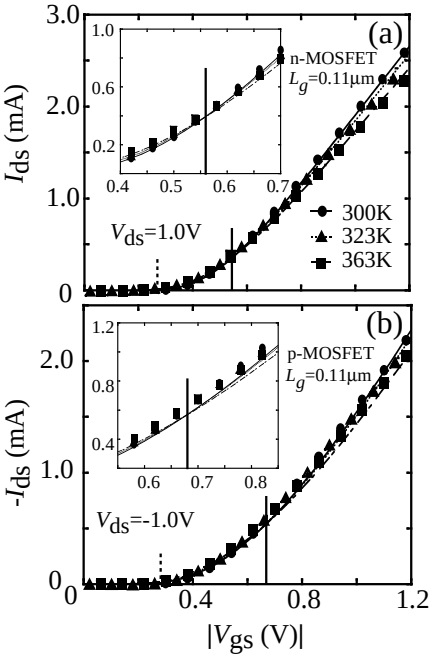

Fig. 4. The same figures as Fig. 3 but for $L_g = 0.11\mu$m.

the reverse-short-channel effect (RSCE) caused by the pocket implantation. Fig. 7 shows the simulation result for an equivalent non-pocket technology. TIP of n- and p-MOSFET don't increase with smaller L_g in Fig. 7, which confirms our argument.

Fig. 6 shows also a continuous increase of the ring-oscillator TIP with decreasing L_g from about 0.45V for $L_g = 1.0\mu$m

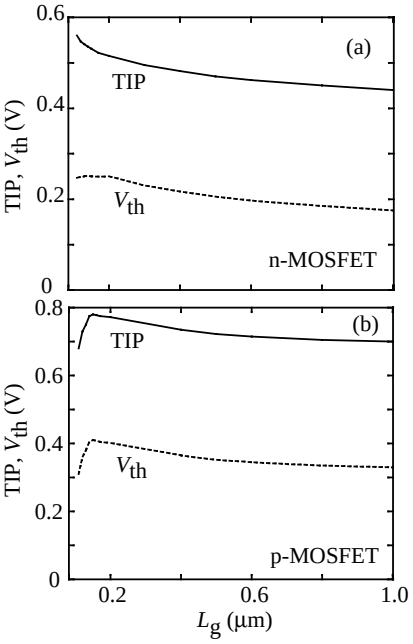

Fig. 5. Extracted TIP with the help of HiSIM and measured V_{th} as a function of L_g. (a) n-MOSFET, (b) p-MOSFET. V_{ds} is fixed to be 1.0V for the V_{th} measurement.

to 0.70V for $L_g = 0.13\mu$m. The ring-oscillator TIP is near to the n-MOSFET TIP for long $L_g = 1.0\mu$m. For shorter L_g it changes its relative position and gets close to the p-MOSFET TIP at $L_g = 0.13\mu$m. This suggests that we have a change from an n-MOSFET domination at long L_g to a strong p-MOSFET contribution at short L_g. The V_{ds} dependence of the TIP is very small as verified in Fig. 8 for n-MOSFETs of short and long L_g as a function of V_{ds}. After a small increase at the beginning the TIP saturates to a constant value above $V_{ds} = 0.25$V. Therefore we can exclude the responsibility of the short-channel effect for the change from n-MOSFET to p-MOSFET domination here.

Fig. 9 shows that the normalized I_{ds} with the channel length decreases by more than a factor 2 for the n-MOSFET, while it remains almost constant for the p-MOSFET, when L_g is reduced from 1.0μm to 0.13μm. For the investigation V_{ds} is fixed to 1V and V_{gs} is selected to give the strong inversion. The reason for the I_{ds} reduction of the n-MOSFET is attributed to the strong electron mobility degradation with decreasing L_g due to the higher lateral electric field, induced along the channel (see Fig. 10). The μ_{eff} is characterized by two steps; the low field mobility μ_0 and the high field contribution.

$$\mu_{eff} = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_y}{v_{sat}}\right)^2\right)^{1/2}} \quad (1)$$

$$\mu_0 = \left(\frac{1}{\mu_{Coulomb}} + \frac{1}{\mu_{phonon}} + \frac{1}{\mu_{roughness}}\right)^{-1} \quad (2)$$

where E_y, v_{sat}, $\mu_{Coulomb}$, μ_{phonon} and $\mu_{roughness}$ represent lateral electric field, saturation velocity, mobility due to Coulomb scattering, phonon scattering and surface roughness scattering,

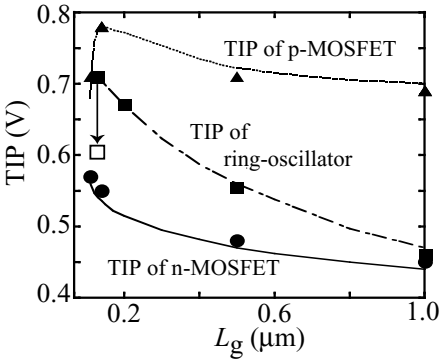

Fig. 6. Measured (symbols) and simulated (lines) temperature-independence points (TIP) of n-and p-MOSFET as well as a ring-oscillator circuit as a function of L_g. Simulations are with HiSIM. V_{ds} of single-MOSFETs is fixed to be 1.0V for the V_{th} measurement.

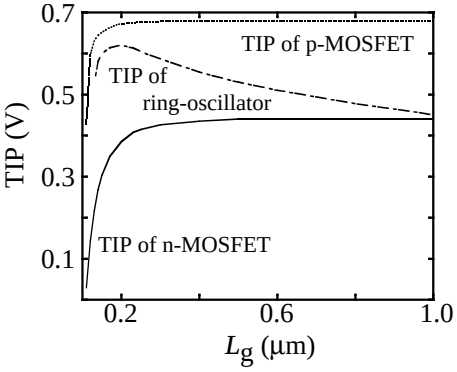

Fig. 7. Simulated TIP-dependence on L_g for transistors with removed pocket implantation. Otherwise transistor data is the same as for Fig. 6.

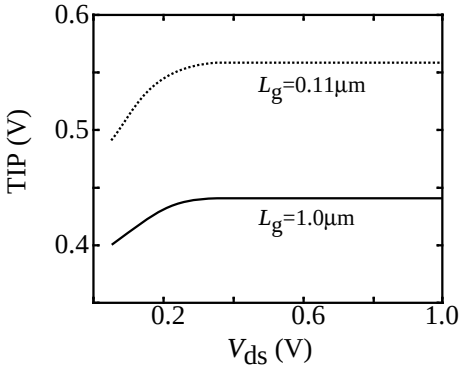

Fig. 8. Drain voltage (V_{ds}) dependence of the TIP for n-MOSFETs under the same bias condition as Fig. 8. The calculation is done with HiSIM.

respectively. The temperature dependence is mainly induced by the phonon scattering in μ_0. Thus the mobility μ_{eff} under high field is strongly suppressed in comparison to the low field mobility μ_0 as demonstrated for the n-MOSFET in Fig. 11. A Monte Carlo simulation result shown in Fig. 12 confirms also the characteristics of the mobility. Namely, in the channel region where the field is not so high, the temperature dependence of the mobility in n-MOSFET is obvious. Whereas it is diminished in the high field region at the drain side. This is also responsible for the observed smaller temperature dependence of n-I_{ds} at short L_g in Fig. 9. On the contrary, the p-MOSFET

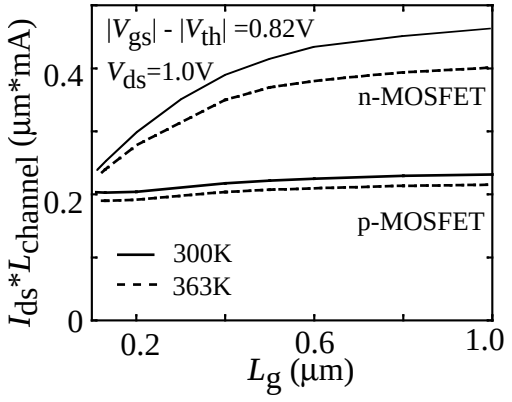

Fig. 9. Measured I_{ds} normalized with the channel length ($L_{channel}$) as a function of L_g. W_g is fixed to 10μm for both cases.

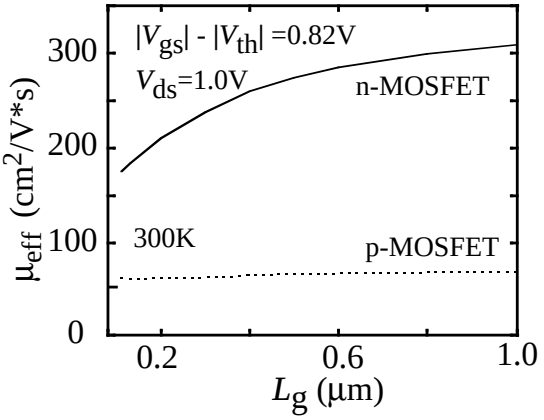

Fig. 10. Extracted mobility values with HiSIM as a function of L_g for n- and p-MOSFET.

mobility is equally low along the whole channel, and shows the weak temperature dependence for all L_g.

For long L_g the temperature dependence of n-I_{ds} is much larger than that of p-I_{ds} (see Fig. 9), which explains the n-MOSFET determination of the ring-oscillator TIP in Fig. 6. For short L_g the temperature dependence of n-I_{ds} and p-I_{ds} become approximately equal. Therefore, the ring-oscillator TIP is expected to be in the middle of the n- and p-MOSFET TIPs. The determination of the ring-oscillator TIP by the p-MOSFET is mainly due to the low inverter-switching threshold, demonstrated in Fig. 13 by a solid circle. This low inverter-switching threshold is caused by a smaller $V_{th,n}$ in comparison to the $V_{th,p}$. Indeed, the inverter switching-threshold rises if we choose the same $V_{th,p}$ for n-and p-MOSFET, as shown in Fig. 13 by an open circle, and the TIP of the ring-oscillator moves closer to $V_{DD}/2$ as shown in Fig. 6 by an open box with an arrow.

III. Discussion

Important is the fact that the delay hardly improves beyond the TIP for $L_g = 0.13\mu$m, while the improvement is still substantial for $L_g = 1.0\mu$m. This is attributed to the high-field effect for short L_g, which prevents further carrier velocity increase as applied voltage becomes larger. Our observations

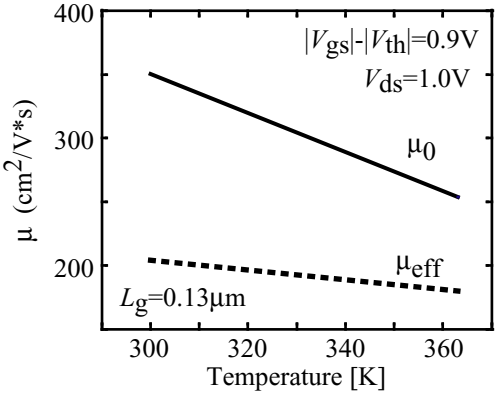

Fig. 11. Extracted mobility values of an n-MOSFET with HiSIM as a function of temperature.

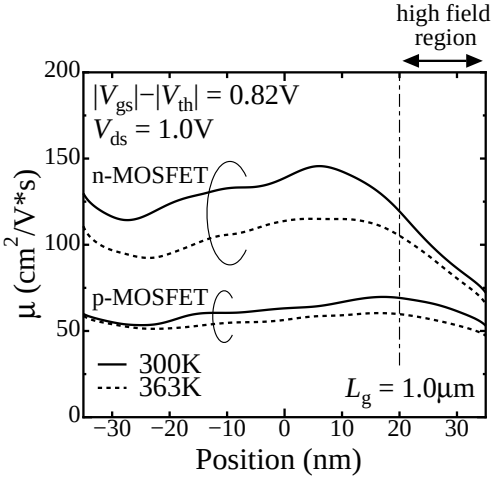

Fig. 12. Mobility vs. position in the channel characteristics simulated by a Monte Carlo device simulator.

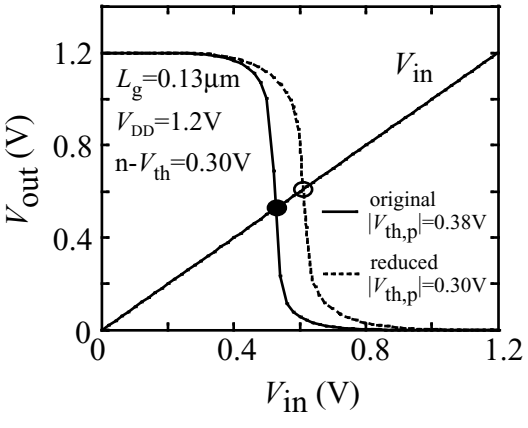

Fig. 13. HiSIM simulation of the switching-threshold voltage of CMOS inverters through a change of the $V_{th,p}$.

suggest, that the TIP may be the best design point for optimizing advanced pocket-implant technologies. It may become possible to fulfill the requirements of low TIP and V_{DD} for low-voltage applications and to combine short delay, minimized temperature dependence and low power dissipation. As we have shown, the n-MOSFET TIP determines the oscillator TIP

for long L_g, whereas the both MOSFET types are responsible for short L_g. This verifies the necessity of a $V_{th,p}$ reduction to meet the requirement of low voltage applications.

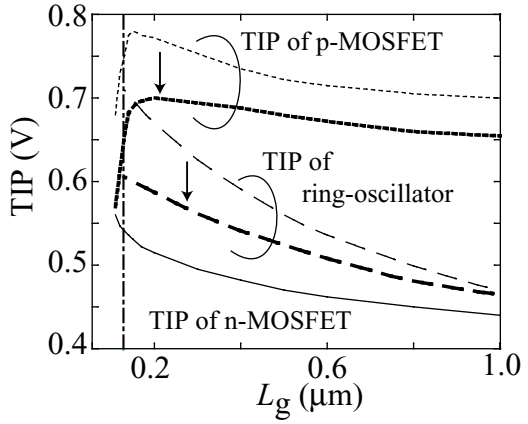

Fig. 14. Simulated TIP of n- and p-MOSFET as well as a ring-oscillator circuit as a function of L_g. The thicker lines indicate the TIP with reduced $V_{th,p}$ by decreasing the bulk impurity concentration and the pocket maximum concentration. The reductions of these values are optimized at $L_g = 0.13\mu$m (indicated by a vertical line) satisfying the inverter-threshold voltage to be equal to $V_{DD}/2$.

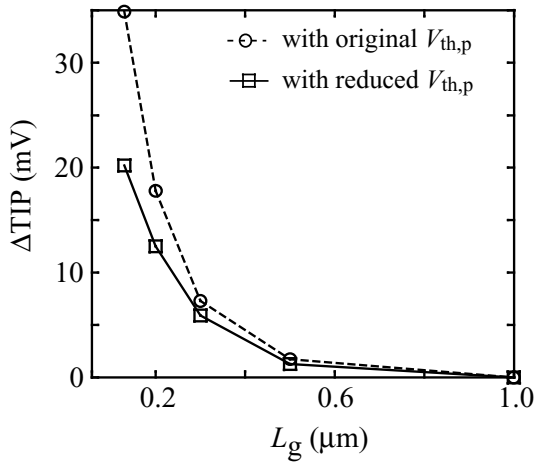

Fig. 15. Simulated difference of the ring-oscillator TIP, by varying the pocket maximum concentration in p-MOSFET (ΔTIP), as a function of L_g. The dashed and solid lines represent ΔTIP with the original $V_{th,p}$ and that with the reduced $V_{th,p}$, respectively.

We realize the reduction $V_{th,p}$ by decreasing both the bulk impurity concentration N_{subc} and the pocket maximum concentration N_{subp}, as shown in Fig. 14 by thicker lines. The reduction of the concentrations are optimized at $L_g = 0.13\mu$m satisfying the inverter-threshold voltage to be equal to $V_{DD}/2$. The TIP reduction for the ring-oscillator is about 0.1V at $L_g = 0.13\mu$m, which is efficient for low power dissipation of CMOS circuits.

For successful low-voltage applications, the TIP is required to be insensitive to technology fluctuations. The pocket implantation is known to cause serious V_{th} fluctuation. Fig. 15 shows the change of the ring-oscillator TIP (ΔTIP) by increasing N_{subp} of p-MOSFET by 10%. The dashed line depicts ΔTIP with the original $V_{th,p}$, and the solid line with the reduced $V_{th,p}$ shown by the thick dotted line. It can be seen that optimizing $V_{th,p}$ closer to $V_{th,n}$ is effective to reduce the TIP fluctuation as well.

IV. Conclusion

It is found that the transistor TIPs for a 0.1μm-scale CMOS technology with pocket implants are at about a factor 2 to 2.5 above threshold, are L_g-dependent and have different magnitudes for n- and p-MOSFET. The measured values range from $0.45\text{V} - 0.57\text{V}$ for the n-MOSFET and from $0.68\text{V} - 0.71\text{V}$ for the p-MOSFET. Circuits such as a ring-oscillator are found to have a TIP ($0.5\text{V} - 0.7\text{V}$), which lies between the TIP-values of n- and p-MOSFET, being dominated by the n-MOSFET TIP for long L_g and both the n- and p-MOSFET TIPs for short L_g.

The low circuit TIP-values are very favorable for low-voltage applications, relieving the concern of circuit operation with a positive temperature coefficient as well as the possibility of thermal instabilities [2]. Furthermore, the ring-oscillator oscillation period for short L_g hardly decreases, in contrast to long L_g, when the supply voltage is raised beyond the TIP. By designing the $V_{th,p}$ closer to $V_{th,n}$, a reduction of the TIP for the ring-oscillator can be realized. This allows not only low power dissipation and higher temperature stability of circuits, but in addition suppresses the TIP sensitivity to technology fluctuations.

References

[1] A. Bellaouar, A. Fridi, M. I. Elmasry, and K. Itoh, "Supply voltage scaling for temperature-insensitive CMOS circuit operation," *IEEE Trans. Circuit Syst.*, vol. 45, pp. 415 – 417, Mar. 1998.

[2] K. Kanda, K. Nose, H. Kawaguchi, and T. Sakurai, "Design impact of positive temperature dependence on drain current in sub-1-V CMOS VLSIs," *IEEE J. Solid-State Circ.*, vol. 36, pp. 1559 – 1564, Oct. 2001.

[3] D. Kitamaru, H. Ueno, K. Morikawa, M. Tanaka, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "V_{th} model of pocket-implanted MOSFETs for circuit simulation," *Proc. Intern. Conf. Simulation of Semicon. Processes and Devices*, pp. 392 – 395, 2001.

[4] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors," *Solid-State Electron.*, vol. 9, pp. 927 – 937, Oct. 1966.

[5] M. Miura-Mattausch, U. Feldmann, A. Rahm, M. Bollu, and D. Savignac, "Unified complete MOSFET model for analysis of digital and analog circuits," *IEEE Trans. CAD/ICAS*, vol. 15, pp. 1 – 7, Jan. 1996.

[6] M. Suetake, K. Suematsu, H. Nagakura, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, S. Odanaka, N. Nakayama, "HiSIM: A drift-diffusion based advanced MOSFET model for circuit simulation with easy parameter extraction," *Proc. Intern. Conf. Simulation of Semicon. Processes and Devices*, pp. 261 – 264, 2000.