Recent Developments in ESD Protection For RF ICs

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Abstract - New challenge in ESD protection design for RF ICs is to address the complex interactions between the ESD protection network and the core circuit being protected in both directions. This paper reviews recent developments in RF ESD protection design, including switching and mis-triggering of ESD protection networks; ESD-induced parasitic capacitive, resistive, noise coupling and self-generated noise effects; RF ESD evaluation techniques; and low-parasitic compact RF ESD protection solutions.

I Introduction

While radio frequency (RF) IC design continuously benefits from advances in IC technologies and circuit design techniques, ESD (electrostatic discharge) protection circuit design for RF ICs slow to evolve and is emerging as a new design challenge in RF and high-speed mixed-signal (M-S) IC development. On one hand, wireless RF ICs have ever increasing demand for ESD robustness because such devices, typically handheld, are much more prone to ESD-induced damages. On the other hand, any ESD protection structures, being extra devices to the core circuits protected, inevitably introduce parasitic effects to core circuits that adversely influence core chip performance, which become real limiting factors in RF and high-speed M-S IC design [1-4]. In a typical full-chip complete ESD protection scheme, multiple one-direction-active ESD protection device may be required for each I/O pad to protect the pad against ESD transients of different modes, i.e., positive (PD) and negative (ND) to V_{DD}, and positive (PS) and negative (NS) to V_{SS}. In addition, an ESD power-clamping device is needed between any pair of power rails, e.g., from V_{DD} to V_{SS} (DS) [4]. Though the total number of ESD devices per chip may be reduced depending upon special ESD protection specs and availability of dual-direction ESD structures, the head count of total ESD protection units needed for full-chip complete ESD protection is fairly large, translating into substantial overall ESD-induced parasitic effects. If one chooses the regular CMOS type ESD protection structures, which rely on large multiple-finger MOSFETs and typically need hundreds of μm in width for just 2kV HBM [5] ESD protection level, the parasitics introduced are completely intolerable to RF and high-speed M-S ICs. Further, the most troublesome issue in RF ESD protection circuit design is associated with the complex mutual interactions between ESD protection networks and core circuits being protected in both directions [4]. This paper reviews recent developments in RF ESD protection design, including the new challenges, the general interactions, the influences of circuits on ESD protection networks, the impacts of ESD protection structures on circuit performance, RF ESD evaluation techniques and possible protection solutions.

II. ESD-Circuit Interactions

The principle of RF ESD protection remains to be using a low-impedance current shunting path to discharge ESD transients safely and clamping I/O pad to a sufficient low level to avoid dielectric rupture [4]. Apparently, there exist mutual interactions between the ESD protection networks and the core circuits protected, which are referred to as the *ESD-circuit interaction*. The unique challenge in RF ESD protection design is that the degree of the ESD-circuit interactions in RF and high-speed M-S ICs becomes intolerable to both ESD protection and RF circuit performance, resulting either substantial degradation or malfunction such that it must be addressed in design [4].

Firstly, performance of ESD protection structures can be adversely affected by core circuits protected, a phenomenon defined as the *circuit-to-ESD influence* [4]. In principle, an ESD protection device works as a switch, which remains in off state during normal circuit operation and is triggered under ESD pulsing to discharge the ESD transients. In other word, an ESD structure must be immune to any desired signals and its reasonable fluctuation. However, it must respond to any undesired ESD pulses efficiently and swiftly in order to provide ESD protection. While there are many different triggering mechanisms for ESD protection structures, it is observed recently that the displacement current caused by significant variation in input voltage signal, dV/dt, and the effect associated with the substantial fluctuation in incoming current signals, dI/dt, may be coupled into the ESD devices through the parasitic capacitor and inductor, resulting in unwanted early turn-on of the ESD protection structures. The likelihood of such accidental triggering shall be apparent in super-GHz RF applications considering the fact that the ESD pulse rise time is around t_r~10ns in HBM mode [6] and $t_r \leq$200ps in CDM mode [7]. In high-speed M-S ICs, the significant switching noises in the digital blocks may also be coupled into the I/O sections and cause mis-triggering of ESD networks. Obviously, early triggering of ESD networks will cause complete malfunction of the ESD protection units and the whole IC. The new challenge here is to design an ESD protection structure with a switching time much faster than that of RF signals processed to avoid the accidental turn-on, a design requirement that is actually in line with designing advanced ESD protection structures for super fast ESD protection modes, e.g., CDM (t_r~200ps) and IEC (t_r~700ps) [8]. Extremely speaking, given significant dV/dt or dI/dt trigger-assisting effects, an ESD protection structure may

eventually not be able to distinguish ESD pulses from desired super-GHz RF signals. The associated new design challenge ahead is therefore to explore novel triggering mechanisms that are immune to the dV/dt or dI/dt effects.

Secondly, on-chip ESD protection does not come for free. Those ESD structures, though designed to be in off-state in normal circuit operation, introduce various parasitic parameters that inevitably affects circuit performance. Such phenomenon, referred to as the *ESD-to-circuit influence* [4], can be very significant to parasitic-sensitive RF and high-speed M-S ICs. Among various types of ESD-induced parasitic effects, the most harmful ones come from the parasitic capacitive elements associated with the normally large ESD structures, i.e., C_{ESD}, the noise coupling effects due to the C_{ESD}, and the noises generated within the ESD structures [1]. The impacts of the parasitic C_{ESD} effect are fairly obvious. Since traditional MOSFET ESD protection networks commonly used in CMOS IC technologies feature very large sizes even for 2kV HBM ESD protection, one would expect significant values for the parasitic C_{ESD}. An immediate adverse effect associated with the C_{ESD}, with typically from 50fF to a few pF [9], is the extra RC delay in the signal paths. Depending upon the types of ESD structures used, such RC delay could be substantial to affect the signal integrity and even corrupt critical clock signals, particularly in very high-speed ICs. The next design problem associated with the parasitic C_{ESD}, unique to RF ICs, is the loading effects of ESD-induced parasitic C_{ESD} and R_{ESD}. Such ESD loading effect will inevitably alter the fixed impedance matching environment commonly required in RF design at I/O ports, e.g., a 50Ω matching. Consequently, negative impacts on RF IC specs, e.g., power transfer efficiency and bandwidth, will result. However, such corruption in impedance matching can be recovered by absorbing the C_{ESD} and R_{ESD} into the matching networks in design phase. The new design challenge here is to accurately evaluate the magnitudes of C_{ESD} and R_{ESD} and their variations upon frequency, biasing and operational temperature, and then to include them into circuit design consideration. It is also desirable to keep C_{ESD} constant over the frequency spectrum of interest. Note that, considering ESD parasitics only matter when in ESD-off state, the R_{ESD} should be defined as the series dynamic resistance in ESD protection branches, which is not the same as either ESD discharging or physical diffusion resistances.

The next severe design problem originates from the ESD-induced substrate noise coupling effect with its root cause being the sizeable parasitic C_{ESD} [4]. ESD noise coupling effect has dual-direction nature. On one hand, any undesired noise signals incident upon an I/O pin will be directly coupled into the substrate through the C_{ESD} and cause noise problems in various blocks on the chip. On the other hand, in RF mixed-signal ICs, the large digital noises leaked into the ESD protection sections due to poor noise decoupling can be easily coupled onto I/O pins via C_{ESD} and flow back into the signal channel, resulting in circuit performance degradation.

While the ESD-induced substrate noise-coupling effect has been recognized as an ESD protection parasitic problem, the other type of ESD-associated noises, the self-generated noises within ESD protection structures, have been largely overlooked by designers. However, such ESD self-generated noises deserve more attention in practical design [4]. Such noises come from ESD structures themselves. Depending upon the device type used in ESD protection networks, i.e., diode, BJT, MOSFET, or SCR, the noises could be resistive thermal noises, shot noises, flicker noises, etc, in nature. Unlike the ESD-induced substrate noise coupling effect that may be suppressed by proper noise isolation and reduction in C_{ESD}, the ESD self-generated noises are inherent to ESD protection devices that always exist and must be dealt with in circuit design. The self-generated noises may have substantial impact on noise performance of RF ICs. All the above ESD-to-circuit influences are expected to get worse in future RF and high-speed M-S ICs because the feature size shrinking laws do not apply to ESD structures if traditional ESD protection devices are used. However, most ESD parasitic parameters are directly proportional to device sizes. Meanwhile, future RF ICs are much more ESD-demanding (i.e., >4kV). Therefore, the new design challenges originated from the ESD-to-circuit influences are fairly self-evident: low-parasitic, compact ESD structures with high protection-to-area ratio are required, which can not be satisfied by using traditional MOSFET ESD devices, e.g., grounded (ggNMOS) or gate-coupled NMOS (gcNMOS). Novel ESD protection solutions are called upon for RF ICs.

Another special requirement for RF ESD protection is that the triggering voltage (V_{t1}) of the ESD structure should be adjustable according to the circuit block protected. The reason is that, an RF or high-speed M-S IC chip often employs several different global and local power supplies and its I/O pads deal with different type of signals. While there is a chance one single type of ESD structure might work for these needs, custom-designed ESD units with varying V_{t1} are beneficial, or even critical to realizing full-chip ESD protection. This consideration translates into designing locally tailored ESD structures for different pads to realize tunable V_{t1}, for which trigger-assisting sub-circuit may be used. Ideally, ESD protection triggering voltage at one pad should be set close to the maximum signal level with a safety margin for quick response. For example, in a practical design case, an ESD protection unit with a V_{t1} of 5V is ideal for a block of V_{DD}=3.3V and an ESD protection device of V_{t1}=23V is good for a block of V_{DD}=15V. However, neither one is a universal solution for the whole chip, because it leads to either short-circuit or inadequate turn-on of ESD protection for the chip [4]. One last, but certainly not the least, RF ESD protection problem is also associated with the sizes of ESD structures. In addition to the proportionally increased ESD parasitics, a large number of big-size ESD structures poises big layout problems, such as, device matching and pad placement, etc.

To summarize, the new challenges in RF ESD protection design are mainly associated with the complex ESD-circuit interactions. Among these, the circuit-to-ESD influences may cause switching and mis-triggering problems for ESD

protection networks, resulting in malfunction of both the ESD protection networks and the core circuits. The ESD-to-circuit influences include RC delay and on-chip clock corruption due to the C_{ESD} and R_{ESD}, as well as noise performance deterioration due to ESD-induced substrate noise coupling effect and ESD self-generated noises. The challenging demands for RF ESD protection include very fast switching time, high immunity to mis-triggering by super-GHz RF signals, high ESD robustness, compact size, high ESD protection-to-area ratio, and low parasitic effects. Another highly desirable feature for RF ESD protection is the multiple-mode active discharging property that allows using one single ESD unit per pad to protect against ESD pulses of all modes, instead of using multiple one-direction-active protection devices, in a complete ESD protection scenario, hence reducing the total ESD-induced parasitics. The new challenges and demands for RF ESD protection are summarized in Tables I. Apparently, ESD protection design and RF IC circuit design can no longer be conducted separately by ESD technologists and designers, respectively. Instead, it must be treated as an integrated design task with mutual interactions considered. Adequate evaluation of such practices, to be discussed later, is essential. Finally, however most importantly, CAD-based full-chip ESD design verification, which includes verifying ESD protection operation at whole chip level and examining RF circuit specs with ESD protection devices in place, must be performed to ensure performance. Such sophisticated ESD design CAD package is still under development [10].

Table I A summary of new RF ESD protection design challenges

Challenges		Design Concerns	Phenomena
ESD-Circuit Interactions	Circuit-to-ESD Influences	ESD protection switching	Response to fast ESD pulses
			Immune to super-GHz RF signals
			Immune to digital noises
		ESD accidental triggering	ESD protection malfunction
			Core circuit malfunction
	ESD-to-Circuit Influences	RC delay by C_{ESD} /R_{ESD}	Signal corruption
		RF I/O Z-matching	Varying RF Z-mismatching
			Power transfer efficiency
		Noise coupling by C_{ESD}	External to substrate noise injection
			Substrate to I/O noise feedback
		ESD self noises	Worse noise figure

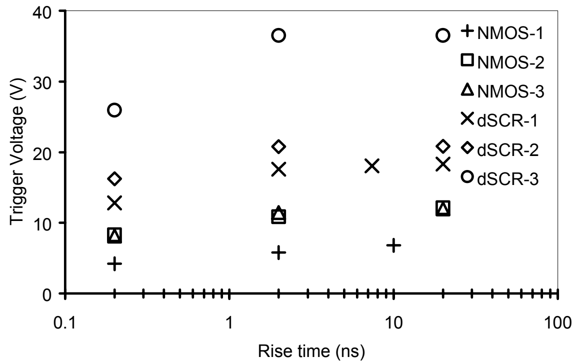

Figure 1 Typical V_{t1}~t_r from TLP tests for ESD protection devices.

III. Circuit-to-ESD Influences

As discussed previously, the core circuits under protection may have adverse impacts on operation of the ESD protection networks. In RF and high-speed M-S ICs, such circuit-to-ESD influences might result in switching or mis-triggering problem of the ESD protection networks, because the ESD devices may not distinguish undesired ESD pulses from the desired super-GHz RF signals and the strong switching noises coupled from digital blocks. Consequently, malfunction of both the ESD protection structures and the core circuits may occur. This negative phenomenon can be understood from the following analysis. It is recently observed in TLP (transmission line pulsing) measurements of ESD protection structures that the triggering voltage, V_{t1}, of an ESD protection structure may be altered by the rise time, t_r, of the TLP pulse used in TLP tests. TLP test data show that triggering voltage may decrease as the TLP pulse rise time increases. This phenomenon is clearly shown in Figure 1, where a variety of different ESD protection structures, e.g., ggNMOS (NMOS1-3) and dual-direction SCR (dSCR1-3), designed in different processes were measured by a TLP tester with varying pulse rise time [4, 11]. The TLP pulse rise time varies from 200ps to 20ns. The strong dependence of V_{t1} on t_r is readily observed from our data. Although the degree of dependence varies for different ESD protection devices: some showing monotonic decrease of V_{t1} with reduced t_r; others featuring a saturation trends beyond some points, the direct dependence of V_{t1} on t_r is undisputable, for which the displacement current associated with the substantial dV/dt rate may play a key role. Taking a ggNMOS ESD protection structure shown in Figure 2 as one example, its protection mechanism follows [4]: As an ESD pulse comes to the drain, its drain junction is reverse biased to breakdown. The avalanche-generated holes flow through the p-well resistor into the ground, build up a forward potential over the source junction, turn it on, and discharge the ESD transient via the parasitic lateral NPN device. Hence, the V_{t1} is directly controlled by the substrate current, I_{sub}, which is mainly the avalanche hole current. However, if the dV/dt rate is significant and the drain junction capacitance is sizable, the displacement current, i=CdV/dt, will be coupled into the substrate, contributes to the I_{sub}, and

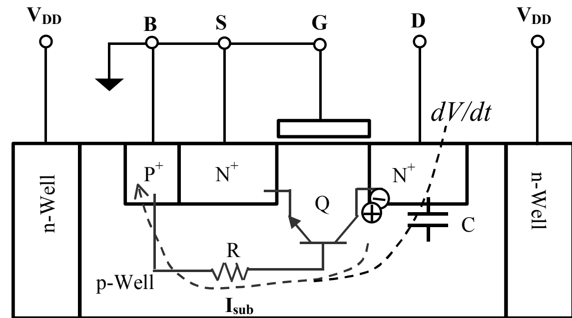

Figure 2 A cross-section for a ggNMOS ESD protection structure.

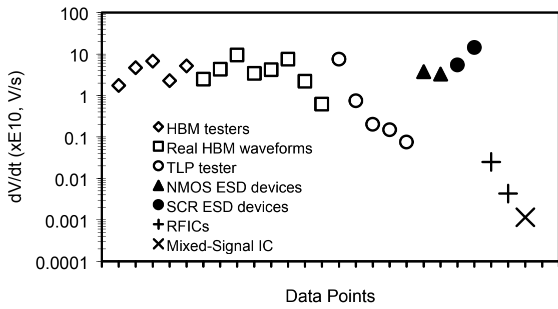

Figure 3 *dV/dt* data for real ESD waveforms, HBM zappers, TLP testers, ESD devices and RF signals reside in the same spectrum.

accelerates the triggering process. The same applies to an SCR ESD protection structure as well. How high a dV/dt ratio is needed to forward turn on a PN junction (~0.65V) in an ESD protection structure and can such a desired dV/dt rate be produced by an ESD pulse? Our rough calculation suggests that the triggering threshold dV/dt ratios are from $3x10^{10}$ V/s to $1x10^{11}$ V/s for typical NMOS and SCR ESD protection structures measured. These estimated data are shown in Figure 3 as solid markers. Further, typical dV/dt data obtained for a set of HBM ESD zapping testers, real HBM ESD waveforms and TLP testers range from $7x10^8$ V/s to $1x10^{11}$ V/s as shown in Figure 3 by hollow markers [12]. Obviously, these two data sets roughly fall in the same bandwidth, which seem to support the dV/dt displacement theory in understanding the V_{t1}~t_r phenomenon observed. Now, let's apply the displacement current theory to RF ESD protection. While recognizing frequencies and magnitudes of RF signals vary widely and without attempting to cover all types of RF signals, a few dV/dt data points are derived from some RF and M-S IC papers. This results in a dV/dt of ~$2.5x10^8$ V/s for a 2.5GHz CMOS clock recovery circuit [13], ~$4.3x10^7$ V/s for a 1GHz CMOS clock synthesizer [14] and ~$1.23x10^7$ V/s caused by 7.1MHz digital clock noise coupling in a mixed-signal CMOS receiver chip [15]. These RF IC signal data, also shown in Figure 3, are really approaching the troublesome dV/dt bandwidth that starts to trigger the V_{t1}~t_r effect. Hence, it is reasonable to believe that, considering possibly stronger signals and higher frequencies, input and output RF signals and substantial digital noises in M-S ICs might accidentally trigger ESD protection structures at I/O pads, leading to chip malfunction. Hence, the V_{t1}~t_r phenomenon associated with RF signals must be considered in RF ESD protection design. Solutions to the problem are to make ESD protection switching much faster than the RF signals processed for dV/dt immunity or to explore novel ESD protection triggering mechanisms.

IV. ESD-to-Circuit Influences

As discussed previously, ESD protection structures inevitably produce parasitic effects, which will affect circuit performance. These ESD-induced parasitics include RC delay associated with parasitic C_{ESD} and R_{ESD}, substrate-I/O noise coupling due to C_{ESD}, and ESD self-generated noises. The ESD-to-circuit influences include clock corruption, signal integrity, RF impedance matching, power transfer efficiency, bandwidth reduction and noise performance, which become intolerable to RF and high-speed M-S ICs. Several RF circuit examples are discussed in this section to illustrate the severity of the ESD-to-circuit influences.

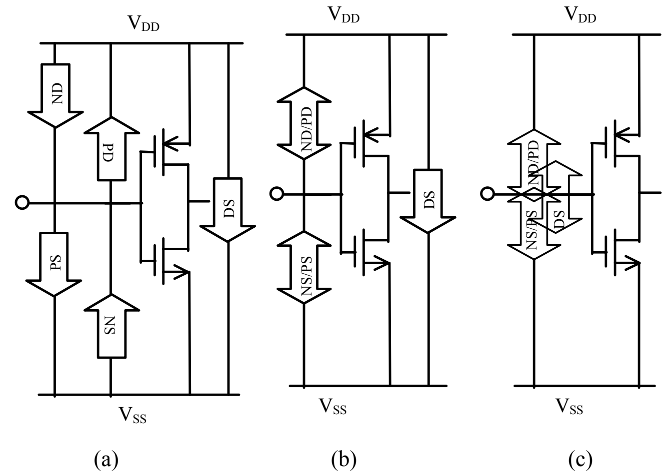

Figure 4 Complete ESD protection schemes using ESD1 (a), ESD2 (b), and ESD3 (b), respectively.

To investigate the impacts of ESD-induced capacitance, C_{ESD}, three different ESD protection structures with different parasitic C_{ESD} are used for the same 4kV ESD protection level. They are a traditional uni-direction ggNMOS structure, ESD1 [4], a dual-directional ESD protection device, ESD2 [16], and a novel all-mode ESD protection structure, ESD3 [3], each having different device size. The main difference between these three structures is their protection efficiency as illustrated in Figure 4. For complete active ESD protection, four ggNMOS protection devices per I/O pad and one power clamp are needed for PD, ND, PS, NS and DS ESD stressing modes. To achieve the same ESD protection, two dual-direction ESD protection devices per pad and one power clamp are necessary. However, only one all-mode ESD protection device per pad is needed to protect against all four ESD stressing modes as well as power surges. The junction capacitances, C_{Si}, associated with these ESD protection structures are extracted as listed in Table II. It is important for designers to understand that parasitic capacitances of metal interconnects in ESD protection structures, C_M, should be considered as well since metal coverage in ESD structures is usually very sizeable [2]. In this study, a commercial 0.18μm 6-metal CMOS process with both Al and Cu interconnects are used and ESD protection metal capacitances are extracted and added to the

Table II Estimated C_{ESD} data for ESD1, ESD2 and ESD3 devices

ESD structures		ESD1		ESD2		ESD3	
C_{ESD} (pF)	C_{Si}	0.54		0.09		0.07	
	C_M	Cu	Al	Cu	Al	Cu	Al
		0.30	0.43	0.029	0.041	0.019	0.028

total C_{ESD}, as listed in Table II. The difference between using Al and Cu interconnects is that Cu is more ESD robust, therefore, requires narrower metal line width (~30% less) for the same ESD protection. Overall, to achieve the same ESD protection level of 4kV, a large C_{ESD} is expected if using ESD1, which is reduced by ~85% when using a dual-direction ESD2 and a further 23% reduction can be realized if using the all-mode ESD3 protection structure [2]. The extracted C_{ESD} values for ESD1/2/3, along with the number of protection units per pad required for complete ESD protection, are used to evaluate the degree of ESD-to-circuit influences on selected RF circuits.

Three special RF ICs were designed in this study to examine the ESD-to-circuit influences including C_{ESD} effects, noise impact and general specification deterioration [2]. The first circuit is a 15-stage 4.7GHz ring oscillator in 0.18μm CMOS process. The three ESD protection devices, ESD1, ESD2 and ESD3, are used to protect the oscillator circuit. They have the same metal coverage and different parasitic C_{ESD} due to silicon structures. The data show that, in a single-load case where only one node has ESD protection, an 85% clock speed reduction occurs when using ESD1, which can be recovered by 41% and 62% if using ESD2 and ESD3, respectively. The clock corruption problem becomes much worse in a full-load ESD protection scenario. This example, though very simple, demonstrates clearly that the C_{ESD} induced RC delay effect may affect on-chip signal integrity severely in RF applications if traditional parasitic-intensive ESD protection structures are used. Novel low-parasitic, compact, multiple-mode ESD structures are highly desirable to suppress this C_{ESD} influence.

A second circuit, a low-power high-speed Op Amp IC is designed to study the full-band C_{ESD} impacts on general circuit specifications. The Op Amp chip, implemented in a 0.18μm CMOS in both Al and Cu interconnects, as depicted in Figure 5, features differential input for noise rejection, a source-follower gain stage for high gain and level shift, a push-pull output stage with low quiescent current for large swing, lower power and crossover distortion elimination, as well as a compensation capacitor with active nulling for wide bandwidth and better stability. Its key specs include a very low power consumption of 0.43mW, a high slew rate of 116mV/ns, a short settling time of 3.7ns at 1%, wide output

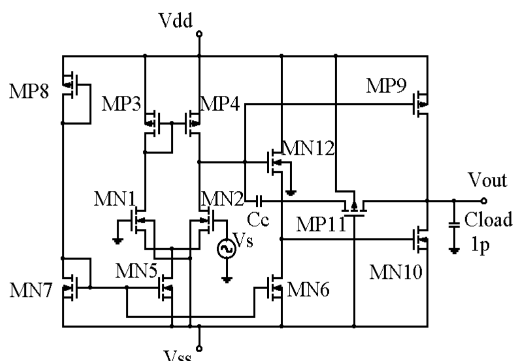

Figure 5 Schematic for an Op Amp circuit in 0.18μm CMOS.

Table III Op Amp spec variation with different ESD (C_L = 1pF).

		f_T (MHz)	Phase Margin	Slew Rate (mV/ns)	Settling Time (ns)
No ESD		120.7	70.1°	115.9	3.77
ESD1	Al	74.0	60.0°	81.0	17.07
	Cu	77.5	61.2°	84.4	11.92
ESD2	Al	109.9	68.7°	109.9	7.60
	Cu	110.7	68.8°	110.4	7.47
ESD3	Al	112.2	69.0°	111.1	7.15
	Cu	113.0	69.1°	111.5	6.85

Table IV C_{ESD}–caused spec degradation of Op Amp in Al.

Parameters	No C_{ESD}	ESD1	ESD2	ESD3
f_T (MHz)	120.7	-38.7%	-8.9%	-7.0%
		Recovery		
		→	+ 81.9% (+83.5% in Cu)	→
Phase Margin	70.1°	-14.4%	-2.0%	-1.6%
		Recovery		
		→	+ 88.9% (+90.3% in Cu)	→
Slew rate (mV/ns)	115.9	-30.1%	-5.2%	-4.1%
		Recovery		
		→	+ 86.4% (+88.7% in Cu)	→
t_{set} (ns, 1%)	3.77	-353%	-102%	-89.7%
		Recovery		
		→	+74.6% (+76.9% in Cu)	→

swing of 0.96 at 80% gain, and a large unity-gain bandwidth of 121MHz. ESD protection are provided by ESD1, ESD2 and ESD3 in both Al and Cu interconnects, respectively. The Op Amp key specs are evaluated for the different ESD protection cases and compared with the non-ESD, C_{ESD}=0, circuit, with typical data summarized in Tables III & IV. These data clearly show that almost all key parameters suffer substantial degradation when using large size ESD protection structure and significant recovery can be realized by using low-parasitic compact ESD protection structures. For example, the f_T decreases 38% when using ESD1 in Al, which recovers by more than 80% if using ESD2 and ESD3. Its slew rate degrades by 30% when using ESD1 in Al that is recovered by 86% if using ESD2 and ESD3. The impact of C_{ESD} of ESD metal coverage, Al versus Cu, is also observed clearly. This example demonstrates that the ESD-induced C_{ESD} may have broad impacts on RF and mixed-signal circuit specs, in addition to the clock corruption due to simple RC delay.

To investigate the influence of ESD self-generated noises, a Bluetooth low-power 2.4GHz LNA circuit is designed and its noise performance is examined for different ESD protections, i.e., using ESD1, ESD2 and ESD3, respectively

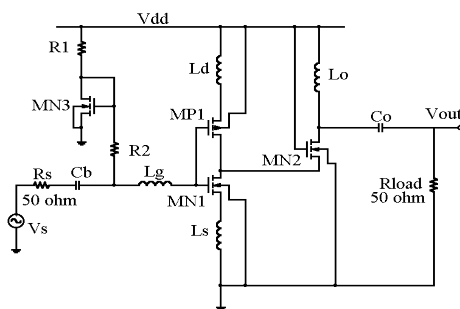

Figure 6 Schematic for the LNA in 0.18μm CMOS.

[2]. Figure 6 shows the LNA schematic featuring two-stage topology for high gain, current sharing for low power and on-chip 50Ω matching at both input and output ports, with typical specs of center frequency of 2.4GHz, noise figure NF=1.76dB, low power of 24mW in 3.3V, S_{21}=23.4dB, S_{11}=-34.5dB, S_{22}=-47.7dB and S_{12}=-39.6dB. The impedance mismatching associated with C_{ESD} and R_{ESD} is absorbed into the LNA matching networks. The LNA noise performance using ESD1/2/3 protection structures are evaluated. The noise models for ESD protection structures can be derived based upon their internal elements, e.g., resistor, diode, MOSFET, BJT and SCR [4]. Figure 7 shows the NF versus ESD1 size relationship, which clearly illustrates that larger size ESD protection device with more self-generated noises affects circuit NF spec significantly. The significance of ESD-to-circuit noise influence when using large-size parasitic-intensive ggNMOS, i.e., ESD1 (increased by 3.78%), and the benefit of using low-parasitic compact protection devices, i.e., ESD2 and ESD3, are readily observed from Table V. The above examples demonstrate very clearly that the ESD-to-circuit influences can be very significant. The adverse impacts of ESD-induced parasitics on RF IC specs are very general, ranging from simple RC-delay, Z-matching, bandwidth, slew rate, stability, to noise figure, etc. It is also fairly clear that low-parasitic compact ESD protection structures are desirable in order to suppress the ESD-to-circuit influences.

V. RF ESD Protection Evaluation

From previous discussions, it is clear that the ESD-circuit interactions must be characterized in evaluating RF ESD protection designs. While no general approach exists yet, several measures play roles. The ultimate evaluation method for RF ESD protection design is to examine the overall specs for both ESD protection and RF core circuit performance, including characterizing the circuit-to-ESD influences and the ESD-to-circuit influences. For the former task, ESD protection design simulation and full chip level ESD protection design verification are critical in design phase. In testing, one may apply RF signals to ESD protection networks and probe the resulting I-V curves to find whether RF signal induced mis-triggering may be a problem, which is very similar to the popular ESD TLP testing [4]. For the latter task, it is imperative to include the ESD parasitic models into circuit simulation and measurements, and then to evaluate the degree of the ESD-to-circuit impacts in terms of general RF circuit specs. After all, a circuit is qualified by a group of specs, instead of one or two figures-of-merit. This general evaluating method approach has been illustrated in the previous section.

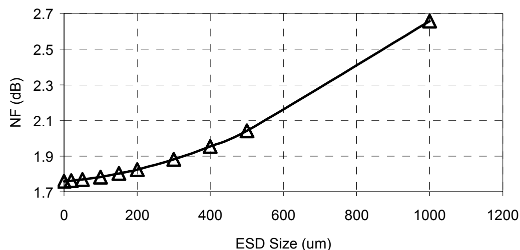

Figure 7 LNA NF~ESD size using ESD1 shows strong impact.

Table V Impact of ESD self generated noise on LNA noise spec

ESD Protection Type	NF (dB)	Degradation
No ESD	1.7582	-
ESD1	1.8247	3.78%
ESD2	1.7596	0.08%
ESD3	1.7586	0.02%

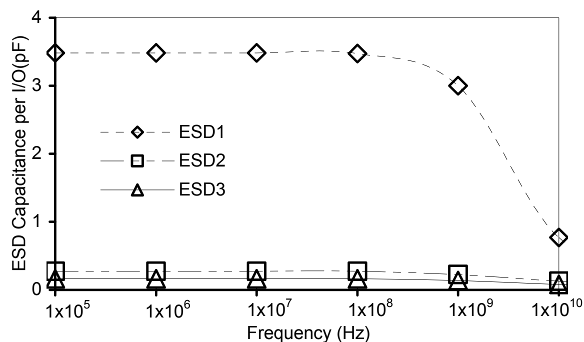

Figure 8 C_{ESD}~f characteristics for different ESD protection structures: 4xESD1, 2xESD2 and 1xESD3.

ESD-induced parasitic capacitances, C_{ESD}, should be examined first. Figure 8 illustrates the C_{ESD} ~ frequency curves up to 10GHz for the 4kV ESD1, ESD2 & ESD3 structures in a full protection schemes, i.e., 4xESD1, 2xESD2 & 1xESD3 per pad. The variation in C_{ESD} for different ESD protection structures is clearly observed. Noise performance should be characterized next for the ESD protection structures designed. In addition, special parameters may serve as characterizing indicators in RF ESD protection. The first are s-parameters, because one is dealing with RF circuit design. Based upon the two-port theory, an ESD network can be modeled by a series RC net consisting of parasitic C_{ESD} and R_{ESD} as shown in Figure 9a where R_{ESD} is the series dynamic resistance in the ESD protection branch in ESD-off state. The impedance mismatching effect caused by the ESD network can then be described by the reflection (S_{11}) and forward transmission

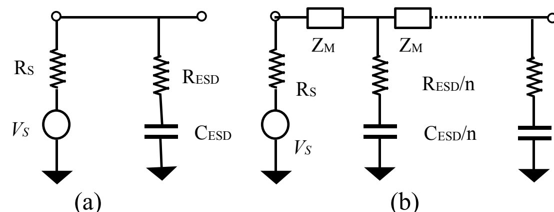

Figure 9 ESD protection model (a) and a distributed ESD protection network model (b).

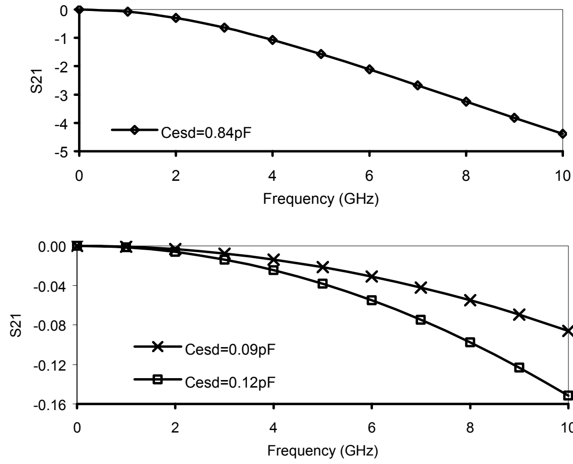

Figure 10 S21~f curves for C_{ESD} =0.84pF, 0.12pF & 0.09pF.

(S_{21}) of RF signals. For example, Figure 10 shows the S_{21}~f curves for C_{ESD}=0.09pF, 0.12pF and 0.84pF, for ESD3, ESD2 and ESD1 devices in Cu process previously discussed with resistive loss ignored. The impacts of C_{ESD} on RF signal reflection and frequency bandwidth are obvious. Another potentially interesting parameter is Q-factor of the ESD network. Using the series C_{ESD}~R_{ESD} model of Figure 9a, the ESD network Q-factor is given by,

$$Q = \frac{1}{2\pi f C_{ESD} R_{ESD}}$$

Now, let's look at the noise figure (NF) of the ESD network. Using the classic two-port noise source model [17], the NF of ESD network due to resistive thermal noises is derived as,

$$NF_{ESD} = \frac{V_{n,out}^2}{A_V^2 4\kappa T R_S} = 1 + \frac{R_S R_{ESD}}{R_{ESD}^2 + \frac{1}{(2\pi f C_{ESD})^2}}$$

where $V_{n,\,out}$ is total output noise, A_v is voltage gain, R_S is internal source resistance. In correlating Q-factor, R_{ESD}, C_{ESD} and NF_{ESD}, if R_{ESD}>>(1/2πf C_{ESD}), a large R_{ESD} is preferred for small NF_{ESD}; however, if R_{ESD}<<(1/2πf C_{ESD}), a small R_{ESD} is desired to reduce NF_{ESD}. A small C_{ESD} is always beneficial to minimizing NF_{ESD}. It seems that the Q-factor can be used as a characterizing parameter for RF ESD protection in terms of noise spec. However, because of the R_{ESD}~C_{ESD} relationship, its frequency dependence and the difficulty in extracting series dynamic R_{ESD}, using Q-factor as a useful indicator is difficult. Although both s-parameters and Q-factor are used in practices for evaluating RF ESD protection [18, 19], characterizing general RF circuit specs should still be the ultimate testing measure for IC designers.

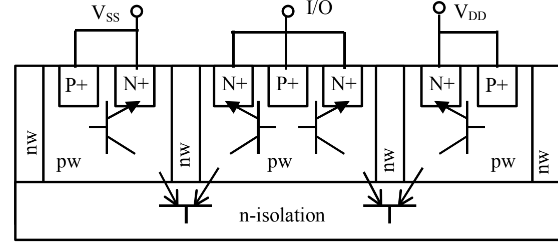

Figure 11 Cross-section for ESD3, an all-mode compact ESD protection structure [3].

VI. RF ESD Protection Solutions

Currently, it is still premature to claim any decisive RF ESD protection solutions yet. On one hand, there is no all-fitting or well-argued RF ESD protection solution in existence. One the other hand, all traditional ESD protection solutions may be used for RF ICs provided that the ESD-circuit interactions are minimized. The root cause to the ambiguity is that RF ESD protection is still in the problem-shaping phase regardless of all existing claims one may have heard. Nevertheless, in practical RF IC design, the demanding factors listed in Tables I shall be good checking points in guiding RF ESD protection design. Several proposed, yet to be further investigated, RF ESD protection solutions follow. First of all, novel, low-parasitic, compact, multiple-mode ESD protection structures are in demand. For example, the dual-mode ESD2 and all-mode ESD3 structures discussed previously are attractive. As indicated in Figure 4, using multiple-mode ESD protection structures can substantially reduce the total headcounts of the ESD protection devices needed on a chip, hence, their parasitic effects in total. Figure 11 shows cross-section of ESD3, which is an all-mode ESD protection device with a high ESD protection-to-area ratio of 80V/μm-width. Other than its large ESD protection to silicon ratio, the main advantage of ESD3 is that one active SCR-type device always exists between any two terminals, making it possible to use one single ESD3 for each pad for complete ESD protection. Consequently, fewer, smaller ESD devices are needed per chip, resulting in much lower ESD-induced parasitics. Bonding-pad-oriented ESD protection structure is another type of attractive RF ESD solution. Figure 12 shows such a design for the all-mode ESD3 structure implemented in BiCMOS [22], which ensures uniform ESD discharging, low parasitics and ease of layout. The popular gcNMOS (gate-coupled NMOS) ESD protection structure cannot be used in RF ICs due to the potential short-circuit problem. It seems to be obvious that MOSFET type protection is not a valuable option due to their large sizes. Interestingly, diode strings re-emerge as attractive candidates because the C_{ESD} can be reduced substantially in the series connection [20]. Of course, one has to minimize diode dynamic resistance by designing proper sizes in order to make sure that the increase in voltage drops over the diode string would not cause voltage-clamping problem under large ESD currents. Another main issue in using diode strings is that substantial

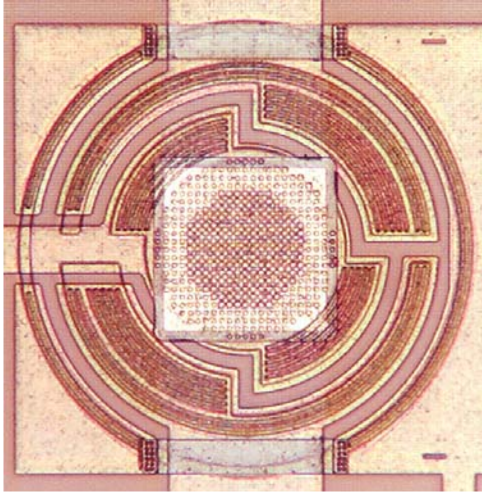

Figure 12 A pad-oriented all-mode ESD structure [22].

leakages may occur due to Darlington effect because an IC diode is a BJT in nature [4]. Stacked diodes in polysilicon can be used in minimizing C_{ESD} and suppressing Darlington effect, with the drawback of poor heat dissipation [21]. In addition, other type of parasitic C_{ESD}, e.g., metal interconnects, might be a significant concern in diode-string design, which has not been studied yet. Since a constant C_{ESD} is preferred [20], complementary ESD protection connection shall be beneficial, while a varactor diode should be avoided. From RF impedance matching viewpoint, if R_{ESD} and C_{ESD} cannot be absorbed by the matching network, an impedance transformation unit may be used. A distributed ESD protection network based upon this concept and using IC co-planer waveguide (Z_M) devices [9], as illustrated in Figure 9b, demonstrates improvement in s-parameters and bandwidth, which, however, increases design complexity. Finally, a well-thought-out full chip RF ESD protection scheme is certainly the most important thing. Figure 13a shows a whole-chip RF ESD protection solution using dual-direction ESD2 type I/O protection units, where a low-resistance, active ESD discharging path exists between any two pads. Compared with a protection scheme using traditional uni-direction ESD devices shown in Figure 4a, the total number of ESD devices is minimized, resulting in much lower total ESD-induced parasitics. Use of a common ESD discharging bus can also help to reduce the number of ESD devices needed [4]. Figure 13b illustrates another full chip RF ESD protection scenario that uses stacked diodes for I/O pads and stacked diodes power clamps, where active discharging paths exist between I/O pad and power buses. However, to ensure active, low-R discharging channels between any I/O pads, a dual-mode power clamp, e.g., ESD2 type, should be used. More solutions are yet to come.

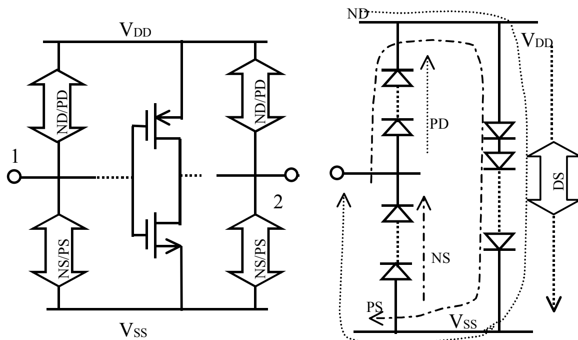

Figure 13 Two full-chip RF ESD protection schemes.

VII. Summary

In summary, RF ESD protection emerges as a new design challenge for advanced RF and high-speed M-S ICs. The problem comes from the ESD-circuit interactions on RF chips. The circuit-to-ESD influences may cause mis-triggering problems of ESD network, leading to malfunction. The ESD-to-circuit influences originate from ESD-induced parasitic C_{ESD}, substrate noise coupling and self-generated noises, may affect RF IC performance. Chip level design verification, covering the ESD-circuit interactions, is desirable in RF ESD protection design. Optimized RF ESD protection solutions demand novel, low-parasitic, compact, multiple-mode ESD protection structures.

Acknowledgements

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