Accurate Prediction of the Impact of On-chip Inductance on Interconnect Delay using Electrical and Physical Parameter-based RSF

Takashi Sato[1,8], Toshiki Kanamoto[2], Atsushi Kurokawa[3], Yoshiyuki Kawakami[4], Hiroki Oka[5], Tomoyasu Kitaura[6], Hiroyuki Kobayashi[7], and Masanori Hashimoto[8]

Desi-micron Design Study Group, EDA Technical Committee of JEITA

[1]Hitachi, [2]Mitsubishi, [3]STARC, [4]Matsushita, [5]NTT-AT, [6]Fujitsu Lab., [7]Nihon Synopsys, [8]Kyoto Univ.

Abstract

This paper proposes a new methodology to accurately predict the impact of inductance on on-chip wire delay using response surface functions (RSF). The proposed methodology consists of two stages which involves first calculating the delay difference between RC and RLC wire models for a set of parameter variations, then building RSFs using electrical parameters such as wire resistance, capacitance, etc., and physical parameters such as wire width, pitch, etc. as variables. The proposed methodology can help 1) to define design rules for avoiding inductance effects, 2) to point out wires that require RLC delay calculation, and 3) to estimate and correct the delay when using an RC model. An example design rule for limiting self inductance and accurate estimation of the delay difference for a 100 nm technology node is also presented.

I. Introduction

Low-resistance metalization and the progressive increase of the clock frequency are forcing designers to consider on-chip inductance effects at every stage of the design [1][2]. Inductance effects, which both circuit and process designers previously ignored as an off-chip issue, are becoming non-negligible in recent LSI design environments. Understanding inductance impact on signal propagation is especially crucial for systems on a chip (SoC) where design and verification processes are highly automated. Stringent and feasible rules to manage inductance have to be integrated into electronic design automation (EDA) tools.

RC models, which consist of a network of resistors and capacitors [3], are commonly used in current SoC timing analysis. With technological advances, the accuracy requirement is becoming more severe. The necessity of including inductance in the wire model (RLC model) must be quantitatively studied since the border of transition from RC to RLC models is not yet clear for general signal wires. A major obstacle for including inductance in delay calculation is the difficulties in extraction — determining current return path which has a significant influence on inductance. The partial equivalent element circuit (PEEC) model eliminates pre-determination of the current path [4], but in turn, the extracted netlist tends to become very large because inductance is not shielded by neighboring conductors.

To determine the wires that require calculation using RLC models, inductance screening functions are proposed in [2][5]. These functions are useful when the exact parasitics are available since they use electrical parameters such as R, L, or C as variables. However in floor-planning or routing, it would be more convenient if the physical dimensions, such as wire width or spacing, were the parameters for predicting the delay difference. Also, the existing functions provide screening with a fixed threshold, for example at 20 % delay difference, which may be too stringent or insufficient depending on the design stages of interest. The authors in [6] propose to calculate the range of inductance by physical dimensions using assumptions for the current return path. They presume lower and upper limit inductance occur when the wire lies next to or in the middle of the ground grid, respectively. Then the inductance impact is evaluated using 2nd and 3rd moments. This approach is efficient for use early in the design phase but instead, it does not give an exact timing difference of introducing inductance into delay calculation, especially when placing the wire in between the extreme positions.

Concentrating on the delay difference for a particular process and design, we propose a methodology that quantitatively compares RC and RLC delay to understand inductance impact on delay calculation and to create accurate response surface functions (RSF) [7], that enable screening at any RC-RLC delay difference threshold. By using electrical or physical parameters as the variables for RSF, vast applications are possible: (1) to define guidelines or design spaces where designers do not need to be concerned about inductance, (2) to establish optimal screening equations or their constants, and (3) to estimate the difference and correct the delay when using RC delay model instead of RLC delay when necessary.

II. Overall flow of the methodology

Fig. 1 shows overall flow to quantitatively compare RC and RLC delay and to generate screening functions. The flow consists of two steps:

1. A quantitative delay difference comparison by including self inductance to the wire model.
2. RSF generation to predict delay difference using electrical and physical parameters for accurate timing

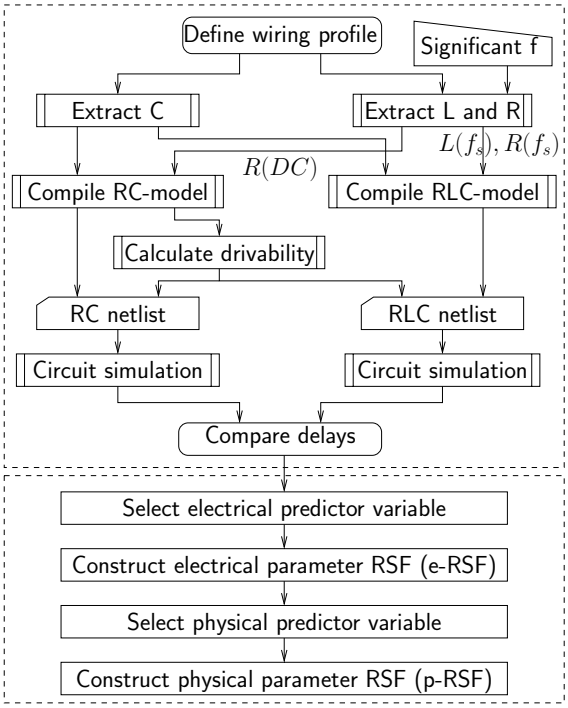

Fig. 1. Overall flow of the proposed methodology.

verification and for inductance impact estimation early in the design phase, respectively.

A. Quantitative comparison of RC and RLC delays

The wire structure consists of a wire profile defined by the process technology such as metal and dielectric layer thickness, etc. and wire dimensions controllable by designers such as width, pitch, or the length. We assume the use of a regular mesh of the power supply and ground grid that serves as the current return path. The structure window is sufficiently wide so that the low-frequency inductance does not fluctuate significantly with ground wires located at the window edge.

In Fig. 1 the proposed flow uses two input files that describe the same wiring structure — one to extract capacitance and the other for resistance and inductance. The extraction of resistance and inductance is executed at the frequency of interest since they are frequency dependent. A low frequency [8] or significant frequency f_s [9] is an example of a representative frequency. Here, f_s is defined as

$$f_s = \frac{0.35}{t_r} \tag{1}$$

where t_r is signal transition time [9][10]. The wire inductance and resistance strongly depend on the relative position of the surrounding conductors as well as its dimensions. Thus three-dimensional (3-D) extraction [11][12] is required. The capacitance extraction can be done by using either 2-D or 3-D tools [11][13]. In many cases where the inductance is a concern, 2-D extraction is sufficient because the wire length is much larger than the cross section. Conductance of the dielectric material is ignored for less than 10 GHz. Using extracted electrical parameters, a ladder circuit is compiled as RLC and RC models. The RLC model is constructed as π-segments using series resistance and inductance and shunt capacitance. The segment length l_s can be determined as follows [10]: 1) when $R/\omega L < 1$, i.e. when inductive impedance is dominant, l_s has to be much smaller than the wave length at f_s; or 2) when $R/\omega L > 1$, i.e. when resistance is dominant, the model needs to be divided into 3 to 5 segments. The RC model, on the other hand, can be generated using low frequency resistance. Removing inductance from the corresponding RLC model to generate the RC model is not necessarily a shortcut when the resistance at the frequency of interest may be different from the one at DC.

To make a fair delay comparison, we have configured the RC and RLC models with the same number of segments. Here in this analysis, the driver and receiver is determined by considering the wire load as a simple RC structure, which is commonly done in the current design [3]. The same set of drivers and receivers is used for both models since the objective is to judge whether RC-based delay changes or not by introducing inductance. The driver is modeled as an equivalent resistance R_d and voltage source with a ramp-input, and the receiver as a gate capacitance C_g. The wire delays of both models are compared through circuit simulations.

B. Electrical and Physical Parameter based RSF

After delay differences between RC and RLC models for the set of parameter variation are calculated, the screening formulas are constructed using response surface methods (RSM). We first select the electrical parameters, such as parasitic inductance or capacitance, etc. as predictor variables, by investigating the results or referencing already proposed screening rules. Then using them as predictor variables, an e-RSF (electrical parameter RSF) to predict latent errors introduced by ignoring inductance is calculated. e-RSF can be used in post-layout verification to point out or to correct the possible delay calculation error.

We then build another RSFs based on physical parameters (p-RSF) for use in the earlier design phases when calculating electrical parameters are too expensive, or when exact values are not available. Signal wire width, ground pitch, etc. are examples of physical parameters. p-RSF may not be as accurate as e-RSF, but it can be used to quickly and interactively calculate the inductance impact in floorplaning, or routing design phase.

III. Example analysis for 100 nm node wires

Based on the projections in International Technology Roadmap for Semiconductors (ITRS) [14], wire dimensions for high-performance SoC are defined as shown in Table I. We apply our proposed methodology at this 100 nm technology node to evaluate inductance effect.

TABLE I
ASSUMED TECHNOLOGY PARAMETERS.

Items	unit	value
Technology node	nm	100
Effective resistivity ρ	$\mu\Omega$-cm	2.2
Dielectric constant ε_r		1.9
ASIC clock frequency	GHz	0.98
Clock rise/fall time t_r	ps	102
Significant freq. f_s	GHz	3.4
Minimum wire pitch P_{min}	nm	460
Minimum wire width W_{min}	nm	230
Wire thickness T	nm	621
Via depth H	nm	644
Wire resistance	Ω/mm	154
x1 inverter on-resistance R_0	Ω	3480
x1 inverter gate capacitance C_0	fF	3.3

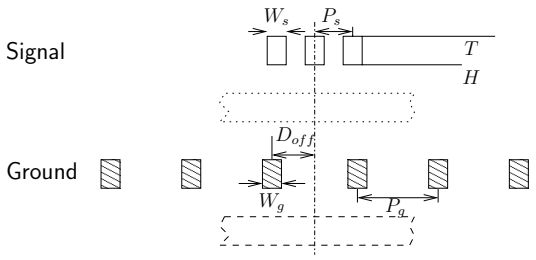

Fig. 2. Signal and ground wire profile.

A. Wiring structure

Fig. 2 shows the wire profile used in this analysis. Three global signal wires run in parallel on the top level metal layer with width W_s and pitch P_s. Below the signals lie power and ground grids running in parallel to the signal with regular pitch P_g. We define parameter variations as shown in Tables II and III. The different parameter ranges used in each case are determined by the relative direction between signal wire and cell row. Table II covers the case when power and ground grids are sparsely distributed around the signal wire thus the cell rows placed in parallel with the signal wires contribute to a major current return path. Table III covers the case when power supply of the cell row runs perpendicular to the signal wires in which case the power and ground lines in the grid contribute to a dominant current return path. We call parameter combinations in Table II and III as "CRC" (current return using cell power supply and ground) and "CRG" (current return using grids), respectively. The combination of these parameters represents a wide range of wire configurations found in the actual design. Here the values for P_s, W_s, P_g, W_g are multiples of their respective minimum dimensions. Wire-alignment offset D_{off} is 0 when the center signal conductor is right above a ground conductor, and 1/2 when signal is in the middle of two neighboring ground conductors. The maximum wire length is limited to 2 mm with the assumption of automatic buffer insertion to avoid crosstalk and slew degradation. RC and RLC delay is compared for all parameter combinations in each table.

TABLE II
PARAMETER VARIATION TO DEFINE WIRING PROFILE "CRC". SIGNALS RUN IN PARALLEL WITH CELL ROW.

Parameter	Unit	Variation
Signal pitch P_s	P_{min}	x1, x2, x5, x10, x20
Signal width W_s	W_{min}	x1, x5, x10, x20
Ground pitch P_g	P_{min}	x2, x16, x32
Ground width W_g	W_{min}	x1
Signal offset D_{off}		1/2
Line length	mm	0.5, 1, 1.5, 2

TABLE III
PARAMETER VARIATION TO DEFINE WIRING PROFILE "CRG". SIGNALS RUN IN PERPENDICULAR TO CELL ROW.

Parameter	Unit	Variation
Signal pitch P_s	P_{min}	x1, x5, x20
Signal width W_s	W_{min}	x1, x5, x20
Ground pitch P_g	P_{min}	x128, x256, x1024
Ground width W_g	W_{min}	x16, x32, x64
Signal offset D_{off}		0, 1/4, 1/2
Line length	mm	0.5, 1, 2

B. Parameter extraction and model generation

Clock frequency of 0.98 GHz and its typical signal slew t_r=102 ps are determined through simulation results of a fanout-of-four ring oscillator using predicted transistor models for 100 nm technology node [15]. The significant frequency f_s becomes 3.5 GHz from Eq. (1). Self and mutual inductance of the signals are extracted using a 3-D tool assuming the current through the signal returns using ground wires. The silicon substrate is modeled during capacitance extraction but ignored for resistance and inductance [2]. Then the RC and RLC wire models are constructed by cascading 100 μm length segments. Mutual capacitances between signal lines are included in both models but self and mutual inductances are used in the RLC models only. The minimum impedance ratios $R_0/(2\pi f_s L_0)$ are about 0.9 and 0.3 for cases CRC and CRG, respectively.

C. Circuit simulation to compare delays

Considering signal wire as an RC load, two types of driver are generated as resistance using the following policies:

Policy 1: Assume that the wire has been already divided sufficiently by repeater drivers. Driver resistance is determined to make driver delay and wire delay equal for minimizing total delay. Qualititatively, this policy uses smaller driver for larger RC loads.

Policy 2: Driver resistance of the driver is calculated so that the transition at the receiver becomes t_r. The

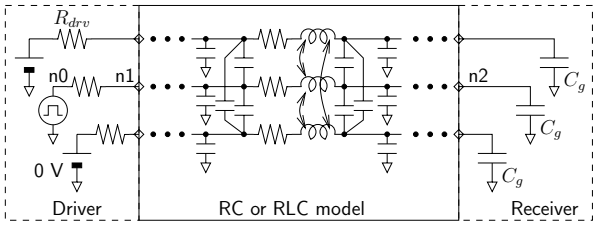

Fig. 3. Wire, driver, and receiver model connection for RLC model.

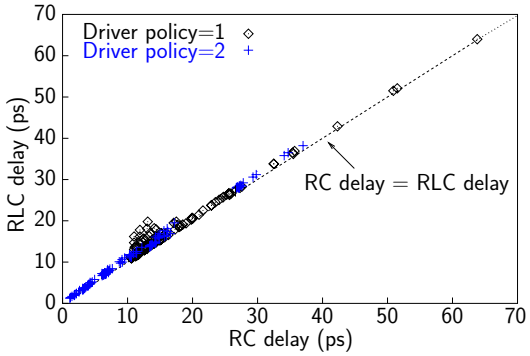

Fig. 4. Comparison between RC-delay and RLC-delay for CRC case.

driver size becomes roughly proportional to the RC load. Qualititatively, this policy uses larger drivers for larger RC loads.

As we vary wire width and pitch in a wide range of CRC and CRG cases, a full combination of the parameter variations includes unrealistic cases. For example, in driver design policy 1, wide, large pitched short wires that should have been used for longer distance connection are generated. Also for design policy 2, narrow, small pitched long wires which should have been divided by repeater drivers are included. In these cases, the automatic determination of the driver resulted in extremely small or minus resistance. We eliminated cases with unrealistically small driver resistance of less than $R_0/256$. Here, R_0 is the resistance of the minimum strength inverter in the technology.

For all except those invalid cases, circuit simulation calculates the delay using the same driver and receiver for both RC and RLC models. Fig. 3 illustrates the simplified schematic diagram for the RLC model. Three parallel signal lines use the same driver and receiver. The center driver sends a pulse with 1.2 V swing while the drivers for two neighboring signals are fixed to 0 V.

IV. Quantitative evaluation of the inductance impact on wire delay

A. Delay and waveform comparison

Fig. 4 compares RC and RLC delays for CRC, and Table IV summarizes delay difference between the models.

TABLE IV
Summary of RC- and RLC-delay difference.

Wire direction	CRC		CRG	
Driver design policy	1	2	1	2
Max. delay difference Δt (ps)	6.7	2.2	23.5	8.3
Relative error err (%)	51	20	169	132

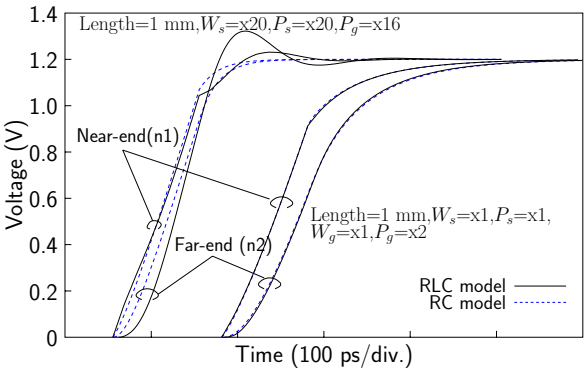

Fig. 5. Waveforms with and without inductance.

Parameter combinations in CRG are better in both delay difference Δt and percent delay difference err. This is not just because the variation is narrower, but CRG has a larger current loop than CRC. Here, we define err as

$$\Delta t = \text{RLC delay} - \text{RC delay} \quad (2)$$

$$err = \frac{\Delta t}{\text{RC delay}} \times 100 \quad (\%). \quad (3)$$

The cases with large RC delay tend to have small Δt since the resistance and capacitance rather than inductance are dominant for those cases. The opposite cases with small RC delay, which have smaller resistance or capacitance, suffered larger inductance impact. It is also shown in Fig. 4 that driver design policy strongly affects the magnitude of inductance effect. This implies that the optimum control of driver strength is required to reduce timing difference between the RC and RLC models.

Signal waveforms for the two extreme CRC cases with small and large Δt at near and far end of the wire are shown in Fig. 5. The driver design (policy 1) and the wire length (1 mm) are the same for the two cases. For the case with signal width W_s=x1, signal pitch P_s=x1, ground pitch P_g=x2, the delay difference Δt is 0.7 ps and percent delay difference err =2.5 %. Inductance has almost no impact since the resistance and capacitance are both large in this case. Whereas for the case with W_s=x20, P_s=x20, and P_g=x16, simulation resulted in Δt= 5.2 ps and err =47 %. Smaller wire load compared with the driver strength enhances inductance effect significantly, creating noticeable overshoot of the waveform at the end of the wire.

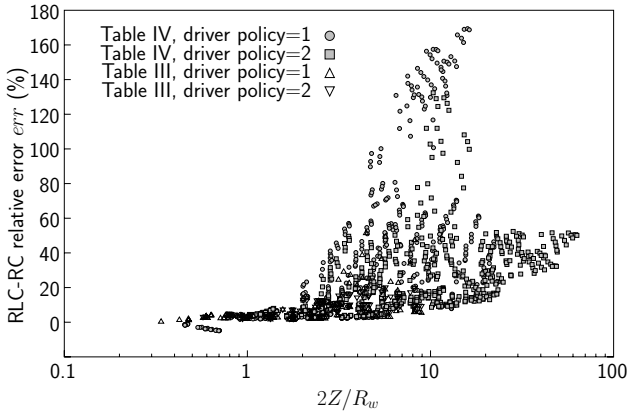

Fig. 6. Percent difference sorted by $2Z/R_w$.

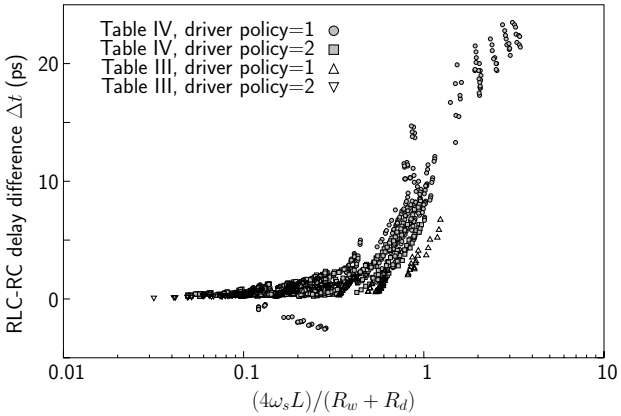

Fig. 7. Delay difference sorted by $\psi = (4\omega_s L)/(R_w + R_d)$.

B. Obtaining optimum screening rule

Several screening equations has been proposed to point out the wires with large inductance impact. Equation (4) appears in several references [2][5].

$$R_w \quad \leq \quad 2Z \tag{4}$$

Here $Z = \sqrt{L_w/C_w}$, and R_w, L_w, C_w are total resistance, inductance, and capacitance of the wire. Equation (4) relates to the dumping factor $\xi = 2Z/R_w$ of the RLC circuit. We can assign a critical dumping condition $\xi = 1$, where inductance should be taken into account when $\xi > 1$. Percent difference as a function of Eq. (4) is shown in Fig. 6 for all cases in this analysis. We understand Eq. (4) works well as a screening function. We can also figure out the optimal boundary of the inductance impact of 20 % from this graph. The threshold to screen inductance effect should be $2Z/R_w = 2$ in this example.

In [9], effect of the driver strength is included in the screening rule as:

$$R_w + R_d \quad < \quad m \cdot \omega_s L_w. \tag{5}$$

Here m is a constant to control test strictness. The scatter diagram for Δt with $\psi = (4\omega_s L)/(R_w + R_d)$ is illustrated in Fig. 7 ($m = 4$). We clearly see that including the driver strength into screening rule is important for accurate evaluation of inductance impact. This point will be analyzed again using RSF in the next section.

Through the comprehensive delay difference analysis described above, it becomes possible to evaluate the optimal screening equations or to determine constants to control the threshold value of test strictness.

V. Accurate difference prediction using RSF

Eq. (5) predicts trend of the delay difference well so that it looks to serve as a function to predict the timing difference of using the RC model instead of the RLC model. However, using Eq. (5) does not give a good estimate since Figs. 6 and 7 are currently multi-value functions even for the same value of variable $2Z/R_w$, and $(4\omega_s L)/(R_w + R_d)$.

In order to enhance the prediction accuracy, we newly propose a Response Surface Function (RSF) for percent delay error err' [7] as:

$$err' = \phi(x_1, x_2, \ldots, x_k) + \epsilon \tag{6}$$

using data collected in the procedures described in previous sections. Here x_i are predictor variables and ϵ is prediction error. We also propose two polynomial functions based on electrical and physical parameters as variables. Each function has practical use in different design phases.

A. Electrical parameter based approach

Fig. 8 compares the simulated delay difference and estimation using quadratic RSF based on electrical parameters (e-RSF) for case CRC,

$$err' = \beta_0 + \sum_{i=1}^{k} \beta_i x_i + \sum_{i=1}^{k} \beta_{ii} x_i^2 + \sum_{i<j} \beta_{ij} x_i x_j \tag{7}$$

where $\beta_0, \beta_i, \beta_{ii}, \beta_{ij}$ are the coefficients. The electrical parameters $1/R_w, 1/R_d, C_t(= C_w + C_g), 1/L_w$ and ψ are chosen as predictor variables x_i by consulting variables used in ψ. The terms which have small contributions to the difference estimation are eliminated using a t-test with confidence limit of 5 %. A good agreement of $R^2 = 0.9988$ and 0.9983 was achieved for both driver design policies 1 and 2 using parameter combination for CRC. coefficient adjusted for the degree of freedom. We can say that the proposed e-RSF can accurately predict and correct the delay difference using the RC wire model compared with using only ψ as the predictor variable for Eq. (7) that resulted in $R^2 = 0.8262$.

The coefficients β and t-values for a further simplified but still accurate ($R^2 = 0.9976$) RSF containing 11 terms are summarized in Table V. We see that ψ squared, ψ, and the ratio of inductive and resistive impedance of the wire L_w/R_w have large contributions to the delay difference.

Using e-RSF, we are not just able to point out the inductance dominant nets but can also predict the exact

TABLE V
COEFFICIENTS AND T-VALUE FOR PREDICTOR VARIABLES (FOR TABLE II, DRIVER DESIGN POLICY 1; $R^2 = 0.9976$)

Variable	coeff.	t	Variable	coeff.	t
ψ^2	5.2e+01	39.6	L_w/R_w	-1.4e+13	-13.8
ψ	8.8e+02	12.2	L_w/R_d	-5.8e+12	-9.5
ψ/R_w	2.4e+03	9.4	ψ/R_d	-2.4e+03	-9.2
L_w/C_t	-9.1e+09	-8.0	$1/(R_wC_t)$	-1.2e-10	-6.5
$1/(R_dC_t)$	1.2e-10	6.5	L_w	1.4e+09	6.1
β_0	-2.2e+00	-3.1			

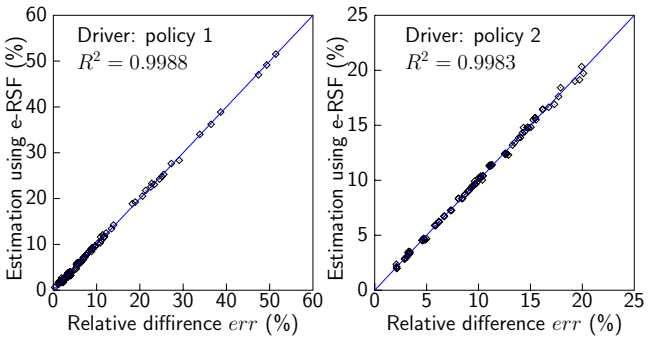

Fig. 8. Accurate difference estimation by the electrical parameter based screening rule for CRC.

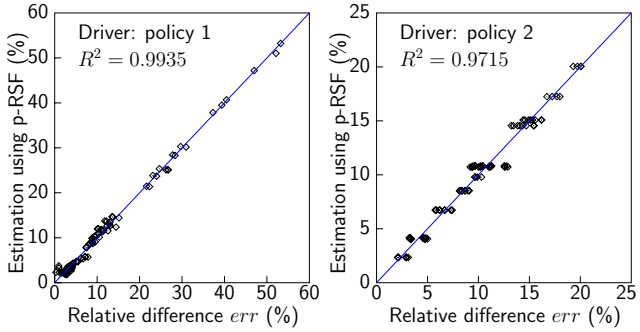

Fig. 9. The accuracy of the screening rule for CRC with physical parameters as variables.

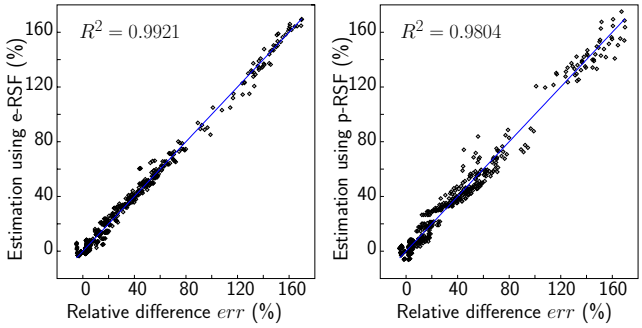

Fig. 10. The accuracy of the screening rule for CRG with electric and physical parameters as variables (driver: policy 1).

delay difference between using the RC and RLC models. e-RSF is suitably applied for accurate screening of the inductance-sensitive wires, delay difference estimation and correction when using the RC model in post-layout timing verification.

B. Physical parameter based approach

e-RSF can be accurate as far as the physical placement of the wires are determined. However, it is difficult to use e-RSF in earlier design stages such as floorplan optimization or routing, in which exact electrical parameters for each wire cannot be calculated. For use in this design phase, RSF using physical parameters as predictor variables (p-RSF) is more preferable.

Referring to the t-test results for e-RSF, physical parameters W_s, P_g, and $1/R_d$ are chosen as variables in this analysis. W_s corresponds to signal wire conductivity $1/R_w$, P_g roughly corresponds to wire inductance L_w which is determined by the distance to the nearest or equivalent distance to ground grid, and driver resistance $1/R_d$. Signal wire offset D_{off} is added as the variable for case CRG. Up to 3-rd order polynomials of Eq. (6) is used for constructing the p-RSF then backward elimination using t-test is executed to make the equation as simple as possible. The accuracy of the resulting p-RSF is presented in Fig.9 for CRC and Fig.10 for CRG. Although R^2 decreased slightly for driver design policy 2 for both CRC and CRG cases, sufficient accuracy required for the earlier design stages is achieved in this example. Constructing hierarchical RSFs, as described in [16][17], by subdividing the range of the predictor variable increased the accuracy. Even when the single RSF is constructed for both driver design policy, the RSF can still predict delay difference with $R^2 = 0.9606$ for CRC.

Although the wire structure shown in this paper is relatively limited, the concept can be applied to various process generation and technologies. Applying this idea for more general wires is reserved for future work. p-RSF can be conveniently used in the optimization of the grid placement or the definition of the design rule to control inductance effect. Also, the prediction equation enables on-the-fly determination of the inductance impact in interactive or automatic routing.

C. Example analysis and rule formulation using RSF

Using RSF, we gain insights for wiring design. In typical SoC design, wide wires are seldom used except for clock signals. Fig. 11 shows the relative delay difference when signal width W_s is limited to x1, x5, x10, and x20 for case CRC. Lines are from e-RSF, and symbols are data derived from SPICE simulations for reference. We can see that when the design rule limits signal wire width to less than x5, err is well controlled under 14%. When limiting wire width, different driver designs make only a small difference on delay. However, if wire width wider than x5 of the minimum is allowed, the difference starts to increase depending on the driver design. The delay difference due to inductance can be reduced to less than 20

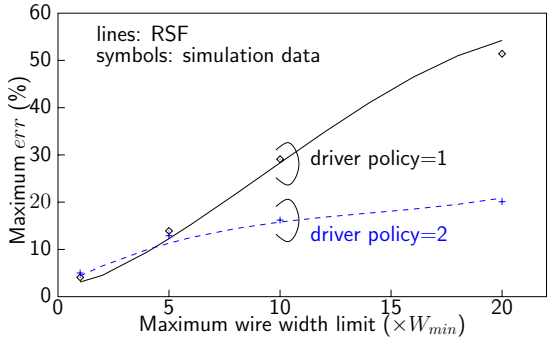

Fig. 11. Maximum relative delay difference as a function of the maximum signal wire width limit for CRC.

% even for the inductance dominant wires when driver design policy 2 is used. To keep inductance impact on delay small, controlling signal slew by choosing optimal driver size is important in addition to using the appropriate wire width.

VI. Conclusion

The methodology presented in this paper realizes quantitative understanding of the inductance impact on the delay difference between RC and RLC models. Although the wire structures presented in this paper are relatively limited, the concept can be applied to various process generation and technologies. Creating a comprehensive set of delay differences and the creation of a difference estimation RSF makes it possible to 1) build design guidelines to control inductance effects, 2) build screening functions using response surface method, and 3) estimate and correct possible error due to using the RC model instead of the RLC model, all optimized for the respective design process technologies or design styles.

To illustrate the use of proposed methodology, the impact of inductance is calculated for global interconnect of a 100 nm technology node with regular grid. Using the above calculated distribution of the RC and RLC delay difference, RSF of electrical and physical parameters as variables are constructed. Both RSF predicts delay difference accurately. Also through the example analysis, the following design considerations were derived for future SoC designs: 1) Relative delay is significantly reduced by limiting signal wire width to 5x of the minimum; and 2) controlling driver strength and wire width is the key to prevent inductance effects in the assumed process technology. Synthesizing an accurate screening rule of the inductance impact through exact timing difference distribution using the proposed methodology is found to be important for accurately estimating the need of taking into account inductance for a particular design.

Acknowledgement The authors would like to thank K. Hachiya of NEC corp., A. Ikeuchi of Toshiba, and T. Yoneda of Fujitsu VLSI with their fruitful discussion. The authors also express appreciation to the members of Desi-micron Design Study Group, EDA Technical Committee of Japan Electronics and Information Technology Industries Association.

References

[1] K. Gara, D. Blaauw, J. Wang, V. Zolotov, and M. Zhao, "Inductance 101: Analysis and design issues," in *Proc. DAC*, June 2001, pp. 329–334.

[2] A. Deutsch et. al., "On-chip wiring design challenges for gigahertz operation," *Proc. of the IEEE*, vol. 89, no. 4, pp. 529–555, April 2001.

[3] F. Dartu, N. Menezes, and L. Pillage, "Performance computation for precharacterized CMOS gates with RC loads," *IEEE Trans. on CAD*, vol. 15, no. 5, pp. 544–553, May 1996.

[4] A. E. Ruehli, "Inductance calculation in a complex integrated circuit environment," *IBM J. of Res. & Dev.*, pp. 470–481, Sept. 1972.

[5] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of merit to characterize the importance of on-chip inductance," in *Proc. DAC*, June 1998, pp. 560–565.

[6] Y.-C. Lu, M. Celik, T. Young, and L. T. Pileggi, "Min/max on-chip inductance models and delay metrics," in *Proc. DAC*, June 2001, pp. 341–346.

[7] W. G. Cochran and G. M. Cox, *Experimental Designs*, John Wiley & Sons, Inc., 2nd edition, 1957.

[8] Y. Cao, X. Huang, D. Sylvester, T.-J. King, and C. Hu, "Impact of on-chip interconnect frequency-dependent $R(f)L(f)$ on digital and RF design," in *Proc. IEEE International ASIC/SOC Conference*, 2002, pp. 438–442.

[9] C.-K. Cheng, J. Lillis, S. Lin, and N. Chang, *Interconnect Analysis and Synthesis*, John Wiley & Sons, Inc., 2000.

[10] R. K. Poon, *Computer Circuits Electrical Design*, Prentice-Hall international, 1995.

[11] Avant! corporation, *Raphael Reference Manual*, RA 2000.2 edition, 2000.

[12] M. Kamon, M. J. Tsuk, and J. K. White, "FASTHENRY: A multipole-accelerated 3-D inductance extraction program," *IEEE Trans. on MTT*, vol. 42, no. 9, pp. 1750–1758, Sept. 1994.

[13] K. Nabors, S. Kim, and J. White, "Fast capacitance extraction of general three-dimensional structures," *IEEE Trans. on MTT*, vol. 40, no. 7, pp. 1496–1506, July 1992.

[14] SIA, "International technology roadmap for semiconductors," 1999 Edition.

[15] Y. Cao, T. Sato, M. Orshansky, D. Sylvester, and C. Hu, "New paradigm of predictive cmos modeling for early circuit simulation," in *Proc. CICC*, May 2000, p. 9.3.

[16] H. Sato, Y. Ito, H. Kunitomo, H. BaBa, S. Isomura, and H. Masuda, "Delay library generation with high efficiency and accuracy on the basis of RSM," *IEICE Trans. Electron.*, vol. E83-C, no. 8, pp. 1295–1302, August 2000.

[17] D. C. Montgomery, *Design and analysis of experiments*, John Wiley & Sons, 2002.