Reduction of crosstalk noise by optimizing 3-D configuration of the routing grid

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Abstract - In this paper, we propose novel physical design techniques for a sub-quarter micron system-on-a-chip (SoC). By appropriately optimizing the routing grid space or the cell utilization ratio, the coupling effects are almost eliminated. By employing our proposed techniques on a 0.13μm six-layer physical design, the longest path delay is significantly decreased by 15% maximum without the need for process improvement. This significant delay reduction, which corresponds to a half generation of process progress, greatly accelerates the performance of SoCs.

I. Introduction

In the case of SoCs fabricated in sub-quarter micron or later nanometer-scale technologies, the interconnect delay is an important performance limiting factor [1]. The proportion of gate and line-to-substrate capacitance to the overall capacitance decreases while that of line-to-line capacitance increases. Therefore, on-chip crosstalk is now becoming manifest [2,3,4,5]. This causes logic errors [6] and delay variations because of signal distortion.

Another unwanted phenomenon of crosstalk is the large variation in effective line-to-line capacitance. If opposite-direction switching activity occurs in adjacent lines, the effective line-to-line capacitance will be doubled. By contrast, if same-direction switching activity occurs in adjacent lines, the line-to-line capacitance is considered to be nonexistent [7]. Because it is difficult to identify the state of the switching activity occurring between adjacent lines, timing constraints must be satisfied in both opposite- and same-direction switching. Therefore, timing closure becomes even more difficult if significant crosstalk noise occurs.

To reduce these unwanted effects, circuitry techniques have been proposed. In the cases reported in [8,9], crosstalk noise was reduced by inserting repeaters. In the case reported in [6], the variations in effective line-to-line capacitance were mitigated by inserting repeaters (inverters) between adjacent lines at staggered points. The circuitry changes would have a direct effect on timing and might result in an increased chip area. Insertion of repeaters at staggered points is effective mainly in making a handcrafted or semi-custom design. However, it is difficult to locate the most suitable insertion points if using an automatic place and route methodology.

Routing techniques were also proposed. One technique is to change the line width and space without changing the given line pitch [10,11]. By using this technique, line capacitance or line resistance change considerably when the line widths are greatly widened and as a result the timing is unfavorably affected. Another technique is to increase the distance to adjacent lines for chosen critical nets [12]. By using this method, the degree of congestion in un-chosen nets increases and as a result the overall crosstalk noise cannot be decreased. Another different technique is to establish a power line and other lines that have no electric-potential variations on either side of a noise-sensitive line for shielding [10,13,14]. By using this method, many wiring resources are required for shielding and the design complexity is also increased.

To solve these drawbacks, we propose new physical design techniques by simply optimizing the routing grid space or the cell utilization ratio for the automatic place and route methodology that is common in today's large-scale SoC design. The correlation between crosstalk noise and the layout-related settings are investigated for developing our techniques.

II. Techniques to Reduce Crosstalk

Line-to-line capacitive coupling between signal wires, which is the main cause of crosstalk noise, can be separated into two components, which are a horizontal line-to-line capacitance (C_H) and a vertical line-to-line capacitance (C_V). In the case reported in [15], the ratio of C_H to C_V is expressed as follows:

$$C_H / C_V = (AR)^n : \quad n \in [1,2] \tag{1}$$

where AR is the aspect ratio of the lines (the ratio of the length of line cross sections in the vertical direction to that in the horizontal direction). Based on the AR values in [3], the ratio of C_H to C_V in 0.13μm technology can be expressed as follows:

$$AR=3.0,\ C_H/C_V=3.0(\min),\ 9.0(\max) \tag{2}$$

As shown above, the horizontal line-to-line capacitance is three to nine times larger than the vertical line-to-line capacitance. Therefore, increasing the lateral line-to-line space is considered to be most effective.

We assume that our techniques are based on the grid-based model and the reserved layer model [16] that are generally used in automatic place and route methodology for today's large-scale SoC layouts. Therefore, to increase the lateral line-to-line space to reduce crosstalk, widening the routing grid space on the same layer seems to be the most attractive

approach. Because the grid space is calculated according to design rules, the smallest value is generally adopted for the grid space to increase the routing resources. However, if only this approach is employed, a shortage of routing resources results in an extraordinary increase in runtime or violations remaining at the detailed route stage. Especially, if employing the highest cell utilization ratio, the situation is still worse.

The objective of this study is to address the trade-off between crosstalk noise reduction and the shortage of routing resources. We propose two novel physical design techniques, one is optimizing 3-D configuration of the routing grid, and the other is optimizing the cell utilization ratio and the routing grid space simultaneously. The details of these techniques are elaborated in the subsequent sections.

A. Optimization for 3-D Configuration of the Routing Grid

To reduce the crosstalk of a layer that has many parallel segments of wire is an effective way of reducing the overall crosstalk. For this purpose, we increase the routing grid space for the automatic place and router. This technique has two features as follows:

(I) Increasing an individual layer's routing grid space in an incremental manner.

(II) In addition to (I), choosing appropriate layers for grid space widening by considering the trade-off between crosstalk noise reduction and routing resources.

These concepts are illustrated in Fig. 1. In this four metal layer example, we can control the widening of the grid space of Ma, Mb, Mc and Md independently. The algorithm for this technique is described in Fig. 2.

In this flow, various types of routing grid settings that vary the choice of layers (PT_LC) and the routing grid space (PT_GS) are prepared first. After executing the route for all patterns, several analyses are performed. First we count the number of crosstalk-violated nets (CN) for which the peak value exceeds the threshold. Secondly, the longest path delay (PD) and the runtime (RT) at the routing stage are measured. If RT exceeds the runtime threshold (TH_RT), we assume that it is impossible to complete the routing. After these analyses, a cost function (COST) is introduced to find the optimum routing grid settings (OPT_LC, OPT_GS) for minimizing the crosstalk effects within a reasonable runtime. We define COST as follows.

$$COST = CN^{\alpha} PD^{\beta} RT^{\gamma} \qquad (3)$$

Here, α, β and γ are weighting factors. The correlation between crosstalk noise, runtime and the routing grid settings can be checked for various patterns of the chosen layer and routing grid space. After that, the optimum grid settings (OPT_LC, OPT_GS) for the lowest COST value are obtained.

B. Co-optimization for Placement and the Routing Grid

Another approach to obtain the routing resources is to reduce cell congestion. For this purpose, we reduce the cell utilization ratio for the automatic place and router in accordance with widening the routing grid space. This technique has two features as follows:

(I) Preparing various types of placement data that vary the cell utilization ratio. The routing resources are equal between these data, in other words, the number of X direction tracks and Y direction tracks are equal between these data.

(II) After the routing is completed, crosstalk noise and static timing analysis are performed and as a result, the optimum cell utilization ratio can be found.

These concepts are illustrated in Fig. 3, in which both reducing the cell utilization ratio and widening the routing grid space are done simultaneously to keep the routing resource equal. The algorithm for this technique is described in Fig. 4.

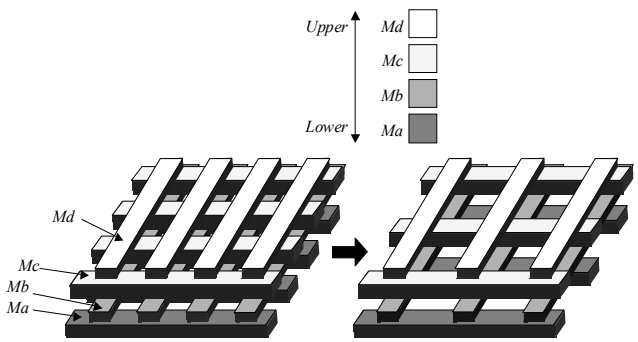

Fig. 1. Basic concept of optimization for 3-D configuration of the routing grid.

```
/* Definition of variables */
Inputs:     PT_LC[i]   ; layer choice patterns
            PT_GS[j]   ; grid space patterns
            TH_RT      ; threshold of routing runtime
Outputs:    OPT_LC     ; optimum layer choise
            OPT_GS     ; optimum grid space
Variables:  CN[i,j]    ; #crosstalk violated net
            PD[i,j]    ; longest path delay
            RT[i,j]    ; routing runtime
            COST[i,j]  ; cost function

/* Calculate cost and find optimum grid settings */
minCOST=COST[1,1], OPT_LC=PT_LC[1], OPT_GS=PT_GS[1];
for (i&j=1 to #patterns ){
   route based on PT_LC[i] and PT_GS[j] ;
   calculate CN[i,j], PD[i,j], RT[i,j];
   if (RT[i,j] < TH_RT) then{
     calculate COST[i,j] = f(CN[i,j], PD[i,j], RT[i,j]);
     if (COST[i,j] < minCOST) then {
       minCOST=COST[i,j], OPT_LC=PT_LC[i], OPT_GS=PT_GS[j];
}}}
```

Fig. 2. Algorithm of optimization for 3-D configuration of the routing grid.

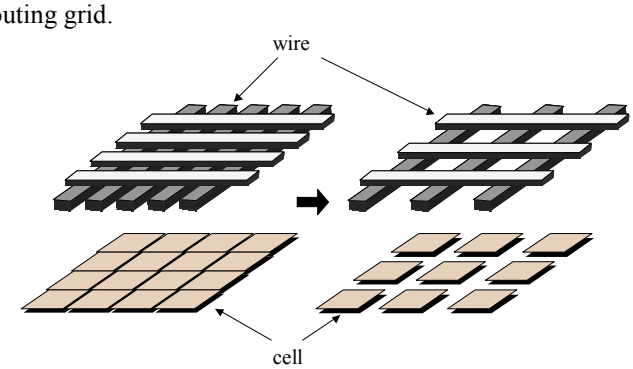

Fig. 3. Basic concept of co-optimization for placement and the routing grid.

```
/* Definition of variables */
Inputs:     PT_CU[i] ; cell utilization patterns
            TH_RT    ; threshold of routing runtime
Outputs:    OPT_CU ; optimum cell utilization ratio
Variables: CN[i]     ; #crosstalk violated net
            PD[i]    ; longest path delay
            RT[i]    ; routing runtime
            COST[i]  ; cost function

/* Calculate cost and find optimum cell utilization ratio */
minCOST=COST[1], OPT_CU=PT_CU[1];
for (i=1 to #patterns ){
   place and route based on PT_CU[i];
   calculate CN[i], PD[i], RT[i];
   if (RT[i] < TH_RT) then{
     calculate COST[i] = f(CN[i], PD[i], RT[i]);
     if (COST[i] < minCOST) then {
       minCOST=COST[i], OPT_CU=PT_CU[i];
} } }
```

Fig. 4. Algorithm of co-optimization for placement and the routing grid.

In this flow, various patterns that vary the cell utilization ratio (PT_CU) are prepared first. After executing place and route for all patterns, CN, PD, and RT are measured while monitoring RT to ensure that it does not exceed TH_RT. After these analyses, we introduce a cost function (COST) to find the optimum cell utilization ratio settings (OPT_CU). The definition of COST is the same as in equation (3). The OPT_CU that largely minimizes COST, in other words minimizes the CN and/or PD with little increase of RT should be obtained.

Regarding the wire's RC delay, the parasitic resistance (R_{wire}), vertical capacitance (C_V) and horizontal capacitance (C_H) are approximately expressed as follows [1].

$$R_{wire} = R_{unit} * L \quad (4)$$

$$C_V = C_{Vunit} * L \quad (5)$$

$$C_H = C_{Hunit} * L * S_p^{-1.34} \quad (6)$$

Here, R_{unit} is the resistance per unit length. C_{Vunit} and C_{Hunit} are the capacitances of the vertical and horizontal components per unit length. L and S_p are a wire's length and space, respectively.

Reducing the cell utilization ratio results in an increase in chip area so that it also results in an increase in the average wire length. From equations (4)-(6), R_{wire} and C_V increases if L increases. If S_p keeps the minimum value, C_H also increases if L increases. But if L and S_p increase simultaneously and the degree of increase of S_p is larger than L, C_H decreases. This fact means that another type of trade-off exists between the delay and the chip area.

III. Experimental Results

The proposed methods are used to layout an image processing circuit of the 100,000-instance scale fabricated in a 0.13µm CMOS process with six layers of copper interconnect.

A. Results of Optimization for 3-D Configuration of the Routing Grid

The routing grid space was increased in five steps from a value specified according to the minimum rule to a value twice as large. For this design, we defined two cases of layer selection for widening the grid space. One was choosing the third to sixth layers (case 1) and the other was the fourth to sixth (case 2). Since the pin pitch inside cells cannot be modified, the pitch of the first and the second layers was kept to the minimum value so as not to degrade the routing efficiency.

The crosstalk distribution for case 1 is shown in Fig. 5(a). From this, the number of crosstalk-violated nets (assuming the peak exceeded 30% of V_{DD}) was decreased by about one-eighth if we made the routing grid space twice as large as the minimum value. In case 2, as shown in Fig. 5(b), the number of crosstalk-violated nets was decreased by about one-third.

The results of the delay improvement for Clock l and Clock 2 are shown in Fig. 6. Clock 1 was operated at 72MHz and Clock 2 was at 114 MHz. By increasing the routing grid space, crosstalk-induced delay variations were reduced. Therefore, the longest path delay was decreased by 15% maximum in case 1 and 7% maximum in case 2.

The runtimes of case 1 and case 2, when the routing grid space was a maximum, were increased by a factor of eight and two, respectively, compared to when the space was a minimum.

For this design, a pitch of 1.5 in case 1 was the best solution for achieving the maximum delay improvement (max 15%) with little runtime penalty (within fourfold). If the grid space was widened by more than 1.5, the improvement seemed to saturate. One reason for this is the increase of detour or off-grid routing due to the shortage of routing resources.

B. Results of Co-optimization for Placement and the Routing Grid

At the beginning of this design flow, we prepared four patterns in which the cell utilization ratio was varied from 40% to 70% in four steps. We observed that this ratio was increased by 3-5% from the default value in each pattern after performing clock tree synthesis and fixing transition violations.

To validate the effectiveness of this approach, we prepared sub-patterns for each utilization ratio setting, one in which the routing grid spaces were widened to keep the routing resources equal in each pattern (case 3), another in which the minimum value of the routing grid space was retained (case 4). In case 3, we selected layers from the third to the sixth for widening. The number of X and Y tracks was defined that would enable routing in the most highly congested pattern. In this example, the highest cell utilization ratio was 70%.

The results of the delay improvement compared to the default settings, which is a 70% cell utilization ratio with the minimum routing grid space, at Clock l and Clock 2 for each setting are shown in Fig. 7. In case 3, the longest path delay was decreased by 5% maximum for Clock 1 and 7% maximum for Clock 2 with a 50% and 60% cell utilization ratio, respectively, because of the large reduction in crosstalk noise. In case 4, however, the longest path delay was decreased by 2% maximum for Clock 1 and 3% maximum for Clock 2 with a 60% and 40% cell utilization ratio, respectively, because of the small reduction in crosstalk noise.

As for the runtimes, no significant difference was observed between the four ratio settings. Furthermore, no significant difference was observed between with and without widening the routing grid space.

For this design, a 50% cell utilization ratio and widening the routing grid space was the best solution for achieving the maximum delay improvement (5% for Clock 1 and 8% for Clock 2) with no runtime penalty.

C. Summary of Delay Improvement

The maximum improvement in the delay by employing the two proposed techniques is summarized in Fig. 8. From these results, both techniques can reduce delay once the optimum cell utilization ratio and routing grid settings are obtained.

IV. Conclusions

In this study, we demonstrated that coupling effects can be reduced by simply optimizing the parameters for automatic place and router. Experimental results showed that our two proposed techniques proved to be effective in reducing crosstalk noise within a reasonable runtime. From the experiments, the longest path delay was decreased by 15% maximum if the proposed techniques were employed. This 15% delay improvement corresponds to a half generation of process progress. Further improvement can be expected if we use both techniques simultaneously.

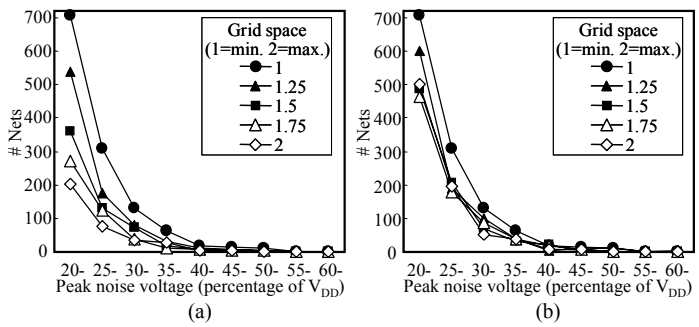

Fig. 5. Crosstalk noise vs. routing grid in (a) case1, (b) case 2.

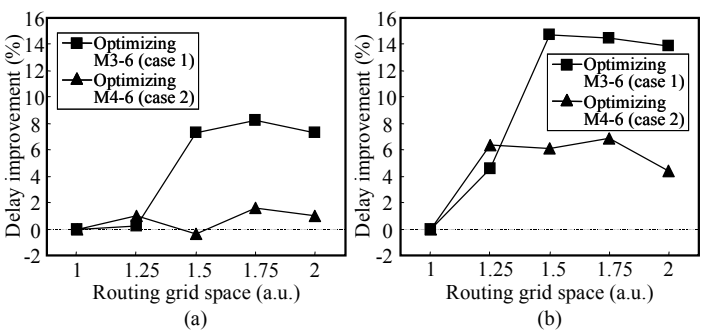

Fig. 6. Delay improvement by optimizing the 3-D configuration of routing grid, (a) Clock 1(72MHz), (b) Clock 2(114MHz).

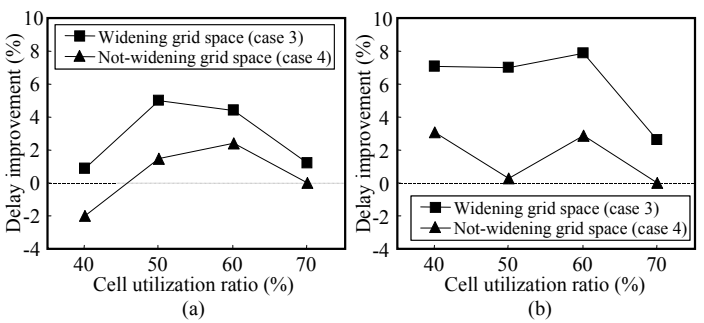

Fig. 7. Delay improvement by co-optimizing the placement and routing grid, (a) Clock 1(72MHz), (b) Clock 2(114MHz).

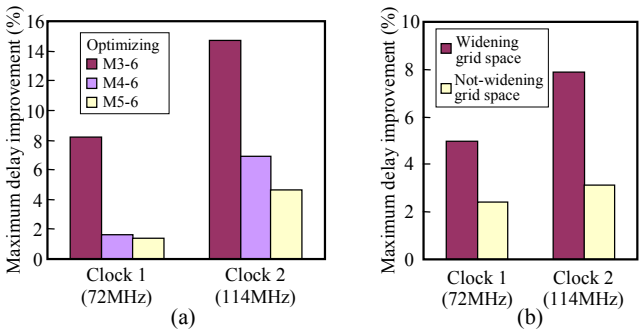

Fig. 8. Summary of Delay Improvement, (a) 3-D routing grid optimization, (b) Co-optimization.

References

[1] H. B. Bakoglu, "Circuits, Interconnections, and Packaging for VLSI," *Addison-Weslay Publishing Company Inc*, 1990.

[2] L. Gal, "On-Chip Cross Talk – the New Signal Integrity Challenge," *Proceedings of CICC'95*, pp. 251-254, 1995.

[3] J. Cong, L. He, K.-Y. Khoo, C.-K. Koh, and Pan Z., "Interconnect Design for Deep Submicron ICs," *Proceedings of ICCAD'97*, pp. 478-485, 1997.

[4] D. Sylvester and K. Keutzer, "Getting to the Bottom of Deep Submicron," *Proceedings of ICCAD'98*, pp. 203-211, 1998.

[5] International Technology Roadmap for Semiconductors 2001 Edition, http://public.itrs.net/Files/2001ITRS/Home.htm.

[6] P. Larsson and C. Svensson, "Noise in Digital Dynamic CMOS Circuits," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 655-662, 1994.

[7] A. B. Kahng, S. Muddu, and D. Vidhani, "Noise and Delay Uncertainty Studies for Coupled RC Interconnects," *Proceedings of IEEE ASIC/SOC conference*, pp. 3-8, 1999.

[8] D. Li, A. Pua, P. Srivastava, and U. Ko, "A Repeater Optimization Methodology for Deep Sub-Micron, High-Performance Processors," *Proceedings of ICCD'97*, pp. 726-731, 1997.

[9] C. J. Alpert, A. Devgan, and S. T. Quay, "Buffer Insertion for Noise and Delay Optimization," *Proceedings of DAC'98*, pp. 362-367, 1998.

[10] A. B. Kahng, S. Muddu, E. Sarto, and R. Sharma, "Interconnect Tuning Strategies for High-Performance ICs," *Proceedings of DATE'98*, pp. 471-478, 1998.

[11] J. Cong, L. He, C.-K. Koh, and Z. Pan, "Global Interconnect Sizing and Spacing with Consideration of Coupling Capacitance," *Proceedings of ICCAD'97*, pp. 628-633, 1997.

[12] C. Nicoletta, J. Alvarez, E. Barkin, C.-C. Chao, B. R. Johnson, F. M. Lassandro, P. Patel, D. Reid, H. Sánchez, J. Siegel, M. Snyder, S. Sullivan, S. A. Taylor, and M. Vo, "A 450-MHz RISC Microprocessor with Enhanced Instruction Set and Copper Interconnect," *IEEE Journal of Solid-State Circuits*, pp. 1478-1491, 1999.

[13] S. P. Khatri, A. Mehrotra, R. K. Brayton, and A. Sangiovanni-Vincentelli, "A Novel VLSI Layout Fabric for Deep Sub-Micron Applications," *Proceedings of DAC'99*, pp. 491-496, 1999.

[14] James D. Z. Ma, and L. He, "Formulae and Applications of Interconnect Estimation Considering Shiled Insertion and Net Ordering" *Proceedings of ICCAD'2001*, pp. 327-332, 2001.

[15] F. Dartu and L. T. Pileggi, "Calculating Worst-Case Gate Delays Due to Dominant Capacitance Coupling," *Proceedings of DAC'97*, pp. 46-51, 1997.

[16] N. Sherwani, "Algorithms for VLSI Physical Design Automation Second Edition," Kluwer Academic Publishers, 1995.