A Fast and Accurate Method for Interconnect Current Calculation *

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Abstract - As VLSI technology continues to scale down, electromigration problem has become one of the dominant factors in determining system reliability. This problem is caused by high current density flowing in the metal interconnect. Therefore, current evaluation is a crucial concern in IC design. SPICE level circuit simulators are excellent for doing current calculation, however, their running time are too expensive to be used repeatedly in design synthesis loops. In this paper, we propose an efficient approach for the interconnect current calculation. This method is based on moment matching but does not need high order moments. It only needs traversing the *RC* **tree once to get the mean current value of every segment, traversing the tree once more is enough for the RMS current calculation, and two more traversals is sufficient for the peak current calculation. We apply our method to a larger number of interconnects getting close-to-SPICE accuracy at significantly faster runtimes. In particular, applying the method to 17,387 wire segments in the clock tree of a commercial IC, we obtained that the average deviation error of mean current is 0.0569%, average RMS current error is 0.703% and average peak current error is 6.552%. It took 28 hours for HSPICE to get current value of all the wire segments and it only took our method 156 seconds.**

I. Introduction

 In recent years, while the feature size of integrated circuits are being scaled down dramatically [10,11], however, the working voltage and current are not reduced at the same rate as IC physical dimensions. Consequently, the current density of interconnect is increased as the physical size of IC is reduced. Interconnect with insufficient width may cause large current density and be subject to electromigration problem [4,17]. Eventually, this problem may cause the failure of the IC during any time in its lifetime [1,5]. Therefore, the evaluation of current which flows through the interconnect is becoming one of the critical concerns in IC design and will take much more attention in the future nanometer technology.

 Circuit simulators, such as SPICE, are excellent for the accurate current calculation. However, the calculation is based on the time-varying waveform, thus their running times are very expensive, especially for the VLSI design in which millions of current value verification are required during the IC design process. Moreover, even to do the electromigration analysis only on the critical nets of a VLSI circuit, it still takes unaffordable time for running SPICE simulation. Therefore, it is important to develop a method that is able to compute current value of interconnects with fast speed. Besides, it is required that the method is able to compute not only the RMS current but also the average and peak current because, with the developing of techniques on electromigration analysis, these three kinds of current values are needed in different analysis models [3,6,14].

 There are several electromigration analysis tools proposed in recent years, however, they either are based on the SPICE level simulators [15,16] or only focus on the power network analysis [2,12]. With the operating frequency of IC increasing and physical dimension scaling down, current densities of signal nets are getting much higher than ever. Besides, the topology complexity of signal network as well as the commercial competitive pressure pushes IC design to the limits of fabrication technology. All these make the evaluation of current density of signal nets imperative to prevent the electromigration problem from becoming a time bomb in the ICs. Thus, most chip fabrication companies require their IC design tools to have the ability to calculate the current density of both signal and power nets in order to verify there is no electromigration problem and Joule heating failure occurring.

 In this paper, we present an efficient method to calculate the mean, RMS and peak current values of signal nets. The basic technique used in this method is moment matching [8], and moreover, it does not need high order moments for the current calculation. Thus the running time of our method is much less than that of the SPICE-level simulator. To get the mean current value of every segment in an interconnect *RC* tree, it only needs to traverse the tree once, for calculating every segment's RMS current, traversing the tree once more is enough and for the peak current value calculation, two more traversals is sufficient. The error of our method on the mean current value calculation is less than 1.93% as compared to SPICE simulation, and within 7.82% of SPICE

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accuracy for the RMS current calculation and, for the peak current calculation, the error is less than 16.65%. Since this method is efficient and easy to implement, in addition, its accuracy and fidelity is reasonable, it may become a preferable tool to use in the VLSI design for fast current evaluation.

II. Interconnect Current Calculation

 Given an *RC* tree with nodes {1, …, *n*}, where node 1 is the driving point, we refer to it as the root and denote r_1 as the driver output resistance, as shown in Fig. 1. We apply the switch-resistor model to the driving gate. Thus, the driving gate is modeled by a step voltage source and its driving resistance r_1 .

Assuming that node *h* is the direct parent of node *i*, let R^i denote the resistance between the node h and i . Let $Cⁱ$ be the capacitance at the node *i*. Denote m_j^i as the *j*th moment of the impulse response at node *i*. Thus, The voltage between nodes *h* and *i* is

$$
V^{h}(s) - V^{i}(s) = \frac{1}{s} \Big[(m_{0}^{h} - m_{0}^{i}) + (m_{1}^{h} - m_{1}^{i})s + (m_{2}^{h} - m_{2}^{i})s^{2} + ... \Big]
$$

= $I^{i}(s) \cdot R^{i}$ (1)

where $V^h(s)$, $V^i(s)$ are the *s*-domain voltage of node *h* and *i* respectively, $I^i(s)$ is the *s*-domain current that flows through the resistor R^i .

 Equation (1) can be expressed by a reduced set of *q* poles and residues as follows:

$$
I^{i}(s) \cdot R^{i} = \frac{1}{s} \sum_{i=1}^{q} \frac{r_{i}^{i}}{s - p_{i}^{i}}
$$
 (2)

where p_1^i to p_q^i are the *q* poles of node *i* and r_1^i to r_q^i are their corresponding residues.

In time domain, the current $I^i(t)$ can be expressed as

$$
I^{i}(t) = \frac{1}{R^{i}} \sum_{i=1}^{q} \frac{r_{i}^{i}}{p_{i}^{i}} e^{p_{i}^{i}t}
$$
 (3)

Fig. 1. *RC* tree. Node *h* is the direct parent node of *i*, R^{i} is the resistance between the node \hat{h} and *i*, C^{i} is the capacitance at the node *i*.

Let
$$
k_i^i = -\frac{r_i^i}{p_i^i}
$$
, equation (3) can be rewritten as:

$$
I^{i}(t) = \frac{1}{R^{i}} \sum_{i=1}^{q} (-k_{i}^{i} e^{p_{i}^{i} t})
$$
 (4)

We will refer to those k_l^i as the residues in the rest of this paper to make for brevity.

A. The Value of Mean Current

Let I_{mean}^i denote the value of mean current that flows through *Ri* . Let *T* be the period of time during which the mean current value is calculated.

$$
I^{i_{mean}} = \frac{1}{T} \int_0^T I^{i}(t) dt = \frac{1}{T} \int_0^T \frac{1}{R^{i}} \sum_{l=1}^q \left(-k_l^{i} e^{p_l^{i} t} \right) dt
$$

$$
= \frac{1}{T} \frac{1}{R^{i}} \sum_{l=1}^q \left(-\frac{k_l^{i}}{p_l^{i}} (e^{p_l^{i} T} - 1) \right)
$$
(5)

 We assume that the input signal switches at the starting time 0 and the voltage of all the capacitors becomes stable at the end of *T. T* can be the cycle time of input signal. Usually the time needed for the interconnect capacitors charging or discharging is much less than the input signal period. Under this assumption, $e^{p_i^T T}$ is much less than 1 and closer to 0 since p_l^i <0. Thus, (5) can be rewritten as:

$$
I^{i}{}_{mean} = \frac{1}{T} \cdot \frac{1}{R^{i}} \cdot \sum_{l=1}^{q} \frac{k_{l}^{i}}{p_{l}^{i}}
$$
(6)

In the *q*-pole system, the following equation is satisfied for the current transfer function (1) [8]:

$$
\sum_{l=1}^{q} \frac{k_i^{i}}{p_i^{i}} = m_1^{h} - m_1^{i}
$$
 (7)

For signal interconnects, most topologies of the wire circuits are tree structure. If so, (7) can be expressed as

$$
m_1^{\;h} - m_1^{\;i} = R^i \cdot C_{td}^{\;\;i} \tag{8}
$$

where C_{td}^{i} is the total downstream capacitance seen from node *i*.

Substituting the above equation into (7) and (6), the mean current can be rewritten as

$$
I^i_{mean} = \frac{1}{T} \cdot \frac{1}{R^i} \cdot R^i \cdot C_{td}^i = \frac{C_{td}^i}{T}
$$
 (9)

 It is obvious that we only need to traverse the *RC* tree once for getting the total downstream capacitance of every node by performing a reverse depth-first traversal beginning at any leaf node [9]. This traversal algorithm guarantees that a node is not visited until the total downstream capacitance of every its descendant gets known. We refer to this traversal as the *first traversal*.

We will use m_1 to denote the first order moment for a generic node and similarly, *mj* as *j*th moment value. We define Δm_1 as the m_1 's difference between a node and its direct parent node, similar is the definition of Δm_2 and Δm_3 . Equation (8) shows that Δm_1 is equal to the resistance multiplying its total downstream capacitance. Thus, during the first traversal, we can obtain every node's Δm_1 value simultaneously. If all the m_1 's differences are summed from the leaf to the root, the difference between the root and each leaf is obtained. Besides, m_1 value of the root can be obtained when finishing the traversal since it is only related to r_1 and the total downstream capacitance seen from the root. Therefore, without much extra work, the m_1 value of every leaf node and Δm_1 value of every node can all be computed during the first traversal. These values are useful in the following current calculation.

B. The Value of RMS Current

Let $Iⁱ_{rms}$ denote the RMS current value that flows through the R^i . By the definition of RMS current and equation (4),

$$
I^{i_{rms}} = \sqrt{\frac{1}{T} \int_{0}^{T} I^{i^{2}}(t) dt} = \sqrt{\frac{1}{TR^{i^{2}} \cdot \int_{0}^{T} (\sum_{l=1}^{q} -k_{l}^{i} e^{p_{l}^{i} \cdot t})^{2} dt}
$$

$$
= \sqrt{\frac{1}{TR^{i^{2}}} \int_{0}^{T} \left(\sum_{l=1}^{q} (k_{l}^{i})^{2} e^{2p_{l}^{i} \cdot t} + \sum_{l=1}^{q} \sum_{m=1}^{q} k_{l}^{i} k_{m}^{i} \cdot e^{(p_{l}^{i} + p_{m}^{i}) \cdot t} \right) dt}
$$
(9)

Taking the same assumption of *T* as that in subsection *A*, we can rewrite equation (9) as follows

$$
I^{i}{}_{rms} = \sqrt{\frac{1}{TR^{i^{2}}}} \cdot \left(-\sum_{l=1}^{q} \frac{(k_{l}^{i})^{2}}{2 p_{l}^{i}} - \sum_{l=1}^{q} \sum_{\substack{m=1 \ m \neq l}}^{q} \frac{k_{l}^{i} k_{m}^{i}}{p_{l}^{i} + p_{m}^{i}} \right)
$$
(10)

Assuming that p_1^i is the dominant pole of node *i*, I^i_{rms} can be approximated as

$$
I^{i_{rms}} = \sqrt{\frac{1}{TR^{i^2}} \cdot \left(-\frac{(k_1^{i})^2}{2p_1^{i}}\right)}
$$
(11)

Since p_1^i is the dominant pole of node *i*, we can take the following approximations [8]:

$$
\frac{k_1^{i}}{p_1^{i}} = m_1^{h} - m_1^{i}
$$
 (12)

$$
\frac{k_1^i}{(p_1^i)^2} = m_2^h - m_2^i
$$
 (13)

From the above two equations (12) and (13), we get

$$
p_1^i = \frac{\frac{k_1^i}{p_1^i}}{\frac{k_1^i}{(p_1^i)^2}} = \frac{m_1^h - m_1^i}{m_2^h - m_2^i}
$$
 (14)

and

$$
k_1^i = \frac{\left(\frac{k_1^i}{p_1^i}\right)^2}{\frac{k_1^i}{(p_1^i)^2}} = \frac{(m_1^h - m_1^i)^2}{m_2^h - m_2^i}
$$
 (15)

Thus, I^i_{rms} can be expressed as

$$
I^{i}{}_{rms} = \sqrt{\frac{1}{TR^{i^{2}}}} \cdot \left(-\frac{(m_{1}^{h} - m_{1}^{i})^{3}}{2 \cdot (m_{2}^{h} - m_{2}^{i})} \right)
$$
(16)

In an *RC* tree,

$$
m_2^{\ b} - m_2^{\ i} = R^i \cdot \sum_{s \in D(i)} C^s m_1^{\ s} = R^i \cdot C m_1^{\ i} \tag{17}
$$

where $D(i)$ denotes the nodes set consisting of *i* and its descendant nodes. Cm_1^i is the value of each node's capacitance multiplying its corresponding m_1 value summed from all the descendant of *i* to node *i* [7].

Substituting (8) and (17) into (16) , we get

$$
I^{i_{rms}} = \sqrt{-\frac{(C_{ul})^3}{2T \cdot Cm_1^{i}}}
$$
 (18)

Equation (18) shows that it needs C_{td}^i and Cm_1^i to calculate RMS current. C_{td} ^{*i*} of every node has been obtained in the mean current calculation. Moreover, since we also know the *m*1 value of every leaf in the *first traverse*, we can traverse the tree once more (*second traversal*) to get all the other nodes m_1 value and Cm_1^i can also be obtained at the same traversal by using equation (17). Thus, based on the mean current calculation, it needs only one more traversal to yield the RMS current value of every node.

Similar to subsection *A*, Δm_2 value of every node and m_2 value of every leaf can be obtained simultaneously in the *second traversal*. These values will be used in the peak current calculation.

C. Peak Current Value

 In this subsection, we will use two poles approximation to calculate the peak current value. The reason why we do not use the dominant pole method to get the peak current value is explained later as a remark.

The *s*-domain voltage of nodes *i* is

$$
V^{i}(s) = \frac{1}{s} \left(m_{0}^{i} + m_{1}^{i} \cdot s + m_{2}^{i} \cdot s^{2} + ... \right)
$$
 (19)

By using two poles approximation, we transform the voltage of nodes *i* from *s*-domain to time domain.

$$
V^{i}(t) = 1 - k_{1}^{i} e^{p_{1}^{i}t} - k_{2}^{i} e^{p_{2}^{i}t}
$$
 (20)

Similarly we can get the time domain voltage of node *h*

$$
V^h(t) = 1 - k_1^h e^{p_1^h \cdot t} - k_2^h e^{p_2^h \cdot t}
$$
 (21)

With the two terminals' voltage of the resistor R^i , the current flowing through it can be expressed as

$$
I^{i}(t) = \frac{1}{R^{i}} \left[V^{h}(t) - V^{i}(t) \right]
$$

=
$$
\frac{1}{R^{i}} (k_{1}^{i} e^{p_{1}^{i}t} + k_{2}^{i} e^{p_{2}^{i}t} - k_{1}^{h} e^{p_{1}^{h}t} - k_{2}^{h} e^{p_{2}^{h}t})
$$
 (22)

 The maximum value equation of (22) is the peak current value flowing through R^i . Thus, the rest part of the problem on calculating peak current value becomes how to get the values of the two poles and two residues of (22). An explicit and stable method for the two poles approximation was proposed by Tutuianu *et al.* [13], however, the method does not work well at the nodes near the driving point. Therefore, we use the classical moment-matching method of AWE to compute the poles and residues for those near driver segments. This method works very well at the near driving point nodes. Consequently, the two methods can compliment each other over all the nodes. We summarize our method to calculate the two poles and residues for equation (22) as follows:

1. *For those near driver nodes*: (i). Solve the matrix equations to get b_1 and b_2 ; $\begin{vmatrix} 1 & m_1 \\ \frac{i}{2} & \frac{i}{2} \end{vmatrix} = - \begin{vmatrix} m_2 \\ \frac{i}{2} & \frac{i}{2} \end{vmatrix}$ $\overline{}$ $\left|m_{2}^{i}\right|$ \lfloor $\begin{bmatrix} b_2 \\ b_1 \end{bmatrix} = -$ L $\overline{}$ $\overline{}$ $\begin{vmatrix} 1 & m_1^i \\ i & i \end{vmatrix}$ $\mathsf{L}% _{0}\left(\mathcal{N}\right)$ L *i i i i i m m b b* m_1^{\prime} *m m* 3 2 1 2 1 $\frac{1}{2}$ 1 m_1

(ii). Get the two roots of the following quadratic function;

 $b_2 x^2 + b_1 x + 1 = 0$

- (iii). The root with smaller absolute value is the poles p_1^i and the other one with larger absolute value is p_2^i ;
- (iv). Residues..

$$
k_{1}^{i} = \frac{(m_{2}^{i})^{3}}{(m_{3}^{i})^{2}}
$$
 $k_{2}^{i} = 1 - k_{1}^{i}$

i

2. *For the other nodes:*

$$
p_1^i = \frac{m_2^i}{m_3^i}
$$
\n
$$
p_2^i = p_1^i \left(\frac{\frac{1}{m_1^i} - \frac{m_1^i}{m_2^i}}{\frac{m_1^i}{m_2^i} - \frac{m_2^i}{m_3^i}} \right)
$$
\n
$$
k_1^i = \frac{1 - m_1^i \cdot p_2^i}{p_1^i - p_2^i} p_1^i
$$
\n
$$
k_2^i = \frac{1 - m_1^i \cdot p_1^i}{p_2^i - p_1^i} p_2^i
$$

The above method indicates that m_3 , m_2 and m_1 are required for calculating the two poles and residues. Every node's m_1 value is obtained in the *second traversal*. Besides, we obtain the Δm_2 value of every node and the m_2 value of every leaf. Therefore, by one more traversal, we can get all nodes' m_2 value. In the same traversal, we can compute Δm_3 value of every node using the same method as that in the above subsection. When this traversal is finished, we can also obtain the m_3 value of the root. Thus, by another traversal of the tree, we can get m_3 value of every node. Therefore, based on mean and RMS current calculation, two more traversal is sufficient for the peak current calculation.

 We summarize the four traversals for calculating the three kinds of current values in Table 1. The symbol with superscript *i* in table 1 represents that its associated value can be obtained at every node in the traversal.

 If we take the coupling capacitance into consideration, the topology of the circuit of interconnect may become tree-like. Defining the notion tree-like topology as: Excluding all capacitors and current sources, if a spanning tree of the circuit can be constructed that includes all voltage sources and resistors, and then the circuit topology is strictly tree-like [9]. The equation (8) and (17) may not be satisfied in the tree-like topology. Thus, to calculate mean current, we need to get m_1 value of every node and it needs two complete traversals to get all m_1 's value. One traversal is to compute the first moment current flowing through all the capacitors and the other traversal is to get all node moment voltages. Similarly, for RMS current calculation, it needs another two traversals to obtain every node's m_2 value. The situation is the same for peak current calculation and it still needs two more traversals to get all m_3 's value based on the RMS current computation. Hence, six traversals are needed for the tree-like topology interconnect to get all the three kinds of current values.

Remark 1:

 To calculate peak current, using only one dominant pole approximation is not enough to get an accurate result. The reason is that RMS value is the statistical result during the time interval of computational, i.e. it is the integral of $I^i(t)$ on the time interval *T*. The waveform derived from the dominant pole technique matches most area of the actual current curve but not fitting good around the time starting point, i.e. $t=0^+$ area [8]. To calculate the peak current value, we need more specific information than that needed for RMS value, especially at near $t=0^+$ zone since the current reaches its maximum value usually in this region. Thus we use two approximation poles instead of one dominant poles to extract more information around $t=0^+$ area.

TABLE 1 Values obtained in each traversal

first		m_1^{μ} - m_1^{μ}		m_1 of every leaf
second	m ₁	Cm_1^i	m_2^h - m_2^h	m_2 of every leaf
third	m _o	m_3^{μ} - m_3^{μ}		m_3 of every leaf
fourth	m ₃			

III.EXPERIMENTAL RESULTS

 We applied our method to the clock tree of a commercial IC and compared the calculation results with HSPICE simulation. There are 17,387 segments in the clock tree. For all these segments, the maximum and average deviation errors of mean, RMS and peak current calculations are shown in Table 2.

 All the experiments are performed in a SUN *Ultra* workstation. It takes 28 hours for HSPICE to finish the current calculation of all the segments and our method uses 156 seconds to yield all the results.

TABLE 2

 The maximum and average deviation error of this method compared with HSPICE simulation on mean, RMS and peak current computations of the clock tree of a commercial IC.

 Furthermore, we generate 2000 VLSI wires with wide range parameters and different tree topologies to test our method. The wire parameters are based on the current and future manufactory technology [10,11]. It takes our method 9 minutes to finish the current calculation of every segment of those wires and it takes HSPICE 105 hours to do all the simulations. The results demonstrate that the maximum deviation error is less than 1.93% compared to HSPICE simulation for the mean current value calculation, less than 7.82% for the RMS current calculation and, for the peak current calculation, it is less than 16.65%. Fig. 2, 3 and 4 show that how many segments among the 2000 wires distribute in the different error percentages of mean, RMS and peak current calculation, respectively.

Fig. 2. The relationship between the number of segments and the error percentages of mean current calculation over the 2000 wires.

Fig. 3. The relationship between the number of segments and the error percentages of RMS current calculation over the 2000 wires.

Fig. 4. The relationship between the number of segments and the error percentages of peak current calculation over the 2000 wires.

IV. CONCLUSION

 Based on the moment-matching technique, a method on calculating interconnect current is presented. The method works efficiently on mean, RMS and peak current calculation compared to other circuit simulators and the results it yields are within reasonable error range. This method can calculate current value for IC interconnect whose topology is a spanning *RC* tree or tree- like. We will extend our research on current calculation to interconnect with resistance loops and inductance loops in the future work.

REFERENCES

- [1] David Gibson, "Statistical reliability prediction," *Integrated Reliability Workshop, 1995. Final Report.*, pp. 161, Oct. 1995.
- [2] C.X. Huang; B. Zhang; An-Chang Deng; B. Swirski, "The design and implementation of PowerMill", *Proc. Intl. Workshop Low-Power Design*, pp. 105--110, Apr. 1995.
- [3] B.-K. Liew; N.W. Cheung; C. Hu, "Projecting interconnect eletromigration lifetime for arbitrary current waveform," *IEEE Trans. on Electron Device*s, vol.37, pp.1343-1351, 1990.
- [4] B.-K. Liew; P. Fang; N.W. Cheung; C. Hu, "Circuit reliability simulator for interconnect, via, and contact electromigration", ," *IEEE Trans. Electron Devices*, vol. 39, pp. 2472-2479, Nov. 1992.
- [5] Ping-Chung Li, Young, T.K, "Electromigration: the time bomb in deep-submicron ICs", *IEEE Spectrum*, Vol. 33 Sept., pp 75 –78, 1996.
- [6] J. A. Maiz, "Characterization of Electromigration Under Bidirectional (BC) and Pulsed Unidirectional (PDC) Currents", *Proc. of Intl. Reliability Physics Symposium*, pp. 220-228, 1989.
- [7] Noel Menezes; Satyamurthy Pullela; Florentin Dartu; Lawrence T. Pillage, "Rc Interconnect Synthesis-a Moment Fitting Approach", *Proc. IEEE/ACM Intl. Conf. Computer-Aided Design,* pp. 418-425, Nov. 1994.
- [8] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Computer-Aided Design*, vol. 9, pp.352-366, Apr. 1990.
- [9] C.L. Ratzlaff; L.T. Pillage, "RICE: rapid interconnect circuit evaluation using AWE", *IEEE Trans.Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, pp. 763-776, June 1994.
- [10] Semiconductor Industry Association, "International Technology Roadmap for Semiconductors 1999 Edition", 2000.
- [11] Semiconductor Industry Association, " International Technology Roadmap for Semiconductors 2000 Update", 2000.
- [12] G. Steele; D. Overhauser; S. Rochel; S. Z. Hussain, "Full-chip verification methods for DSM power distribution systems ", *Proc. of Design Automation Conference*, pp. 744-749, 1998.
- [13] Bogdan Tutuianu; Florentin Dartu; Lawrence T. Pileggi, "An Explicit RC-Circuit Delay Approximation Based on the First Three Moments of the Impulse Response ", *Proceedings of 33th Design Automation Conference*, June 1996.
- [14] Jiang Tao; Cheung, N.W.; Chenming Hu, "An electromigration failure model for interconnects under pulsed and bidirectional current stressing," *IEEE Trans. Electron Devices*, vol. 41, pp. 539-545, Apr. 1994.
- [15] Robert H. Tu; Elyse Rosenbaum; Wilson Y. Chan; Chester C. Li; Eric Minami; Khandker Quader; Ping K. Ko; Chenming Hu, "Berkeley reliability tools-BERT", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* Vol. 12, pp. 1523-1534 Oct. 1993.
- [16] Xiangdong Xuan; Abhijit Chatterjee, "Sensitivity and reliability evaluation for mixed-signal ICs under electromigration and hot-carrier effects" *Proc. IEEE Intl. Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 323-328, 2001.
- [17] D. Young, A. Christou, "Failure Mechanism Models for Electromigration", *IEEE Trans. on Reliability*, Vol. 43, no. 2, pp. 186-192, 1994.