A Statistical Gate Delay Model for Intra-chip and Inter-chip Variabilities

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Abstract— This paper proposes a model to calculate statistical gate-delay variation caused by intra-chip and inter-chip variabilities. Our model consists of a statistical transistor model and a gate-delay model. We present a modeling and extracting method of transistor characteristics for the intra-chip variability and the inter-chip variability. In the modeling of the intra-chip variability, it is important to consider a gate-size dependence by which the amount of intra-chip variation is affected. This effect is not captured in a statistical delay analysis reported so far. Our gate-delay model characterizes a statistical gate delay variation using a response surface method (RSM) according to the intra-chip and inter-chip variability of each transistor in a gate. We evaluate the accuracy of our model, and we show some simulated results of a circuit delay variation characterized by the measured variances of transistor currents.

I. Introduction

Device characteristics fluctuate much further in deep submicron technology. In a conventional worst-case timing analysis, the device characteristics are usually assumed to be uniform across a chip, but in fact, they are different [1, 2]. It is known that the intra-chip variability of the devices reduces a yield of products [2, 3, 4]. Some methods of the statistical timing analysis with the intra-chip variability are proposed [5, 6, 7]. However, a methodology is not shown to give an intra-chip variation of each gate from measured variances of transistors. The variation of each gate delay directly influences the variation of circuit delay. It is important to estimate each gate-delay variation accurately [1, 2]. At that time, it is necessary to consider the size dependence of the intra-chip variability [8, 9].

This paper proposes a model of statistical gate-delay calculation based on measured intra-chip and inter-chip variabilities. Figure 1 shows an overview of our method. The method consists of two components: a statistical modeling method of the inter-chip and intra-chip variabilities with the size dependence; and a calculating method of delay variation from the statistical models using a response surface method (RSM)[10].

At the statistical modeling of transistor characteristics, it is necessary to separate the intra-chip variability and the inter-chip variability. A conventional method extracts MOSFET model parameters from measured current characteristics. The intra-chip variation and the inter-chip variation of MOSFET parameters are then calculated from those extracted model parameters [8, 11, 12]. In this method, however, it is not easy to separate the variability into the intra-chip and inter-chip components. It could be advantageous to work on the variability

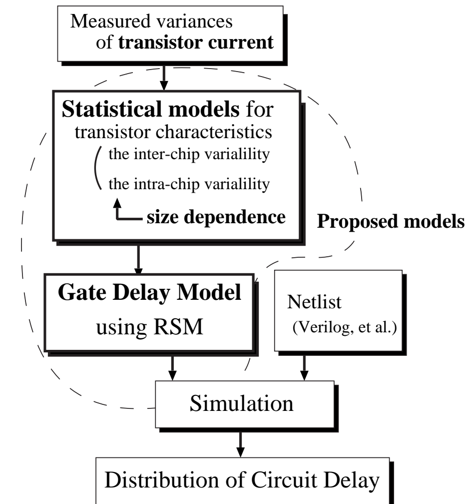

Fig. 1. The flowchart diagram of our proposed method.

of the current characteristics directly, which is the strategy we adopt in our statistical modeling.

For the reduction of computational cost, our method uses a response surface method (RSM)[10] to calculate a delay variation. A straightforward way of evaluating the intra-chip variability is to assign variables of the RSM to every transistor in the circuit, which is prohibitive. For further cost reduction, we propose a model that calculates the intra-chip variability of gate delay by a fewer variables.

This paper is organized as follows. Section II explains our statistical modeling method of transistor characteristics. We explain how to extract model parameters from variances of measured current, and show an experimental result. Section III shows a building method of RSM for the inter-chip variability, and proposes a calculating method of delay by the RSM with consideration of the intra-chip variability. Section IV demonstrates some experimental results, and presents the necessity to consider the size dependence from the results. Finally, section V concludes our discussion.

II. Modeling of variabilities

In this section, we show models for the inter-chip variability and the intra-chip variability, and present a procedure extracting each model parameter from current values.

The variabilities of transistor characteristics are classified into a local component and a global component according to

a kind of process non-uniformities. The local component is a variation caused by a stochastic nature, a white noise, of fabrication processes or a variation depending upon a layout [8, 9, 13, 14]. The global component represents a spatial parameter-value distribution over the whole wafer, which is caused by, for example, a non-uniform thermal distribution during a fabrication process [11, 12, 13, 14]. The components differ in a point of statistical behavior, so our method characterizes the components as an intra-chip variation and an inter-chip variation separately.

A. Modeling method of transistor characteristics

The transistor characteristics are mapped into physical parameters. You can choose any as the physical parameters. In this paper, we use V_{TH0}, T_{OX}, W_{int}, L_{int} as the physical parameters. The parameter V_{TH0} represents a threshold voltage of a large channel device. The parameter T_{OX} represents a gate-oxide thickness. The parameter W_{int} and L_{int} represent the differences, calculated electrically, of gate-width and gate-length from the original mask size respectively. The physical parameters should depend upon neither geometry nor bias voltages, so a threshold voltage V_{TH} (not V_{TH0}) is not suitable.

Physical parameters are represented as the sum of the mean value μ, an inter-chip variation g and an intra-chip variation r as follows.

$$p = \mu + g + r \tag{1}$$

The mean value μ is common to all. The inter-chip variation g is different in every chip but it is uniform in each chip, while the intra-chip variation r is different in the geometrical location in each chip. The inter-chip and intra-chip variations are expressed as a normal distribution, and the distributions of the variations are statistically independent. Both of the statistical models for the variations characterize variances of physical parameters and correlations among the parameters.

Several physical parameters determine electrical characteristics of a transistor practically. The influences of physical parameters are mingled with each other, so it is difficult to separate each physical parameter from the electrical characteristics. In our method, a *variance* of physical parameter is extracted from *current variance* directly based on the sensitivities of the physical parameters to the current value.

B. Models for the intra-chip and inter-chip variability

Pelgrom's model is most widely accepted to compute the local variability (mismatch) [8, 9, 11, 12]. The model characterizes the mismatch, the characteristic difference of two transistors, by the area of transistors and the distance between two transistors. We use following equations (2) ~ (5) as the model of the intra-chip variability, which is derived from Pelgrom's model.

$$\sigma^2(V_{TH0}) = \frac{A_{V_{TH0}}}{WL} \tag{2}$$

$$\sigma^2(T_{OX}) = \frac{A_{T_{OX}}}{WL} \tag{3}$$

$$\sigma^2(W_{int}) = \frac{A_{W_{int}}}{L} \tag{4}$$

$$\sigma^2(L_{int}) = \frac{A_{L_{int}}}{W} \tag{5}$$

The parameters $\sigma(V_{TH0})$, $\sigma(T_{OX})$, $\sigma(W_{int})$ and $\sigma(L_{int})$ are standard deviations of physical parameters V_{TH0}, T_{OX}, W_{int} and L_{int} respectively. The smaller the gate-size, the larger the standard deviation becomes. The parameters W and L are an effective gate-width and gate-length respectively. The model parameters $A_{V_{TH0}}$, $A_{T_{OX}}$, $A_{W_{int}}$ and $A_{L_{int}}$ are constants specific to a fabrication process.

The inter-chip variability cannot be expressed as a normal distribution in a strict sense [14], but this work characterizes the inter-chip variability as constant on a chip and normally distributed among chips in order to simplify statistical analysis. The inter-chip variability of transistor characteristics is expressed by the variances and covariances of the physical parameters.

C. Parameter extraction from variances of current

We explain a method to extract statistical model parameters for the intra-chip variability and the inter-chip variability from the variations of measured current values. Intra-chip and inter-chip components are separated on the current variations.

A variance of drain current is the sum of the inter-chip and intra-chip variances, so an intra-chip variance is the difference between the inter-chip variance and the total variance of current value. A typical value of drain current depends on the size of transistor, so we need many transistors of the same size in order to calculate an average and a variance of drain current.

We present a method that extracts the model parameters of intra-chip variability from the variations of measured current values. First, transistors are labeled on each chip. The current value of the i-th transistor on the j-th chip is I_{ij}. The current value I_{ij} is expressed by a MOSFET model function f with a row vector of physical parameters $\boldsymbol{p}_{ij}$ and a row vector of bias voltages $\boldsymbol{b}_{ij}$ as follows.

$$I_{ij} = f(\boldsymbol{p}_{ij}, \boldsymbol{b}_{ij}) \tag{6}$$

We use BSIM3v3 as the MOSFET model. The vector of the physical parameters $\boldsymbol{p}_{ij}$ is the sum of an inter-chip variation $\boldsymbol{g}_{ij}$, an intra-chip variation $\boldsymbol{r}_{ij}$ and an average vector $\boldsymbol{\mu}_i$.

$$\boldsymbol{p}_{ij} = \boldsymbol{\mu}_i + \boldsymbol{g}_{ij} + \boldsymbol{r}_{ij} \tag{7}$$

We assume that the intra-chip variance $\boldsymbol{r}_{ij}$ is sufficiently smaller than the average $\boldsymbol{\mu}_i$ empirically. The variance of current $\sigma^2(\Delta I_i)$ is represented as follows.

$$\begin{aligned} \sigma^2(\Delta I_i) &= \sum_n \left(\frac{\partial f_i}{\partial r_n}\right)^2 \sigma^2(r_{i,n}) \\ &+ \sum_n \sum_{m \neq n} \left(\frac{\partial f_i}{\partial r_n}\frac{\partial f_i}{\partial r_m}\right) \sigma(r_{i,n}|r_{i,m}) \end{aligned} \tag{8}$$

where $\frac{\partial f}{\partial \boldsymbol{r}}$ is a column vector, each element of which is a sensitivity of physical parameter to current value.

The n-th element of $\boldsymbol{r}_i$ is $r_{i,n}$. $\sigma^2(r_{i,n})$ is a variance of $r_{i,n}$. $\sigma(r_{i,n}|r_{i,m})$ is a covariance between $r_{i,n}$ and $r_{i,m}$. As the MOSFET model function f is known, the elements of $\frac{\partial f}{\partial \boldsymbol{r}}$ are differential functions of f by elements of $\boldsymbol{r}$ respectively.

TABLE I
SIZE (W/L) OF TRANSISTORS INCLUDED IN THE TEG.

ID	L (μm)	W (μm)	ID	L (μm)	W (μm)
1	0.10	0.36	6	0.3	10
2	0.10	0.6	7	1	10
3	0.10	10	8	10	0.3
4	0.13	10	9	10	0.4
5	0.18	10	10	10	0.6

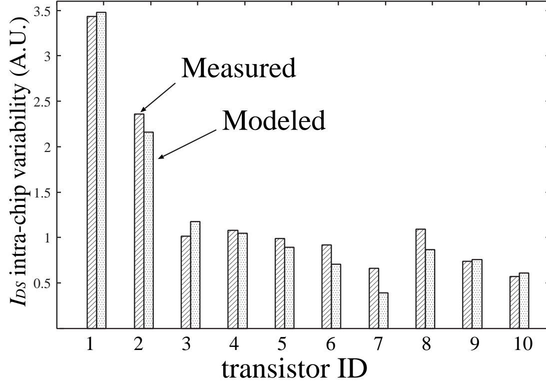

Fig. 2. Comparison of I_{DS} intra-chip variability between measured and modeled values. The boxes "Measured" shows the intra-chip components separated from the inter-chip components of current values. The boxes "Modeled" shows the values simulated by the modeled parameters.

In order to derive an equation for model parameters $\boldsymbol{A}_n$ and $\boldsymbol{A}_{nm}$, Eqs. (2) ~ (5) and models of correlations are substituted into Eq. (8). $\boldsymbol{A}_{nm}$ is a model parameter for correlation $\sigma(r_{i,n}|r_{i,m})$. The equation is solved using measured variances $\sigma^2(\Delta I_i)$, bias voltages $\boldsymbol{b}_{ij}$ and transistor sizes W_i and L_i, and the model parameters, $\boldsymbol{A}_n$ and $\boldsymbol{A}_{nm}$, are derived.

Model parameters of the inter-chip variability are variances and covariances of the physical parameters. Typical values of physical parameters on each chip are calculated from an average current value over the chip. The variances and covariances are calculated from the typical values of all chips.

D. Experimental results for the extraction

We report the result of parameter extraction for the intra-chip variability. The current values were measured from TEGs, which were fabricated using a 0.13 μm CMOS process. The TEG consists of 10 transistors, and TEGs were arranged on 56 chips over the whole wafer. Table I shows the sizes of the transistors. Inter-chip components and intra-chip components of current variation were separated from the measurements. The model parameters $\boldsymbol{A}_n$ and $\boldsymbol{A}_{nm}$, for the parameters V_{TH0}, T_{OX}, W_{int} and L_{int}, are calculated using Eq. (8) from the intra-chip components of drain current variation when the drain voltage is 0.1 (V) and the gate voltages are 0.6, 0.7, 0.8, 0.9 and 1.0 (V).

Figure 2 shows the variation of measured and modeled current values. The horizontal axis represents the ID number of transistors in Table I. The vertical axis represents the I_{DS} variability (standard deviation in an arbitrary unit). The drain voltage was 0.1 (V), and the gate voltage was 1.0 (V). In the figure, the boxes "Measured" shows the intra-chip components separated from the inter-chip components of current values. The boxes "Modeled" shows the values simulated by the modeled parameters. The average error is 12% of measured value.

III. STATISTICAL GATE-DELAY MODELING

In this section, we explain a gate-delay model to characterize an inter-chip and intra-chip delay variation using a response surface method (RSM)[10].

In order to calculate not only the inter-chip delay variation but also the intra-chip delay variation, it is necessary to consider a variation among transistors in a gate. The transistors fluctuate each other in each gate. If we assign variables of RSM to each transistor, many variables would be needed. For example, if we assigned 4 variables to each transistor, a 4-input 4-folded NAND gate would need 64 variables. The increase of variables is not good, because it requires more time to generate RSMs and calculate delay. Then, we propose a method to calculate the intra-chip variation of delay using an RSM generated for the inter-chip variability in order to reduce the variables of RSM.

A. RSM using lookup tables

First, we explain how to generate a response surface model (RSM) using lookup tables for the inter-chip variability. The physical parameters are expressed as a vector $\boldsymbol{p} = (p_1, p_2, \ldots, p_n)^T$. A delay time t_{d} is calculated by a linear RSM as follows.

$$\begin{aligned} t_{\mathrm{d}} &= \mathrm{rsm}(\boldsymbol{p}) \\ &= b_0 + \boldsymbol{b}^T \boldsymbol{p} \end{aligned} \tag{9}$$

The delay time is influenced by not only transistor characteristics but also a transition time and a load capacitance. Coefficients of RSM also depend on the transition time and the load capacitance. It is difficult to build the accurate RSM that has transition and capacitance as a parameter for a wide range.

Then, we use a table-lookup RSM, a coefficient of which is calculated from a table of transition and capacitance. In each element of table, coefficients of RSM are derived from several SPICE simulations using a least square method. A set of coefficients is simulated for each transition and each capacitance, which form a 2-dimensional table. The table-lookup RSM is built for each gate and each rise and fall time.

B. Reproduction of physical parameters and Delay calculation

Here, we discuss a delay calculation using RSM about a gate which has one nMOS and one pMOS such as an inverter gate. The physical parameters are represented by the sum of inter-chip variation $\boldsymbol{p}_{\mathrm{g}}$ and intra-chip variation $\boldsymbol{p}_{\mathrm{r}}$. The vectors $\boldsymbol{p}_{\mathrm{g}}$ are common among transistors in each chip. The vectors $\boldsymbol{p}_{\mathrm{r}}$ of every transistor are different.

The physical parameters generally have correlation each other. The correlative parameters $\boldsymbol{p}$ are derived from non-correlated variables $\boldsymbol{x}$ using the Principal Component Analysis (PCA) as follows [15].

$$\boldsymbol{p} = \boldsymbol{D}\boldsymbol{U}\boldsymbol{\Lambda}^{1/2}\boldsymbol{x} \tag{10}$$

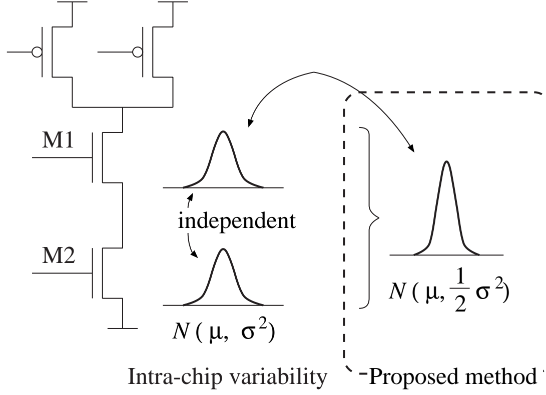

Fig. 3. Delay variations of 2-input NAND gate.

where $\boldsymbol{U}$ is a matrix whose column vectors consist of eigenvectors of a correlation matrix of $\boldsymbol{p}$, and $\boldsymbol{\Lambda}$ is a matrix which has eigenvalues of the correlation matrix in diagonal. $\boldsymbol{D}$ is a matrix whose diagonal elements are standard deviations of the physical parameters. Each element of vector $\boldsymbol{x}$ is a random number with a normal distribution whose mean value and variance are 0 and 1 respectively.

Considering the inter-chip variation and the intra-chip variation, a delay t_{d} is modeled as follows.

$$
\begin{aligned}
t_{\mathrm{d}} &= b_0 + \boldsymbol{b}^T \boldsymbol{p} \\
&= b_0 + \boldsymbol{b}^T (\boldsymbol{\mu} + \boldsymbol{p}_{\mathrm{g}} + \boldsymbol{p}_{\mathrm{r}}) \\
&= t_0 + \boldsymbol{\tau}_{\mathrm{g}}^T \boldsymbol{x}_{\mathrm{g}} + \tau_{\mathrm{r}} x_{\mathrm{r}} \qquad (11)
\end{aligned}
$$

$$
\begin{aligned}
\boldsymbol{\tau}_{\mathrm{g}} &= \boldsymbol{b}^T \boldsymbol{D}_{\mathrm{g}} \boldsymbol{U}_{\mathrm{g}} \boldsymbol{\Lambda}_{\mathrm{g}}^{1/2} \qquad (12) \\
\tau_{\mathrm{r}} &= \sigma(\boldsymbol{b}^T \boldsymbol{p}_{\mathrm{r}}) \qquad (13)
\end{aligned}
$$

The terms $\boldsymbol{\tau}_{\mathrm{g}}^T \boldsymbol{x}_{\mathrm{g}}$ and $\tau_{\mathrm{r}} x_{\mathrm{r}}$ represent the inter-chip delay variation and the intra-chip delay variation respectively. Each element of vector $\boldsymbol{x}_{\mathrm{g}}$ is a standard normal-distributed variable. A scalar number x_{r} is a standard normal-distributed variable. The subscripts g and r represent the inter-chip variability and the inter-chip variability respectively. The matrices $\boldsymbol{D}_{\mathrm{g}}$, $\boldsymbol{U}_{\mathrm{g}}$ and $\boldsymbol{\Lambda}_{\mathrm{g}}$ are calculated using the inter-chip model.

C. Application to complex gates

In section III.B, we described the model for the calculation of the delay variation in the case that the number of transistors on a charging/discharging path is one such as an INV gate. In this section, we explain how to extend this model in such a case where multiple transistors exist on a charging/discharging path.

When multiple transistors exist on a charging/discharging path, each transistor affects the transient behavior of the gate. There are two cases in the connection of the transistors: serial connection and parallel connection. An example of the former is a pull-down path of NAND gate, and an example of the latter is a multiple-folded transistor. Generally, Eq. (11) can be written as follows.

$$
\begin{aligned}
t_{\mathrm{d}} &= b_0 + \boldsymbol{b}_1^T \boldsymbol{p}_1 + \boldsymbol{b}_2^T \boldsymbol{p}_2 + \boldsymbol{b}_3^T \boldsymbol{p}_3 + \ldots + \boldsymbol{b}_m^T \boldsymbol{p}_m \qquad (14) \\
&= b_0 + \sum_k^m \boldsymbol{b}_k^T \boldsymbol{\mu} + \sum_k^m \boldsymbol{b}_k^T \boldsymbol{p}_{\mathrm{g}} + \sum_k^m \boldsymbol{b}_k^T \boldsymbol{p}_{\mathrm{r}k} \qquad (15) \\
&= t_0 + \boldsymbol{\tau}_{\mathrm{g}}^T \boldsymbol{x}_{\mathrm{g}} + \sum_k^m \tau_{\mathrm{r}k} x_{\mathrm{r}k} \qquad (16)
\end{aligned}
$$

where m is the number of the transistors on the charging/discharging path. Terms $\boldsymbol{b}_k^T \boldsymbol{p}_k$ are assigned to each transistor. The vectors $\boldsymbol{x}_{\mathrm{g}}$ are common among transistors in each chip. The scalars $x_{\mathrm{r}k}$ of every transistor are different. The variables $\boldsymbol{x}_{\mathrm{g}}$ and $x_{\mathrm{r}k}$ do not have correlation with each other.

Here we explain how to calculate the standard deviation of intra-chip delay variability using a 2-input NAND gate of Figure 3 as an example. We assume that intra-chip variations and sensitivities to a delay time of each transistor (M1 and M2) are equal. In Figure 3, a delay variance of each transistor is represented as σ^2. A total delay variance is $\frac{1}{2}\sigma^2$ when characteristics of the transistors M1 and M2 fluctuate independently.

It is difficult to derive every variables $\tau_{\mathrm{r}k}$ of Eq. (16) from the RSM $\boldsymbol{b}$ directly, so we introduce a sensitivity constant s_k.

$$
\begin{aligned}
\tau_{\mathrm{r}k} &= s_k \tau_{\mathrm{r}0} \qquad (17) \\
\tau_{\mathrm{r}} &= \sigma(\boldsymbol{b}^T \boldsymbol{p}_{\mathrm{r}}) \qquad (18) \\
&= \sigma\left(\sum_k^m \tau_{\mathrm{r}k} x_{\mathrm{r}}\right) \qquad (19) \\
&= \sum_k^m s_k \tau_{\mathrm{r}0} \qquad (20)
\end{aligned}
$$

where $\tau_{\mathrm{r}0}$ is a reference value. Each intra-chip variation $x_{\mathrm{r}k}$ is independent, and our proposed model can be derived from Eq. (11) as follows.

$$
\begin{aligned}
t_{\mathrm{d}} &= t_0 + \boldsymbol{\tau}_{\mathrm{g}}^T \boldsymbol{x}_{\mathrm{g}} + \sqrt{\sum_k^m s_k^2}\ \tau_{r0} x_{\mathrm{r}} \qquad (21) \\
&= t_0 + \boldsymbol{\tau}_{\mathrm{g}}^T \boldsymbol{x}_{\mathrm{g}} + \frac{\sqrt{\sum_k^m s_k^2}}{\sum_k^m s_k} \tau_{\mathrm{r}} x_{\mathrm{r}} \qquad (22)
\end{aligned}
$$

We can calculate the sensitivity constants s_k using a few sensitivity analysis. If the sensitivity constants are equal to each other on a charging/discharging path, the intra-chip variation factor is simplified as follows.

$$
\frac{\sqrt{\sum_k^m s_k^2}}{\sum_k^m s_k} = \frac{\sqrt{ms^2}}{ms} = \frac{1}{\sqrt{m}} \qquad (23)
$$

A transistor with large width is often folded. Each divided transistor has less channel area and hence fluctuates more than the original transistor. In this case, we can also use Eq. (22) to calculate a delay time.

D. Accuracy evaluation for the reduction of variables

In this section, we evaluate an accuracy of our method. We compare the delay variation simulated by a Monte Carlo analysis using SPICE and the delay variation calculated by our

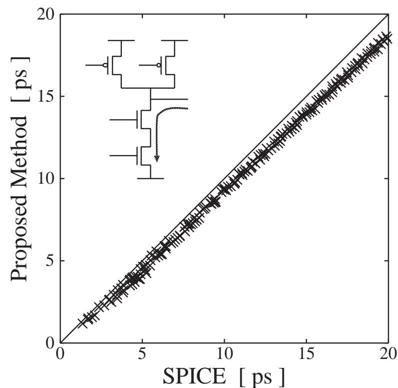

Fig. 4. Comparison between simulated (SPICE) and modeled (Proposed method) deviations of delay (2-input NAND gate).

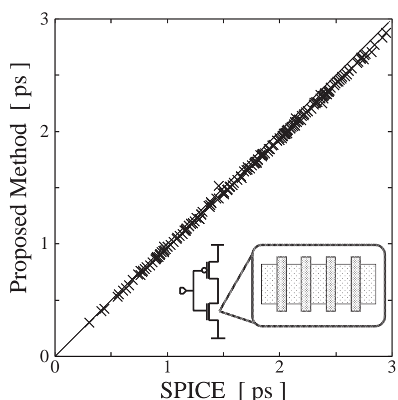

Fig. 5. Comparison between simulated (SPICE) and modeled (Proposed method) deviations of delay (folded INV gate).

model for 2-input NAND gate and 4-folded INV gate. We assume that each sensitivity constant s_k is 1.

We use a cell library and MOSFET model parameters for a 0.13 μm CMOS process. The physical parameters are fluctuated according to our model whose parameters are extracted from measured current values. The range of load capacitance is 2fF to 100fF, and the range of input transition time is 10ps to 100ps. Figure 4 and Figure 5 show the standard deviations of delay for 2-input NAND gate and 4-folded INV gate respectively. The horizontal axis represents the standard deviation of delay variation simulated by SPICE. The vertical axis represents the standard deviation of delay variation calculated by our method. The average error of 2-input NAND gates is 8.6% in Figure 4. The average error of 4-folded INV gates in Figure 5 is 3.1%.

IV. Experimental results

In Sections II and III, we evaluate the accuracy on the statistical modeling of transistor current and the calculation of the intra-chip delay variation using an RSM generated for the inter-chip variability. In this section, we show experimental results for the evaluation of the size dependence using our method. We present an importance of the size dependence in an intra-chip delay analysis.

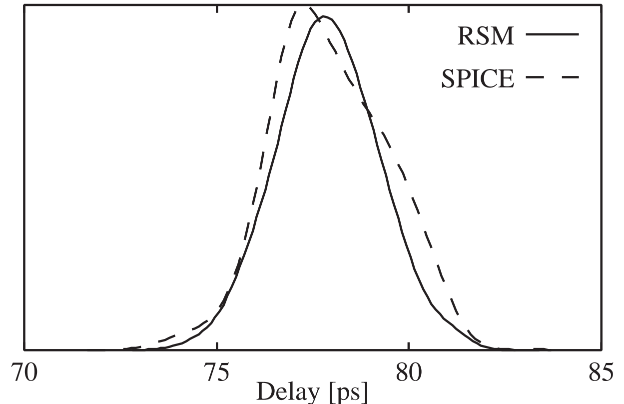

Fig. 6. Comparison of delay distribution between RSM and SPICE (a 5-stage inverter chain).

A. Accuracy of RSM-based statistical delay analysis

We show a comparison between circuit delay calculated by RSM and SPICE. Figure 6 shows experimental results for a 5-stage inverter chain. The physical parameters V_{TH0}, T_{OX}, W_{int} and L_{int} are fluctuated according to the models extracted using measured current values. The broken line represents a distribution of circuit delay simulated by SPICE. The solid line represents a distribution of circuit delay calculated by our method. The difference of the mean values is 0.116 [ps]. The difference of the worst cases is 0.175 [ps].

B. Experimental results for the size dependence

We report experimental results for the size dependence. For comparison, we simulated circuit delays under two models of transistor characteristics: a proposed model is derived from measurements using our method and considers the size dependence while a conventional model treats the intra-chip variance such that the variance is equal to all transistors with different size [5].

Figure 7 shows the delay variances of an INV8 gate and an INV0.5 gate. The INV8 gate is constructed from transistors with the width being 16 times as large as that of INV0.5 gate. As the conventional model does not characterize the size dependence, delay variances do not depend upon the size of transistors. The ratio of intra-chip delay variances simulated by the proposed model depends upon the size of transistors.

Figure 8 shows distributions of circuit delays simulated by the conventional model and our model. The simulated circuit (des) consists of 3759 logic gates, which is a combinational circuit included in LGSynth93 benchmark set. The broken line represents the distribution of circuit delay simulated by the conventional model. The solid line represents the distribution of circuit delay calculated by our model. The error of the mean values is 0.0386 [ns]. The error of the worst-case values ($\mu + 3\sigma$) is 0.177 [ns], which is 26.1% of the mean value. Execution time of 1000-times Monte Carlo analysis was 15.8 seconds on a Pentium4 1.7GHz running Linux.

Although the effect of intra-chip variation becomes small for a circuit with larger logic depth, we can see noticeable difference in the worst-case delay in our benchmark circuit. It

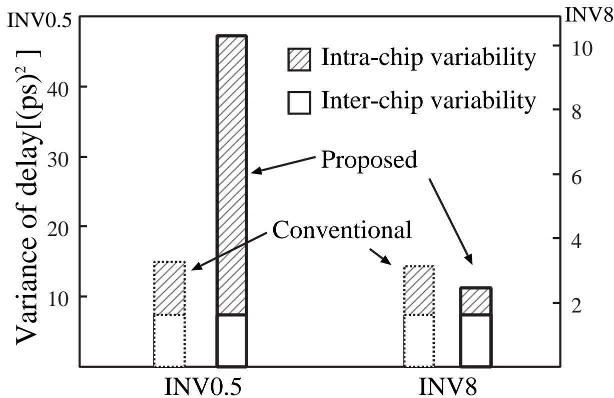

Fig. 7. Comparison between delay variances by proposed and conventional models.

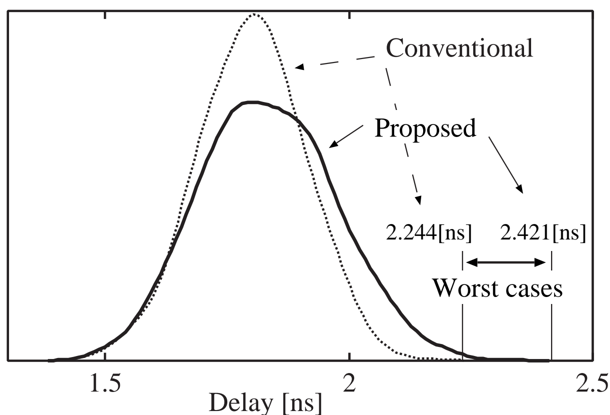

Fig. 8. Comparison of delay distribution between proposed and conventional models (des circuit).

is important to consider the size dependence of the intra-chip variability.

V. Conclusion

This paper propose models of statistical gate-delay calculation based on measured intra-chip and inter-chip variabilities.

We show a method that characterizes the intra-chip variability and the inter-chip variability separately and calculates the model parameters directly from the variances of current value for accuracy improvement. The average error of the extraction is 12%.

We use a response surface method (RSM) to calculate delay from transistor characteristics. In order to reduce computing cost, we propose a method to calculate the intra-chip variation of delay by the RSM which has a fewer parameters generated for the inter-chip variability. The simulation on our test case shows that the error is 8.6% in the case of cascaded transistors and the error is 3.1% in the case of folded transistors.

The intra-chip variation of gate delay depends upon its transistor sizes. Our method considers the size dependence of transistor characteristics in the calculation of delay variation. We show the results of our simulation that the difference between the delay variation calculated with and without the size dependence is 26.1% in our example, which indicates the importance of the size dependence in the modeling of the intra-chip variation.

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