# Physical Design with Multiple On-Chip Voltages

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## EXTENDED ABSTRACT

Supply voltage is one of the dominant factors that determine the timing performance and power consumption of VLSI chips. For digital systems with a single supply voltage, some logic devices typically operate faster or more frequently than necessary, consuming extra power. This motivates the need for multiple-voltage design for an aggressive power optimization as slow operation allows a reduced voltage level. While the past few years have seen some successful examples from behavioral- and logic-level synthesis, physical designers are facing the challenges under such a new design environment. This talk discusses the physical aspects of multiple-voltage design, including the latest approaches to emerging problems such as voltage interface, clock distribution, power/ground network, and place-and-route (for more info, visit the web site at: *http://www.vlsi.uwindsor.ca/~cchen*). The goal is to enable designers to deal with key issues in implementation of multiple-voltage chips.

We first introduce the concept of hierarchy with multiple voltages which can be applied to various design levels. In general, the voltages could be either dynamically or statically variable. The dynamic-voltage scheme requires high-efficiency DC-DC converters and a voltage scheduling mechanism which treats the voltage as a function of workload and timing constraints. The static-voltage strategy calls for considerations about the number of different voltages and the selection of their values. We discuss these issues with emphasis on dual-voltage solutions which are a typical case.

We then study the interface between different voltages on a same chip. At high levels of abstraction, the chip needs to be partitioned into several regions so that each individual region uses the same supply voltage. This can be done with careful floorplanning and power/ground network design. At low levels of abstraction, the interface design involves investigating specific layout structures. Particularly, we discuss level converters which are inserted between different voltages to prevent the static current. Techniques to minimize the effect of level converters are also explored.

Since clock distribution network is a power-hungry component on today's chips, applying multiple voltages to it can save significant power. The basic idea is to use a lower voltage swing through the clock tree, and the clock signal can be converted to a higher voltage at the sinks. Buffers in the clock tree and/or flip-flops at the sinks can be combined with level converters to reduce their delay and power overheads.

We also look at the power/ground network which is another concern with multiple on-chip voltages. Designers can simply distribute different power lines to everywhere by using standard cells with more than one power rails. Alternatively, different power supplies can be separately delivered to individual regions, depending upon the layout structures. We will compare these approaches, and analyze their effect on place-and-route. In addition, a new "fabric" layout for P/G and signal nets will be reviewed towards tackling the cross-coupling and signal integrity which are exacerbated for signal nets with different voltages.

Multiple-voltage brings additional physical constraints into both placement and routing, resulting in a more difficult layout design for signal nets. To improve routing, new placer and router should be able to assign highly-connected logic devices to the same voltage, and to locate signals with same voltage in the neighboring areas. Recent methodology from the literature will be described. Furthermore, shielding techniques can be used locally to minimize the capacitive crosstalk between signal nets.

Finally, we will present the future trends for multiple-voltage design, together with tool aspects from an industrial perspective.

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