Physical Insight Into Fractional Power Dependence of Saturation Current on Gate Voltage in Advanced Short Channel MOSFETS (Alpha-Power Law Model)

Hyunsik Im [1,2], M. Song [2], T. Hiramoto [1,3], and T. Sakurai [1,4]
[1] Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-Ku, Tokyo 153-8505, Japan
[2] Department of Semiconductor Science, Dongguk University, 3-26 Phil-Dong, Joong-Gu, Seoul 100-715, Korea
[3] VLSI Design and education Center, and [4] Center for Collaborative Research, University of Tokyo
(+82) 2 2260 3740 and (+81) 3 5452 6264
Hyunsik7@dongguk.edu

ABSTRACT
The physical origin of the fractional power dependence of MOSFET drain current on gate voltage, namely α-power law model that has been considered as a fully empirical model, is analytically investigated. For this purpose, we have developed a new physics-based analytical drain current model. Using this model, we prove that the saturation current can be simplified in the form of $B\cdot(V_g-V_{TH})^{\alpha}$, α-power law model. The physical interpretations on α, B, V_{TH} are elucidated, and their analytical expressions are given in terms of MOSFET's parameters. Since the α-power model is compact and physics-based, it allows circuit designers to easily estimate the power dissipation and the gate delay time in a predictable manner.

Categories & Subject Descriptors: I.6.5 Model Development.

General Term: Theory, Verification.

Keywords: MOSFET modeling, Saturation current, α-power model.

1. INTRODUCTION
Since Shockley's square model is not inadequate for today's MOSFETs due to various effects of velocity saturation, short channel effect, mobility degradation, and series resistance, new MOSFET's models have been developed to replace it [1][2][3]. The general strategy for the MOSFET's model development can be categorized into two ways as follows:

1. A *compact* (but empirical) model of the drain current (I_{ds}) in advanced short channel MOSFETs is very important in VLSI initial designs (*ie* quick estimation of power and speed performance).

2. In parallel, it is also strongly required to develop a *physics-based analytical* drain current model for the sake of better physical insights into the fundamentals of future ultra-short MOSFETs characteristics.

Most of drain current models reported are reasonably accurate, but their mathematical expressions are complicated to use. On the other hand, the conventional α–power law model [3] is widely used in discussing low power/low-voltage circuits, but since it is totally empirical we cannot know the applicability of the α–power model for future devices, including SOI transistors and dual-gate MOSFETs. In addition, the physical background of its main parameters, α, B, and V_{TH} has not been satisfactorily understood yet, leading to some uncertainty in the evaluation of circuit performance. It is empirically known that the value of α of present advanced MOSFETs is around 1.3. In this study, we develop an analytical drain current model for advanced short channel MOSFETs, and then demonstrate that its saturation current equation can be switched into the α–power law model revealing the physical origins of α, B, and V_{TH}. The α–power model is also successfully verified by comparing with experimentally measured bulk and SOI MOSFETs data. It is thus shown for the first time from the analytical and experimental approaches that the α-power model is not just an empirical model, but it is a general model applicable to various MOSFETs including SOI, SiGe and dual-gate structures.

2. MODEL
The objective in the development of this model is to analytically investigate the effect of velocity saturation on the drain current characteristics of advanced short channel MOSFETs, taking into account series resistance.

2.1 New velocity-field model for short channel MOSFETs
Due to the different dependence of the carrier drift velocity, $v(E)$, on the longitudinal channel field E, the electrical characteristics of

ISLPED'02, August 12-14, 2002, Monterey, California, USA.

the short channel MOSFETs differs from those of the long channel MOSFETs. Therefore, the determination of $v(E)$ is crucial to the accuracy of the short channel MOSFET model. In this work, an improved empirical velocity-field expression depicted in (1) is proposed to analytically drive the drain current equation of the short channel MOSFETs:

$$v(E) = \frac{v_0 \cdot a \cdot (E/E_c)}{[b + c \cdot (E/E_c)^n]^{1/n}}, \quad E_c = v_0 / \mu_{eff} \qquad (1)$$

where v_0 is a constant whose dimension is velocity [m/s], and μ_{eff} is the effective mobility dependent on the gate voltage [4]. It is generally accepted that n = 2 with a, b, c = 1 for electrons, and n = 1 with a, b, c = 1 for holes. The saturation velocity, v_{sat}, is equal to v_0. However, the mathematics in solving the n = 2 case to derive the drain current are very delicate and tedious [5]. For that reason, by additionally introducing the new parameters (a, b, and c) instead for the n = 1 case, we are able to reasonably well reproduce the n=2 electron velocity *vs*. longitudinal field characteristics, consequently leading to the derivation of the drain current. Here, v_{sat}, corresponds to $v_0 \times a/c$. In the low field limit, $v(E) \rightarrow \mu_{eff} \cdot E$, whilst in the high field limit, which is of greatest interest in the present deep sub-micron technology node, $v(E) \rightarrow v_{sat}$. This is only an empirical part in this work and the other parts are fully analytical. For the values of a, c, and n used for this work, refer to table I. For simplicity, b is set to be 1.

Table 1. Parameters used for present velocity–field model

For simplicity, *b*=1.

	n	*a*	*c*
Si-NMOSFET	1	1.431	1.089
Si-PMOSFET	1	1	1

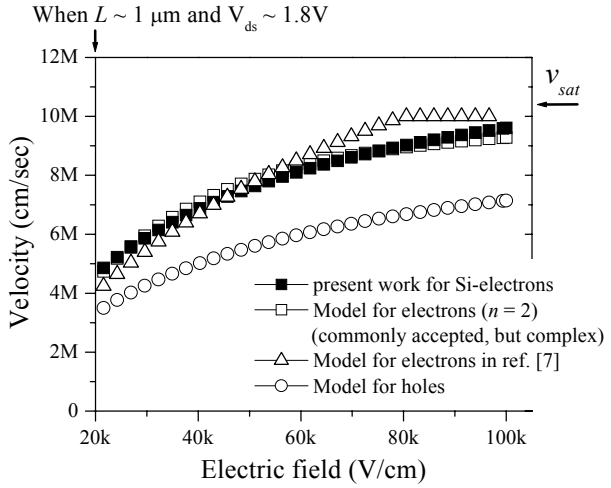

Fig 1. Comparisons of commonly used electron velocity-field models with the model in (1). Present model for holes is the same with a commonly used hole velocity saturation model.

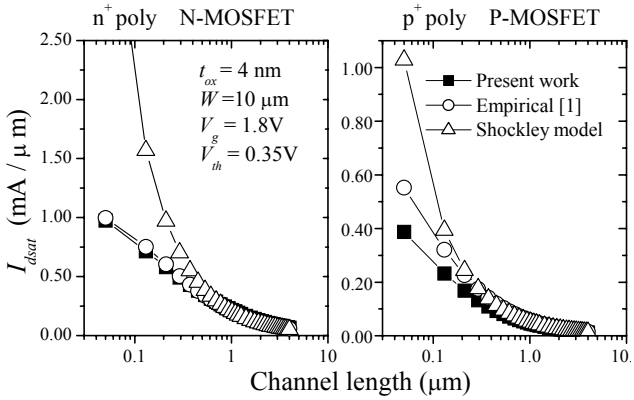

Fig 2. The new analytical I_{dsat} model is in excellent agreement with an already- verified empirical model [1] for MOSFETs with various channel lengths.

Furthermore, notice that adjusting the values of *a, b*, and *c* the model can be also applicable to SiGe, III–V and SOI MOSFETs.

Fig 1 shows the comparisons of the present velocity-field model with the commonly used velocity-field models [6][7]. Our present model is in good agreement with the more complicated model with n = 2 which fits experimental data quite well but *cannot lead* to an analytical solution of I_{ds} due to its complex mathematical form. Overall relative error between our present model and the commonly accepted model (n = 2) has been found to be less than 3%.

2.2 Analytical drain current model for short channel MOSFETs

To obtain the drain current model one must solve the following equation:

$$I_{ds}(x) = -\mu_{eff} W \frac{dV}{dx} Q_i(V) \qquad (2)$$

where W is the channel width, V is the quasi-Fermi potential at a point x in the channel, and $Q_i(V)$ is the total inversion charge density at the point. The charge sheet model and carrier drift velocity formula depicted in (1) yield an analytical drain current equation:

$$I_{ds}(V_g) = a\mu_{eff} C_{ox} \frac{W}{L} \frac{V_G \cdot V_{ds} - m/2 \cdot V_{ds}^2}{1 + c \cdot m \cdot V_{ds}/2\beta} \qquad (3)$$

where $\beta = \frac{m \cdot v_0 \cdot L}{2 \cdot \mu_{eff}}$, $m \cong 1 + 3t_{ox}/W_{dm}$, $V_G \equiv V_g - V_{th}$ and W_{dm} represents the maximum depletion width. Its saturation voltage (V_{sat}) and current (I_{dsat}) can be found by solving $dI_{ds}/dV_{ds} = 0$:

$$V_{sat} = \frac{2\beta}{c \cdot m}\left(\sqrt{1+\frac{c}{\beta}V_G} - 1\right)$$
$$I_{dsat} = (a/c^2)\cdot C_{ox}\cdot W \cdot v_0 \cdot \beta \cdot \left(\sqrt{1+c\cdot V_G/\beta} - 1\right)^2 \quad (4)$$

It can be shown that when $(V_g - V_{th}) << \beta$, I_{dsat} reduces to the long channel saturation current, $\propto (V_g - V_{th})^2$ (i.e. α=2), and in the limit of β(or L)$\rightarrow$0, to the velocity-saturation limited current, $\propto (V_g - V_{th})^1$ (i.e. α=1). The following equation in (5) represents I_{dsat} taking into account the effect of the series resistance (R_s) of the source end, which can be calculated iteratively or by solving a second-order function of I_{dsat}:

$$I_{dsat} = (a/c^2)\cdot C_{ox}\cdot W \cdot v_0 \cdot \beta \cdot \left(\sqrt{1+c\cdot (V_G - I_{dsat}\cdot R_S)/\beta} - 1\right)^2 \quad (5)$$

3. MODEL VERIFICATION

Present analytical I_{dsat} model is compared with a widely used validated empirical model [1] and with the classical Shockley' square model, as seen in table II and in Fig 2. In the Shockley' model, α is always 2 irrespective of gate length, because the velocity saturation effect is neglected. In most of empirical models, the velocity saturation effect is incorporated in the Shockley's model in an empirical manner. Excellent agreement between the present model and the validated empirical model is achieved. For the further verification of our model, Fig 3 shows the comparisons of the measured I_{dsat} in the 0.2μm technology node Bulk MOSFETs (see Fig 4 for the I_{ds}–V_g characteristics) to the modeled I_{dsat} using (5). For these comparisons, the value of R_s is experimentally extracted using the channel resistance method [8]. The measured total resistance, R_{tot} (V_{ds}/I_{ds} at small V_{ds}) *vs*. channel length (L) yields a straight line. Its intercept at L = 0 is taken as the total source-drain parasitic resistance, R_{sd} (=2×R_s). It is assumed that effective channel length (L_{eff}) is the same with the mask length (L_{mask}). Good agreement between the measured and analytically calculated I_{dsat} is also achieved in the entire range of channel length. However, notice that for the p-MOSFET data shown in Fig. 2 and Fig. 3, our analytically modeled data seem to get smaller with decreasing channel length than the data obtained from the experimental measurements and the empirical model. We thus suspect that the generally accepted values of *a*, *b*, and *c* for holes in table I should be adjusted.

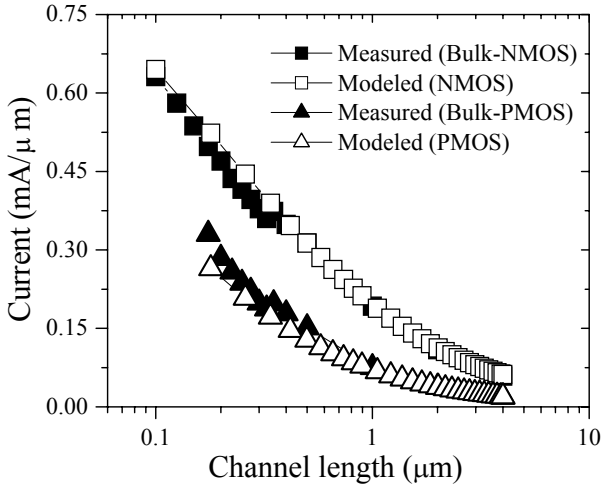

Fig 3. Comparisons between the measured and modeled I_{dsat} using (5). R_s = 15Ω for NMOSFET and 8Ω for PMOSFET. No fitting procedure is performed for the comparisons. V_g = 1.8V and V_{ds} = 1.8V.

4. THE PHYSICAL NATURE OF THE α–POWER LAW MODEL

In the ISLPED held in 2001, we successfully modeled the active power consumption of the variable threshold voltage CMOS (VTCMOS), using the empirical α–power law model [9]. However, since the physical origin of its main parameters, α, B and V_{TH} , were not fully understood, some uncertainty in the power estimation of the device remained. In this section, the α–power law model is analytically discussed in terms of the drain current model explained in the previous sections.

First, examples of the measured I_{dsat}-V_g characteristics taken from both *bulk* and *SOI* MOSFETs, and their $\log_{10}(I_{dsat})$ *vs*. $\log_{10}(V_g - V_{TH})$ plots are illustrated in Fig 4. The excellent linearity of the logarithm plots confirms the validity of $I_{dsat} = B\cdot(V_g - V_{TH})^{\alpha}$. The slopes of the logarithm plots and values of $\log_{10}(I_{dsat})$ at $\log_{10}(V_g - V_{TH}) = 0$ correspond to the values of α and

Table II. Two I_{dsat} models compared to the analytical model presented here.

	Classical Shockley's square model	Chen *et al* [1] [Widely used empirical model]	Present model in (3) and (4)
$I_{ds}(V_g)$:	$\mu_{eff} Cox \frac{W}{L}[(V_g - V_{th})\cdot V_{ds} - m/2\cdot V_{ds}^2]$	Not Available	$a\mu_{eff} C_{ox}\frac{W}{L}\frac{V_G\cdot V_{ds} - m/2\cdot V_{ds}^2}{1+c\cdot m\cdot V_{ds}/2\beta}$
I_{dsat} :	$\mu_{eff} Cox \frac{W}{L}\frac{(V_g - V_{th})^2}{2m}$	$Wv_{sat}C_{ox}\frac{(V_g - V_{th})^2}{V_g - V_{th} + 2Lv_{sat}/\mu_{eff}}$	$(a/c^2)C_{ox}W\cdot v_0\cdot\beta(\sqrt{1+c\cdot V_G/\beta} - 1)^2$

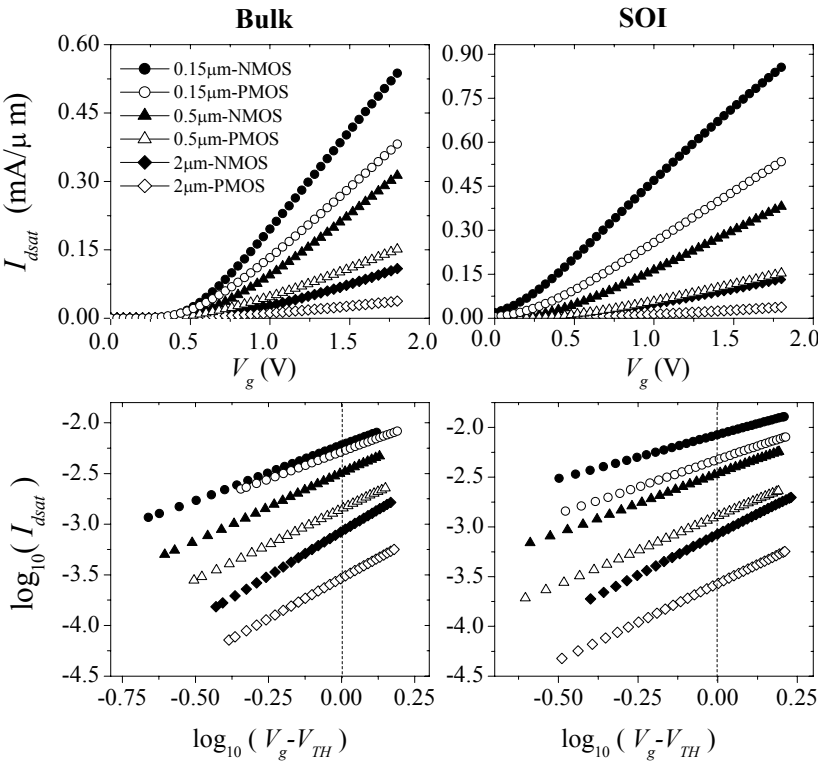

Fig 4. Examples of the measured $I_{dsat} - V_g$ characteristics for the 0.2μm technology node *bulk* and *SOI* MOSFETs and their logarithm plots. V_{ds} = 1.8V and W =15μm.

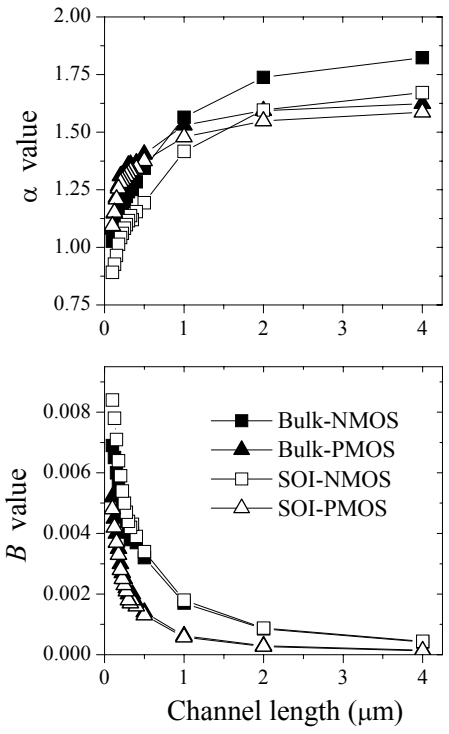

Fig 5. Extracted values of α and *B* from the measured data in Fig 4, as a function of channel length.

B respectively, and they are plotted in Fig 5, as a function of channel length. As *L* decreases, the values of α and *B* decrease and increase, respectively. However, in the Shockley's and most of empirical models presented elsewhere, they can qualitatively explain the increase of *B* but cannot do the decrease of α.

To investigate how α and *B* are affected by R_s, *L*, and substrate doping concentration (N_a and N_d), α and *B* are modeled by analytically solving (4) and (5), as seen in Fig 6. It is obvious that larger R_s makes α and *B* smaller, consequently leading to decreasing I_{dsat}. The gate length dependences of the modeled α and *B* are in good agreement with the measured data in Fig. 5. Note that the analytical threshold voltage (V_{th}) and α-power threshold voltage (V_{TH}) extracted from the analytically modeled I_{dsat} are different. V_{TH} is iteratively calculated until the percent error (as shown in Fig 7) becomes less than 2% in the entire range of V_g. It is found from this calculation that V_{TH} can be approximated as the linearly extrapolated threshold voltage, V_{on}, which is typically higher than V_{th} by (2~4)kT/e [10]. When R_s=0, analytical expressions of α and *B* are as follows:

$$\alpha(\beta) = log_{10}[\beta_2 \cdot (\sqrt{1 + c \cdot (0.1 + \Delta V_{th})/\beta_2} - 1)^2] - log_{10}[\beta_1 \cdot (\sqrt{1 + c \cdot (1 + \Delta V_{th})/\beta_1} - 1)^2] \quad (6)$$

and

$$B \cong (a/c^2) \cdot C_{ox} \cdot W \cdot v_0 \cdot \beta_1 \cdot (\sqrt{1 + c/\beta_1} - 1)^2 \quad (7)$$

where β_1 and β_2 are the values of β at $V_g - V_{TH}$ = 1 and 0.1 respectively and $\Delta V_{th} = V_{TH} - V_{th}$. It is obvious from these equations that the values of α and *B* are mainly determined by the value of β (= $m \cdot v_0 \cdot L/(2\mu_{eff})$). The physical implication of 2β is the effective drain voltage roughly corresponding to the velocity saturation. Thus, it is clearly understandable that if $\beta \to 0$ (equivalently, $L \to 0$), the current saturation at a given gate voltage (V_g) occurs at a lower drain voltage (V_{ds}) compared with the long channel case when $\beta >> 0$. This is well consistent with experimental observations.

Since β is a function of the channel length (*L*) determining the lateral electric field, effective mobility (μ_{eff}) controlling the degree of the velocity saturation, and structural parameter ($m = 1+3t_{ox}/W_{dm}$) related with the strength of the short channel effect, the value of α is determined by the combination of the velocity saturation and short channel effects. It is obvious from (6) that as the dependence of β on the gate voltage (V_g) (*ie* difference between β_1 and β_2) becomes smaller, α decreases. This means that the value of α becomes smaller with decreasing $m \cdot L/\mu_{eff}$, and when *L* is fixed its value is determined by m/μ_{eff}. However, in determining the value of α, the velocity saturation is a more dominant factor rather than the short channel effect, due to a relatively smaller impact of the short channel effect on *m*.

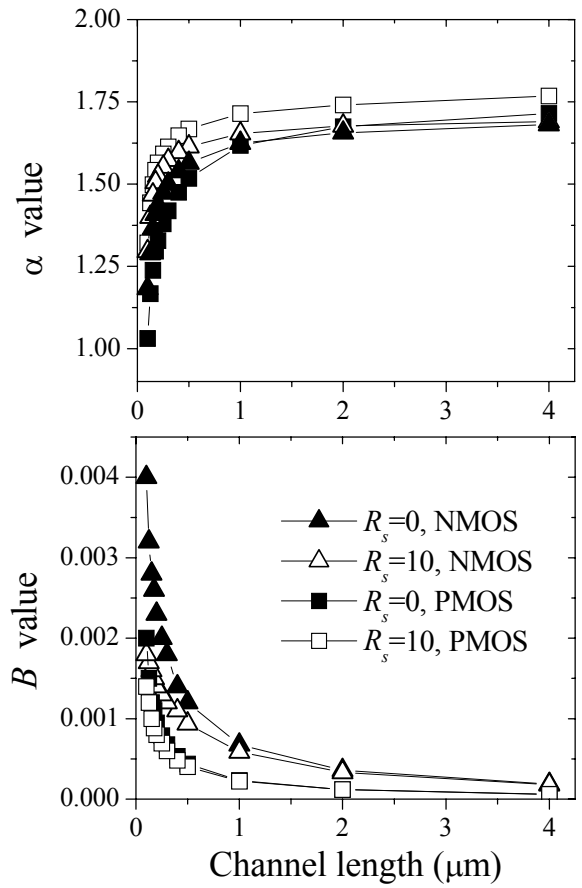

Fig 6. Simulated values of α and *B* for uniformly doped N- and P-MOSFETs using the analytical models in (4) and (5), as a function of channel length. N_a = 2×10^{18}/cm^3 and N_d =8×10^{17}/cm^3. R_s is in the unit of Ω.

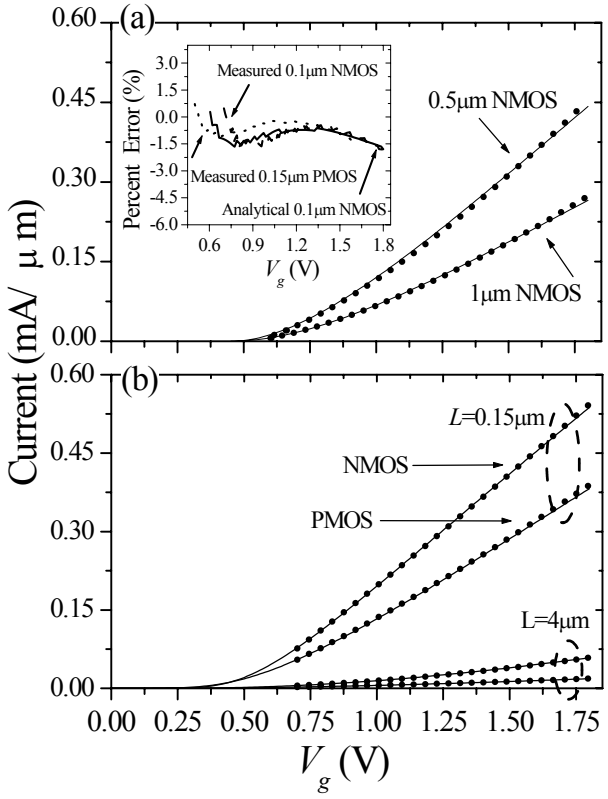

Fig 7. Examples of the comparisons of (a) the analytically calculated and (b) the measured I_{dsat} (thin lines) to the reproduced I_{dsat} (thick dotted lines) using the α–power law model with the extracted values of α, *B* and V_{TH}. Inset: Examples of the percent difference of the α–power law model relative to the measured and analytical data against V_g.

Fig 7 compares the α–power law model to the measured and the analytical data. Excellent reproduction of both the measured and the analytically calculated I_{dsat} using (5) are achieved using the α–power law model. These results clearly confirm the validity of the α–power model. The percent errors of the α–power I_{dsat} relative to the measured and to the analytically modeled I_{dsat} are less than 2% in the wide range of V_g, as seen in the inset.

The key point of the analysis of this section is that since α, *B* and V_{TH} are basically determined by the short channel effect and the velocity saturation, the compact α–power law model can be applicable to future advanced MOSFETs with any structures. Therefore, we can continue to use the α–power model for the power estimation of the next generation MOSFETs as well as for the gate delay time evaluation.

5. CONCLUSION

In this paper, we have presented a compact analytical drain current model for short channel MOSFETs and elucidated the physical origins of the α–power law model providing analytical expressions of α and *B*. This paper clarifies for the first time the applicability of the α–power law model for future scaled MOSFETs by using both analytical and experimental approaches. Our compact and predictive model will provide CMOS engineers and circuit designers with a convenient and accurate way to start their advanced research.

For the future research, the most important extension to this work will include the further refinements of the equations presented here including the p-MOSFET case, derivation of corresponding α-power model in the triode regime, and practical applications to various circuits. It would be also interesting to derive the α-power law model using different approaches such as a MOSFET capacitor model and to find its validity of the model in the nano-metric technologies.

6. ACKNOWLEDGEMENTS

This work was partly supported by the JSPS Research for the Future Program in Japan. Hyunsik Im thanks the QSRC (KOSEF) at Dongguk University for its assistance.

7. REFERENCES

[1] K.Chen et al, "An accurate semi-empirical saturation drain current model for LDD N-MOSFET", IEEE Electron Device Lett., vol 17, 1996, pp. 145.

[2] K.Y.Toh, Ping-Keung Ko, and R. Meyer, "An engineering model for short channel MOS devices", IEEE J. Solid State Circuits, vol 23, 1988, pp. .950-958.

[3] T.Sakurai and A.R.Newton, "Alpha power law MOSFET model and its applications to CMOS inverter delay and other formulas", IEEE J. Solid State Circuits, vol 25, 1990, pp. 584-594.

[4] S. Takagi, M. Iwase, and A. Toriumi, "On universality of inversion-layer mobility in n- and p-channel MOSFETs", IEDM technical Digest, 1988, pp. 398-401.

[5] G. W. Taylor, "Velociyu-saturated characteristics of short channel MOSFETs", AT&T Bell Lab. Tech. Hournal, vol **63**, 1984, pp. 1325-1404.

[6] D.M.Caughey and R.E.Thomas, "Carrier mobilities in Silicon empirically related to doping and field", Proc.IEEE, vol 55, 1967, pp. 35.

[7] C.G.Sodini et al, "Effect of high fields on MOS performance", IEEE Trans. Electron Devices, ED-31, 1984, pp. 1386 - 1393.

[8] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, "A new method to determine MOSFET channel length", IEEE Electron Lett. ED-1, 1980, p. 170.

[9] Hyunsik Im, T. Inukai, H. Gomyo, T. Hiramoto, and T. Sakurai, "VTCMOS characteristics and its optimum conditions predicted by a compact analytical model", Proceeding of ISLPED, CA, 2001, pp. 123-128.

[10] Y.Taur and T.H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 1998, chapter 3.