TUTORIAL 2

FPGAS: COMPUTER-AIDED DESIGN, APPLICATIONS AND FUTURE ARCHITECTURES

Speakers:

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Background: With increasing system complexities and the need to reduce manufacturing costs, use of FPGAs in SOC designs is becoming inevitable. An FPGA component in SOC would increase fault tolerance and product durability, because the FPGA fabric can be tailor-made in the running environment of the system with new configurations to either overcome faults or reflect updates to the original design. This tutorial addresses issues that facilitate utilizing FPGAs in such a context. The target audience consists of circuit designers, CAD engineers and academic researchers.

Description: The first part of the tutorial covers existing and emerging commercial and academic FPGA architectures. We discuss the effects of different architectural options such as the granularity of functional units on the FPGA, size and physical distribution of memory modules within the FPGA fabric, embedding the FPGA fabric within an ASIC design or vice-versa, hierarchical structures and communication mechanisms for inter- and intra-FPGA data transfers.

The second part describes computer aided design methods for FPGAs, including synthesis, technology mapping, and physical design. Different design effort / quality requirements at the development and the final optimization phases call for approaches that provide trade-offs between short design cycles and high clock frequencies. Higher quality expectations require interaction between synthesis and physical design. We also address the need for incremental design flows. Finally, we will address physical design algorithms that facilitate runtime reconfiguration of the FPGA fabric.

The third part surveys current C-to-hardware methods, including languages, compilation and high-level synthesis. Such methods are necessary for fast HW/SW co-design of large SOC designs. Memory block allocation in the FPGA fabric and resource allocation / scheduling will be discussed.

The fourth part will survey FPGA and reconfigurable computing applications that have shown significant improvements over ASIC implementations in terms of speed, power consumption and size. The present state and the future of dynamically reconfigurable systems will be discussed.