TUTORIAL 1

HIGH PERFORMANCE INTEGRATED CIRCUIT ANALYSIS AND DESIGN INCLUDING ON-CHIP INDUCTANCE

Speakers:

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Background: On-chip inductance significantly affects the performance of chips in current technologies. These effects are expected to increase in future technologies due to several technology trends. Some of these trends are the exponentially increasing operating frequencies, lower resistivity interconnect (such as copper), low K dielectrics, faster devices (such as SOI and SiGe technologies), improved cooling techniques, and wider busses. The target audience consists of circuit designers, CAD engineers, and academic researchers. Familiarity with basic concepts in circuit design, model order reduction, extraction techniques, and design methodologies is assumed.

Description: The first part of the tutorial discusses the growing importance of on-chip inductance and its effects on propagation delay, rise time, power consumption, and noise. These effects are discussed both quantitatively and intuitively. This part also characterizes how important inductance effects are in current technologies.

The second part discusses the problem of inductance extraction. 3D full extraction techniques are discussed. Other techniques with lower computational complexity are also discussed such as 2 _ D and 2 D extraction techniques and analytical approximate methods. The problem of determining the return paths is also discussed for these approximate techniques. The sensitivity of delay and performance estimations to errors in extracted inductance values is also discussed.

The third part discusses noise and inductive coupling effects. Wide busses are of specific interest. Model order reduction techniques that can efficiently handle multi-input circuits with large amount of coupling are also discussed. Realizable reduced order models are presented for RLC circuits.

The fourth part discusses design methodologies including inductance. Physical design and timing of integrated circuits including inductance is presented. The effects of inductance on repeater insertion, impedance matching, and wire and transistor sizing are discussed.

The fifth part discusses inductance effects in global distribution networks such as clock and power distribution networks.

Finally, future trends and expectations for inductance effects with technology scaling are discussed in the sixth part.