Metrics for Structural Logic Synthesis

Prabhakar Kudva
IBM TJ Watson Research Center
Yorktown Heights

Andrew Sullivan William Dougherty
IBM Technology Group
Hopewell Junction, NY

Abstract

Routability or wiring congestion in a VLSI chip is becoming increasingly important as chip complexity increases. Congestion has a significant impact on performance, yield and chip area. Although advances in placement algorithms have attempted to alleviate this problem, the inherent structure of the logic netlist has a significant impact on the routability irrespective of the placement algorithm used. Placement algorithms find optimal assignment of locations to the logic and do not have the ability to change the netlist structure. Significant decisions regarding the circuit structure are made early in synthesis such as during the technology independent logic optimization step. Optimizations in this step use literal count as a metric for optimization and do not adequately capture the intrinsic entanglement of the netlist. Two circuits with identical literal counts may have significantly different congestion characteristics post placement. In this paper, we motivate that a property of the network structure called adhesion *can make a significant contribution to routing congestion. We then provide a metric to measure this property. We also show that adhesion as measured by this metric can be used in addition to literal counts to estimate and optimize post routing congestion early in the design flow.*

1. Introduction

Early synthesis transformations where little physical design information is available or usable have significant impact on the structure of a logic circuit. By the time the synthesis process has reached the late timing correction stage, the network structure is only changed in limited ways. The logic structure remains unchanged by the placement algorithms. The quality of the placement is not only determined by the placement algorithm but by the structure and flexibility of the logic network as well. Two boolean equivalent logic networks may have remarkably different quality of placement results with the same placement algorithm. It has been noticed during high peformance design that certain forms of factoring and cloning can increase the wiring congestion and hence the difficulty in routing.

As device geometries shrink, the interconnect delay between gates will begin to dominate the performance of the finished circuits. Thus, the performance of the circuit will depend heavily on the ability of the placement step to find an assignment of gates to physical locations on a chip such that the impact on interconnect delays are minimized. Given this, it is imperative that future logic synthesis systems more directly relate the multi-level logic optimization and technology mapping steps to the physical placement of the circuit components.

Technology independent synthesis has primarily used the notion of literals and levels in the design network as a measure for optimization. The improvement in the number of literals and levels are assumed to be proportional to the area and performance of the design respectively. Literals measure the number of connections in the network and to a very first order give the overall area of the circuit. It is used even though it does not precisely predict area because at the technology independent stage of the design, it is the best metric available. We seek an additional such property that will predict routability. Such a metric should distinguish between the *structure* of two boolean equivalent circuits that have the same literal count.

The question asked is whether there are properties of logic network graphs that can be improved without constraining the placement algorithm. The need for such a property that describes structural flexibility is motivated in the form of a property called *adhesion* proposed in this paper. A method to measure this property is developed. This metric helps identify circuits that have lower adhesion and therefore are more likely to result in placements that meet varied physical constraints and produce solutions with better wiring characteristics. Intuitively, the less intrinsically entangled a design network is, the easier it is to place and will result in a less congested design. Congestion and routability of a design in turn affect the performance of the design.

2. Related Work

Work in the area of congestion reduction during technology independent optimization is extensive and typically uses placement models or makes assumptions regarding placement. Research along this line of work [8, 11] has shown promising results. Our paper on the other hand seeks to explore the question whether congestion can be predicted and reduced in the technology independent phase without making any assumptions about placement. This is important since it is hard to ensure that the placement assumptions made during technology independent optimization can be realized during placement.

[10] uses a lexicographic ordering of inputs to improve routability during factorization. The impact on the congestion of the overall network due to the local optimization is not addresed. Wire planning [5] evaluates the placement characteristics of circuits during logic synthesis and approaches the same problem from a different angle. The wire planning approach assumes that the locations of IO pins are known. Constraints are generated from placement models and synthesis is performed using the constraints. Assumptions about i/o locations for pins of a region where local optimizations are being performed are generally difficult to preserve post placement. In our approach, we explore whether we can find a property and relevant metrics based only on the network graph that can predict congestion characteristics during optimization early in the design flow. The metric is based on the connectivity of the network graph implementing the logic function, and does not make assumptions about i/o locations and does not require the generation and feedback of placement constraints to synthesis.

Statistical interconnect prediction methods such as Rent rule [3], do not distinguish between two networks which have the same number of connections. Interconnect estimates are based primarily on the number of logic gates and IOs. Therefore, they are unsuitable as predictors for routability optimization during technology independent synthesis.

3. Background

0-7803-7607-2/02/$17.00

Some research exists on defining and analyzing adhesion in general graphs. The use of such techniques spans a wide range of fields from network reliability to social anthropology [15, 6, 9] and are accompanied by various algorithms. Depending on the application area, adhesion of graphs have been defined in terms of network densities, k-connectivity and clique behaviors. In this section, we will review relevant definitions and graph-theoretic issues.

3.1 Structural Metrics in Social Networks

Some representative works have been studied in the area of social networks. One application of graph theory to social adhesion [15, 6, 9] is discussed in more detail to explain the limitations of current state of the art. We will describe the technique, it's limitations and the need for a suitable metric as it pertains to the domain of logic synthesis. Since we are exploring a novel approach, we do leave open the possibility that certain other techniques are indeed available in these areas that could be more suited to applications in logic synthesis.

In a recent paper [15], the state of the art measurement metrics for social adhesion are discussed and shown to be misleading. Previous definitions of social adhesion measured in terms of the number of paths between pairs of nodes are shown to be erroneous. A tree network and a star network are shown to be counter examples that have a high density (number of paths between pairs) but very low adhesion. Further, examples are given where an edge is moved between one pair in the network to another pair, while making the network more intuitively adhesive but where the measure fails to capture it correctly. Alternate definitions are provided in the same papers [15], as more accurate metrics for social adhesion.

Social networks or groups consist of members and social relations. A network can be represented as a graph $G(V, E)$, where the set of vertices V represent members of the network and the set of edges E, the social relationships. The graphs may be directed or undirected and the edges may be weighted. Intuitively, the ability of a group to hold together increases with the number of independent ways the group members are linked.

We briefly review some of the definitions and concepts in social adhesion given in [15]. The most general definition of social adhesion is presented in Definition 1

DEFINITION 1. *A group is adhesive to the extent that multiple independent social relations of its members are pairwise resistant to being pulled apart.*

further refined as,

DEFINITION 2. *A group is adhesive to the extent that social relations distributed among different pairs of members prevent the group from being pulled apart by the removal of subsets of edges.*

further refined as,

DEFINITION 3. *A group's adhesion is equal to the minimum number of edges between pairs of members that if removed would disconnect the group.*

A Blocking procedure is described in [9] in terms of a recursive algorithm to find $k - connectivity$ of sub-graphs induced by each k cut-sets at the current level of connectivity. The algorithm recursively computes sub-groups induced by the cut-sets. Our analysis of this algorithm shows that due to the extremely high level of fanout and reconvergence in typical logic networks, clearly identifying groups and application of the recursive blocking among overlapping groups becomes very difficult and impractical. Further, the groups are often asymmetrical in the number of vertices making it difficult to obtain a single number that gives adhesion. In the absence of clearly identifiable hierarchy or groups, the blocking procedure of [9] is not suitable to a logic network.

3.2 SAPMC: Problem Definition

In this section we will review some of the basics of the well known all pairs min-cut problem with respect to graphs. Later we will show that SAPMC is one way to measure adhesion in a netlist. An $s - t$ *cut* for an undirected graph $G(V, E)$ with nonnegative capacities on its edges, and two distinguished vertices s and t is a partition of the vertices into two parts, one containing s and another containing t. The capacity of the cut is the sum of the capacities of the edges going from the part containing s to the part containing t. An $s-t$ min-cut is a cut of minimum capacity among all $s-t$ cuts.

The "sum of all-pairs min-cut" (SAPMC) computes the sum of the capacities of $s-t$ mincuts for each pair of vertices $s, t \in V$ [2].

A standard method used to solve s, t cuts of undirected graphs in a compact way is to use *Cut trees*, also known as *Gomory-Hu trees*. For the purposes of this paper, we will assume that the SAPMC algorithm can be solved using efficient versions such as [4] of the Gomory-Hu algorithm [12].

The most efficient exact algorithms are $O(n-1)F(n,m)$ [2], where $F(n,m)$ is the time taken to solve a max-flow problem on an n-vertex m-edge network, and therefore the SAPMC algorithm often becomes impractical for graphs that run into thousands of vertices.

Alternately, it has been shown that heuristics which *approximate* the cost to almost 99 % accuracy can run in linear time [16]. For most practical tasks such as those proposed in this paper, the accuracy of these approximations may be sufficient. Although our paper follows the exact approach for theoretical purposes, other approximations to adhesion can be considered.

4. Adhesion in Logic Networks

4.1 Definition of Adhesion

We adapt adhesion as given by Definition 3 to logic networks in Definition 4. Examples of the pervasiveness of this intuition appears in the various min-cut algorithms used for placement.

DEFINITION 4. *The adhesion of a logic network represented by an undirected graph $G(V, E)$ can be measured by the minimum number of edges between all pairs $s, t \in V$ that if removed from the graph would disconnect the graph.*

For measuring connectivity in a technology independent netlist we propose a novel use of the all-pairs minimum cut problem to determine the minimum cut size of all pairs of nodes of a graph. Although for reasons of brevity and explanation the only metric described is the "sum of all-pairs min-cut" (SAPMC), it is acknowledged that other metrics for adhesion are possible. *Adhesion refers to a property of the graph and SAPMC is the metric for the property*. In the rest of this paper, they will be used interchangeably.

LEMMA 1. *The adhesion in an undirected graph representing a logic network as given by definition 4, can be measured by the Sum of all-pairs min-cut (SAPMC) for the graph.*

4.2 Application of Adhesion

We conjecture that adhesion can describe routability after placement and can be used by various logic optimization techniques to improve the connectivity of the circuit.

CONJECTURE 1. *Networks with a lower adhesion value will on the average have better routability post placement.*

It is conjectured that circuits optimized using adhesion will have more structural flexibility and will generally result in placed circuits

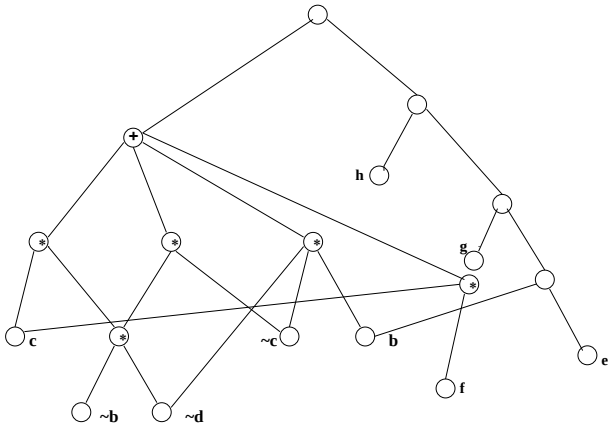

Figure 1. Original Circuit

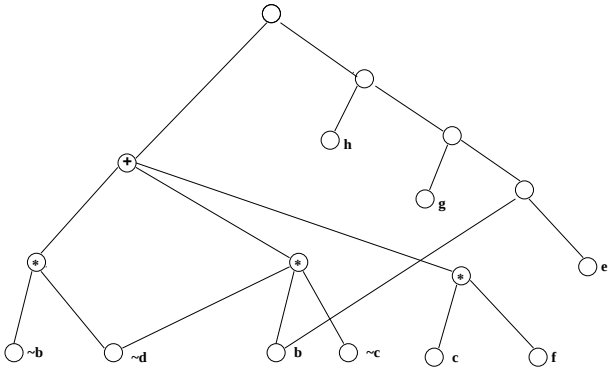

Figure 2. Optimized Circuit 1: opt1

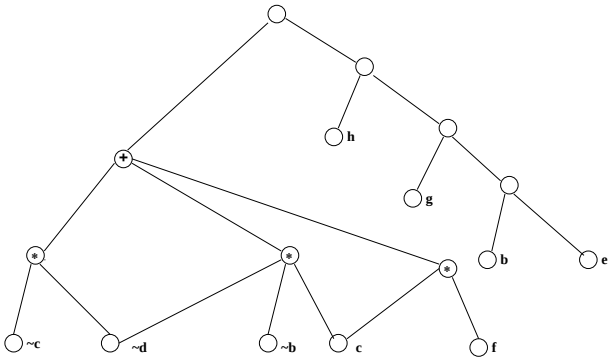

Figure 3. Optimized Circuit 2: opt2

with less wire length and routing congestion. The phrase *on the average* is used to indicate that just as *literal counts* approximately mirror area and *number of levels of logic* measure delay, adhesion approximately mirrors routability. Conjecture 1 is evaluated emperically in section 5.1 and 5.2.

CONJECTURE 2. *Using adhesion during logic synthesis transformations will result on the average in better routability post placement.*

Conjecture 2 is evaluated in Section 5.3. Since our goal is the optimization of logic networks which are hypergraphs, we first transform such networks into a pure graph by using a clique model. A clique model replaces a net connected to k pins with a complete subgraph of $n(n-1)/2$ edges. The standard clique model weights each edge with a value of $1/(k-1)$ and other weighting schemes have been proposed. Based on our experiments we have found that most clique models provide equivalent connectivity information and thus have marginal impact on our metric.

Adhesion can be used in a wide variety of multi-level optimizations, as well as late timing correction algorithms such as factoring, rewiring, decomposition, buffer insertion, mapping and cloning just to name a few. We will illustrate some examples of the application.

4.3 Example: Adhesion in Factorization

Consider the unoptimized network of Fig 1. Assume both a literal and it's complement are available at the inputs. Two possible optimizations are applied and the resulting networks, opt1 in Fig 2 and opt2 in Fig 3 are obtained. Consider applying the SAPMC, to the graph in Fig 2, i.e., sum of the mincut between every pair of nodes is 273 with a total number of connections to be 21. Both optimizations opt1 and opt2 reduce the number of connections to 18. The opt1 optimized circuit has a SAPMC cost of 173 while the opt2 optimized circuit has a SAPMC cost of 152. From this we deduce that opt2 is a better optimization for the same connection cost, which also appears intuitively correct from observing the networks.

4.4 Example: Adhesion in Rewiring

Consider the network in Fig 4. Fig 4 (i) shows an unoptimized circuit, Fig 4 (ii) shows the addition of two possible wires which will make the wire marked to be redundant and can be removed. Fig 4 (iii) shows the equivalent transformed circuit. Such an optimization is typically performed in logic synthesis systems [13] to reduce the number of levels.

Consider the situation where signals a, b, c, are early arriving signals and have positive slack. Then one can ask the question whether the transformation, which preserves the number of logic gates indeed had any beneficial value, or made the network more $adhesive$ causing it to be less routable later in the design flow.

An evaluation of the adhesion as defined earlier, gives adhesion values of 36 and 42 showing that Fig 4(i) is a better circuit, the transformation of Fig 4(iii) is not preferable for congestion given the timing constraints described earlier.

5. Measurements of Adhesion

The experimental evaluation of the correlation of the technology independent graph adhesion with the post technology mapped placement consisted of generating multiple versions of the same circuit with identical literal counts but different congestion values. The experiments were conducted over 27 designs in the MCNC and ISCAS combinational and sequential benchmark sets. To generate the circuit variants, a version of the fast extraction, f_x logic synthesis transform [14] was modified to randomly select an improvement rather than operate in a greedy fashion. This process was repeated until f_x was unable to improve the circuit further, leading to a final result that was as optimized as possible, but different from run to run. Each of the benchmark designs was synthesized 25 times using the modified f_x transform. In order to remove any layout effects due to technology mapping the library was limited to two input nand gates. Each of these designs was then placed 25 times with independent random IO locations along the perimeter of the placeable area. The placement tool used a combination of quadrisection and partitioning algorithms similar to those given in [1, 7]. A total of 16875 design points were considered.

To cancel out IO placement affects on congestion, representative

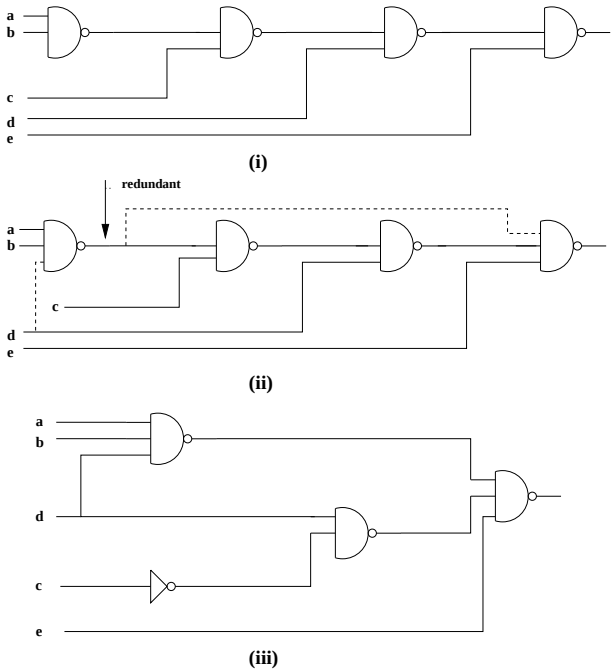

Figure 4. Example of Rewiring

Table 1. Max Congestion Fit

Variables	R square	Residual Std. Error
Num of Cells	0.866	21.70
Literals	0.844	23.46
Adhesion	0.643	35.46
Levelization Metric	0.404	45.86
Normalized APMC	0.086	56.79
Average Fanout	0.077	57.05
Literal Density	0.007	59.18

Table 2. Avg Congestion Fit

Variables	R square	Residual Std. Error
Num of Cells	0.851	17.48
Literals	0.825	18.90
Adhesion	0.620	44.20
Levelization Metric	0.394	35.24
Average Fanout	0.062	43.87
Normalized APMC	0.047	43.67
Literal Density	0.009	45.09

Table 3. Total Wire Length Fit

Variables	R square	Residual Std. Error
Num of Cells	0.953	11.02
Literals	0.942	12.21
Adhesion	0.860	18.99
Levelization Metric	0.618	31.41
Normalized APMC	0.137	47.23
Average Fanout	0.116	47.79
Literal Density	0.000	50.82

congestion and wire length numbers were derived for each synthesized circuit by averaging values over the 25 runs. Two interesting cases were identified for each benchmark; circuits with identical literal counts but different SAPMC costs, and circuits with lower literal counts but higher SAPMC costs. From this subset of the data, linear regression models were built for the entire group and for each individual circuit. Tables 1, 2, 3 show the regression results for single variable models built using the the entire data set. Stepwise regressions were performed to understand the combined effects of the various variables, and are given in Table 4. Additional experiments with polynomial regression models showed poorer correlation than the linear models.

5.1 Single Variable Regression

First we will discuss the correlation of each individual variable. Later we show that when taken together they correlate very well with the post placement measure of congestion. Tables 1, 2 and 3, show the correlation/goodness or $r - squared$ measure of the linear regression fit of the measured maximum congestion to each of the individual variables, average congestion and total wire length data respectively. For max congestion, in table 1, the literal variable based models of the aggregate data set had an $r - squared$ value of 84 % , while adhesion based models showed a 64 % correlation. Similarly, the average congestion measure showed, 82 % and 62 % for for the same variables. The total wire length measure exhibited the best correlation with each of the individual variables separately, 94 % and 86 % respectively. All measures correlated very well with the *number of cells* in the design. Other heuristic variables such as *average number of fanouts* in the design showed very poor correlation to all the measures indicating that the number of fanouts alone is not enough to measure adhesion, but the nature of the entanglement created by such fanouts is more significant. *Literal density* measured as the ratio of literals (number of connections) to the number of gates in the design similarly correlated very poorly. This is due to the fact that the nature of the connectivity is more important than the number of connections per unit gate. A *levelization metric* which measures the number of nets that cross levels in the levelized graph of the network is shown to be next in importance to adhesion.

Figures 5 through 9 demonstrate the individual variable correlations with a linear regression observed earlier. Among all the figures, we notice average fanout, levelization and literal density fare poorly. Known metrics such as cell count and literal count do quite well. Adhesion is the only one among the newer metrics that is shown to perform quite well.

5.2 Stepwise Regression

Table 4 shows the stepwise regression model. $f()$ denotes a model of the variables. L denotes number of literals, C the cell count, A the adhesion value, B the number of boxes (library gates) in the design, L_d, the literal density, F the average fanout, O all other variables in the model. The stepwise regression was started with the literal variable L, each new variable was added to the model based on the highest goodness or $r - squared$ value obtainable. The $r - squared$ values are then reported for each of the measures of max congestion, average congestion and total wire length. The interaction effects were limited to 3 linear terms of the variables in the model. For example, even the simple formula $a.L + b.C + c.A + d.L.A$ where a, b, c, d are co-efficients produced good correlation. It is important to note that during the technology independent phase only literal count L and adhesion A can be computed for use in optimizations. The *levelization metric* appears to be subsumed by the adhesion metric in the stepwise regressions.

From table 4, when the literals, cell count and adhesion are taken together,the accuracy of the models increases to at least 98 %. From this observation, we conclude that the three primary contributors of maximum congestion are *number of connections*, *cell count*, and

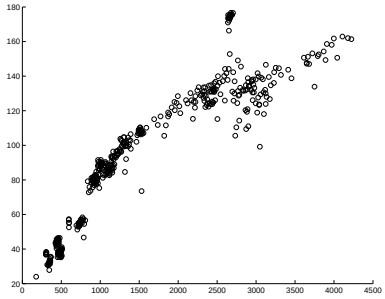

Figure 5. Lit. Count (x) vs Max Cong (y)

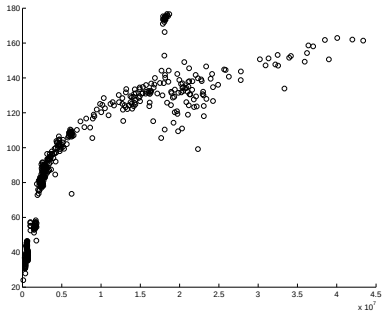

Figure 6. Adhesion (x) vs Max Cong (y)

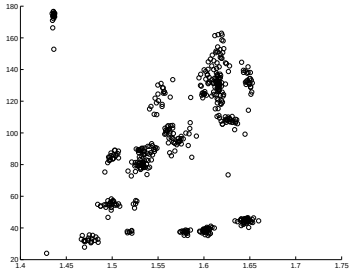

Figure 7. Avg Fanout (x) vs Max Cong (y)

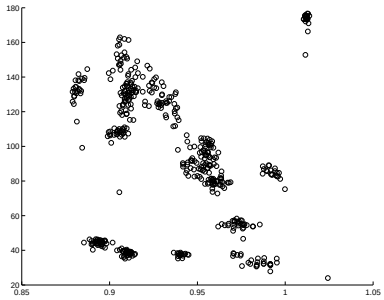

Figure 8. Level Metric (x) vs Max Cong (y)

adhesion. Most state of the art logic synthesis systems already optimize the first two variables (i.e., literal count and cell count) aggressively. To the best of our knowledge, the adhesion variable is not considered in any optimization, although it is a major contributor to the overall congestion of the design.

The increase in correlation occurs because each metric is capturing something that the other cannot. The literal count captures the number of wires that are needed, but cannot judge how many wires want to travel to the same places or how far away from the optimal path they will need to go in order to reach their destination. A high adhesion value on the other hand captures this information, but cannot distinguish a large number of low cost paths from a small number of high cost paths. While it would seem that the size information could be added to the adhesion cost by some normalizing factor, all attempts at doing this substantially decreased the correlation in our experiments.

Adding additional variables into the regression models, significantly increased the complexity of the models but improved the correlation only slightly (about 1 % with three additional variables added).

5.3 Optimization Using Adhesion

As shown in section 4.2, adhesion can be used to make decisions regarding the choice of optimizations. Typical choices between cloning and buffer insertion, rewiring choices and factorization need to be reconsidered with the new metric. We do not address the vast area of such optimization possibilities, only a simple experiment was used to illustrate that such a possibility holds promise. The algorithm f_x [14] which works in a loop and performs extraction was modified slightly from its normal operation. One implementation of f_x finds the factors with with the most amount of literal saving, in each iteration. In case of tie, a random optimization is picked. In our case only this particular step of tie resolution was modified to use adhesion as a secondary property based on which the factor was picked, rather than randomly. Due to the nature of this local optimization and the nature of the f_x algorithm itself, the final results varied signficantly in literal count betwen the normal operation of fx and the modified operation. This problem is inherent in the greedy nature of f_x due to lack of lookahead. From the results, we picked designs from the benchmarks where the number of literals were within 5 % of each other. The results of this experiment are given in Table 5. From the congestion results, we can say there is promise in modifying the optimization algorithms to take into account adhesion. In Table 5 experiments were run using the partitioning based placer. MC_{nor} indicates the maximum congestion with normal fx, MC_{adh} indicates the maximum congestion with the modified fx algorithm and $SAPMC_{nor}$ and $SAPMC_{adh}$ are the adhesion values respectively.

The exact nature of the algorithms as well as the nature of the global and local metrics are worthy of future research. Our experiments only illustrate the promise of using adhesion and do not illustrate the best way of doing so.

Table 4. Stepwise Regression

Model	Max Con	Avg Cong	TWL
$f(L)$	0.841	0.825	0.942
$f(L, C)$	0.932	0.922	0.961
$f(L, C, A)$	0.984	0.983	0.998
$f(L, C, A, B)$	0.988	0.987	0.999
$f(L, C, A, B, L_d)$	0.989	0.988	0.999
$f(L, C, A, B, L_d, F)$	0.990	0.989	0.999
$f(L, C, A, B, L_d, F, 0)$	0.993	0.991	0.999

6. Conclusions and Future Work

We have shown that adhesion is a property of a logic netlist that contributes significantly to it's routability and that SAPMC can be used to measure adhesion. Our results show the correlation of adhesion to average, maximum and total wire length. The results demonstrate that taking into account adhesion early in logic synthesis transformations hold significant promise. Other influential properties such as total cell count and literal count are already opti-

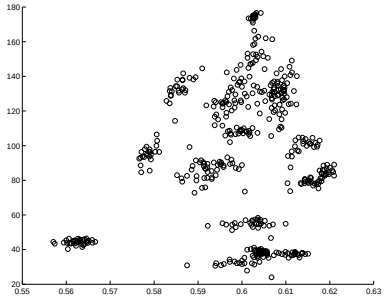

Figure 9. Lit Density (x) vs Max Cong (y)

Table 5. Modified f_x Optimization Results

Circuit	MC_{nor}	MC_{mod}	$APMC_{nor}$	$APMC_{mod}$
C880	63	61	681128	643362
S420	25	25	40375	40375
C17	8	8	205	205
S820	66	63	328125	321772
S641	44	42	160944	158527
S382	32	28	95789	76108
S349	36	35	81619	79222
C1908	79	67	781140	763519
S838	30	30	154769	154769
C432	75	72	629335	621463
S1423	107	83	2458040	2202390

mized by current logic synthesis systems.

Adhesion can be used in conjunction with other properties such as literal count, number of levels and cell count to decide the benefit obtained from a logic synthesis transform. The weight given to each metric will depend on the property being optimized. As illustrated in Section 4.3 adhesion can be used to prefer more flexible networks with better routability characteristics in the optimizations.

A key area of research is the development of a synthesis approach that uses adhesion. An incremental analysis tool that will evaluate the adhesion cost of a change proposed by a synthesis transform is necessary. For incrementally updating the cost, it is required that recomputation of the adhesion metric is fast. A mechanism for lazy evaluation and identifying dependencies between vertex costs is also necessary.

One of the drawbacks of the use of the use of exact SAPMC to measure adhesion is it's lack of scalability with the number of vertices. As part of ongoing research, we have developed a variety of graph-theoretic approximations for adhesion which are quite accurate, but at a significantly lower runtime cost. The goal is to have run time scale linearly to large chips with millions of placeable objects as well a predict congestion incrementally. The base analysis system will be architected to form a common infrastructure to predict routability at all levels of synthesis, placement and routing in a consistent manner.

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