ECO algorithms for removing overlaps between power rails and signal wires *

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Abstract

Design ECO commonly happens in industry due to constraints or target changes from manufacturing, marketing, reliability, or performance. At each step, designers usually want to modify the existing solution incrementally and keep the design as close as possible to the existing one. In this paper, we address the PSO (Power rail - Signal wire Overlap) problem which solves overlaps between power rails and signal wires due to the changes in power rail design on the top layer of a multiple layer routing region. PSO problems are frequently caused by changes from power delivery system or package design. The new routing solution satisfies the following constraints: 1) Keep the routing of power rails in the new design unchanged. 2) Only the routing of the top two layers is changed. 3) Horizontal (vertical) signal wire segments on the top layer can only move up/down (left/right). At the same time, the new routing solution keeps the routing pattern unchanged. This requires: a) If one end point of a horizontal (vertical) wire segment on the top layer is a fixed pin, this segment can not move. b) If vertical (horizontal) projections of two horizontal (vertical) signal wire segments have overlaps, then the up/down (left/right) relationship should not be changed. c) If two horizontal (vertical) segments belonging to different nets are on the same track, their left/right (up/down) relationship should not be changed as long as the two segments still exist in the new solution. 4) For each signal wire segment, the deviation (i.e., the difference between its new position and the old one) should not exceed the user-defined allowable deviation bound. Different bounds can be set on different segments. We propose two algorithms to solve the PSO problem. Both algorithms guarantee to find a feasible solution as long as one exists. One is faster, while the other makes effort to minimize the total deviation as well as the max deviation. According to time and quality requirements, users can choose an appropriate algorithm to solve the problem. For a set of industrial test circuits, we were able to remove all overlaps between power rails and signal wires with minimal wire deviation.

1. Introduction

In ECO (Engineering Change Orders), a design need go through many changes[1, 5] due to constraints or target changes from manufacturing, marketing, reliability or performance. At each step, designers usually want to modify the existing solution incrementally and keep the design as close as possible to the existing one. In this paper, we address the PSO (Power rail - Signal wire Overlap) problem and propose two algorithms to solve it. PSO problems are usually caused by design changes in power delivery or package - both can be requested from performance, noise, reliability, or marketing considerations. An efficient and graceful solution to PSO is very important due to design constraints and tight schedules during the late ECO stages. For most high-performance VLSI design where mesh power rails are used to provide dense power supply for better signal integrity, the most upper metal layer can be changed due to different reasons such as current consumption requirement changes, package connection changes when the low resistance highest metal are used to deliver power, local routing ECO changes, etc. For most circuits at ECO stage, it is important to minimize disturbance upon the existing converged design while implementing ECO requests.

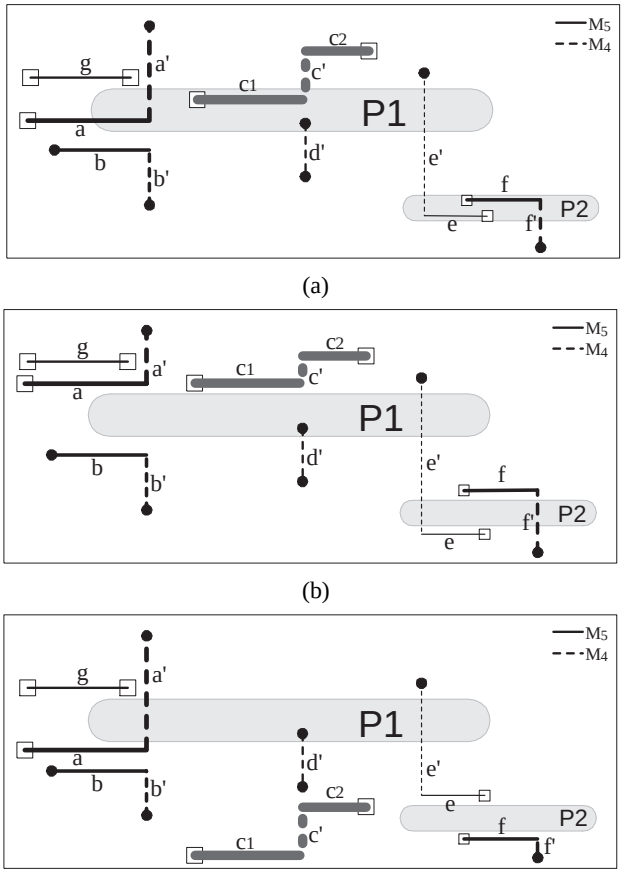

Figure 1: M_5 is presented by solid lines; dotted lines are for $M-4$. (a) Due to the introduction of the new power rails P_1 and P_2 on M_5, some horizontal signal wire segments on M_5 overlap with $P1$ and $P2$. (b) A feasible PSO solution. (c) A solution with P-constraint , track consistency and order consistency violations.

Informally, the PSO problem can be described as follows. On a multiple layer routing region with fixed power rails P on the top

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layer, there is a clean signal wire routing design which has no wire separation violations. Now a new design of power rails $\bar{P}$ on the top layer is adopted to replace the existing one P. Some power rails in $\bar{P}$ may overlap with signal wires or the horizontal/vertical spacing between two wire segments is less than the wire separation requirement. Without lost of generality, we assume the multiple layer routing design is in HVHVH style. We refer to the top layer as M_5 and the second top layer as M_4. M_5 is used for horizontal tracks and M_4 is for vertical tracks. Figure 1 shows an example. We use solid horizontal lines to present the top layer M_5 routing, and doted lines are for M_4 routing. Segments of different nets may have different widths. Due to the introduction of the new power rails P_1 and P_2 (the shadow area), some segments on M_5 overlap with P_1 and P_2.

Our purpose is to find a new clean routing solution without wire spacing violations. At the same time, we hope to keep the topology of new routing solution as close as possible to that of the original one. Thus four constraints are set: 1) Keep the routing of power rails in the new design unchanged. This is required by the problem itself. 2) Only the routing of the top two layers is changed. The changes on the top layer M_5 may cause changes on M_4. However, the changes should not propagate to all layers. By treating all connections to M_4 from lower layers as fixed pins, the changes can be restricted to the top two layers. 3) Horizontal signal wire segments on the top layer M_5 can only move up/down. At the same time, keep the routing design pattern unchanged. This requires: i) If one end point of a horizontal (vertical) wire segment on the top layer is a fixed pin, this segment can not move. This kind of segments is called "P-segment". And its unmovable property is called "P-constraint". Since pins on M_4 may connect to both M_5 and M_3, keep all pins on M_4 fixed and they are treated as a vertical wire segment with a length of zero so that there is no influence to lower layers. In Figure 1, fixed pins are denoted by a solid dot. But some pins on M_5, which are end points of horizontal segments, are allowed to move with the corresponding horizontal segments. They are unfixed pins and they are presented by tiny squares. In Figure 1, horizontal segment b is a P-segment and can not be moved like Figure 1 (c). ii) If vertical (horizontal) projections of two horizontal (vertical) signal wire segments have overlaps, then the up/down (left/right) relationship should not be changed. This is called "order consistency". For example, in Figure 1 (c), horizontal segment e is above f while in the original design, e is below f. So this violates order consistency. iii) If two horizontal (vertical) segments belonging to different nets are on the same track, their left/right (up/down) relationship should not be changed as long as the two segments still exist in the new solution. This is called "track consistency". In Figure 1 (c), vertical segment c' is below d' while c' should be above d' to maintain track consistency. 4) For each signal segment, the deviation (i.e., the difference between its new position and the old one) should not exceed the user-defined allowable deviation bound so that local changes are confined. Different bounds can be set on different segments.

For the given new design of power rails $\bar{P}$, does there exist a clean routing solution satisfying the above constraints? If there is a solution, how to find one? For Figure 1, (b) gives a clean routing solution.

As we notice that, once a segment is moved, it may overlap with some signal wire segments. Consequently these signal segments have to be moved, which may cause overlaps with other segments, etc. In Figure 1 (b), the move-up of a causes g to move up too. Further, the movement of wire segments on the top layer may make some segments on M_4 become longer/shorter and introduce overlaps on M_4.

Note that our problem is significantly different from the overlap removal problem in macro-cell placement [2, 3, 4]. When macro cells are placed based on analytical techniques (e.g., force-directed placement, quadratic placement), there are overlaps between the macro cells. A clean-up phase is needed to shift the macro cells to remove all overlaps. However, PSO problem is significantly more difficult since moving the horizontal wire segments on M_5 also changes the vertical wire segments on M_4.

In this paper, we first give the definition of PSO (Power rail - Signal wire Overlap) problem in section 2. In section 3, we give the definition of *FP-Range* and prove that if all segments move in their *FP-Range* as well as keeping order consistency and horizontal wire separation in the new routing solution, it satisfies the vertical wire separation requirement as well as track consistency and P-constraint. On the other hand, if a solution of a PSO problem exists, the new position of each segment must be in its FP-Range. In section 4, we discuss the construction of the consistency graph. Based on FP-Range and consistency graph, we propose two polynomial-time algorithms PSO-H and PSO-G to solve PSO problems in Sections 5 and 6 respectively. Both algorithms guarantee to find a clean routing solution as long as one exists. PSO-H is faster than PSO-G, but PSO-G makes effort to minimize the total deviation. We show the experimental results in section 7 and conclude the paper in section 8.

2. PSO (Power rail - Signal wire Overlap) Problem

A multiple layer routing region is 3-dimensional. For convenience, we call the 3 dimensions as x, y and z dimension. Each layer is an x-y dimensional plane, where x-axis goes horizontally and y-axis goes vertically. For convenience, let the coordinate of its bottom left corner be $(0,0)$, and W and H be the width and the height of the routing region respectively. In most existing high-performance chips, each layer has its specific track orientation in either horizontal or vertical and its design rule which specifies minimum width and separation of wires. Let s be the half minimum wire separation of a metal layer. To simplify the presentation, suppose the wire separation requirement is $2s$ for both M_4 and M_5. The algorithms proposed in this paper can be easily extended to handle different wire separations for different layers.

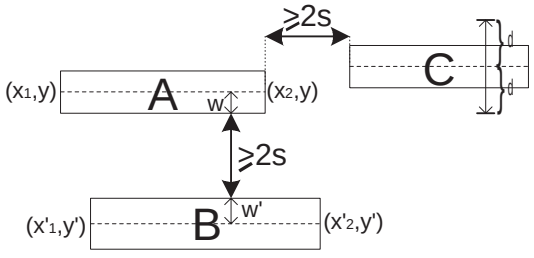


Figure 2: Wire separation requirement illustration.

For a horizontal segment, it can be presented by (x_1,x_2,y,w) where (x_1,y) and (x_2,y) are the end point coordinates of the center line ($x_1 < x_2$), and w is the half-width of the segment. Similarly, a vertical segment can be presented as (y_1,y_2,x,w). For any two horizontal segments (x_1,x_2,y,w) and (x'_1,x'_2,y',w') ($x_2 < x'_1$), if $(x_1-s,x_2+s) \cap (x'_1-s,x'_2+s) \neq \phi$, $|y-y'| \geq w+w'+2s$ must hold; also if $(y-w-s,y+w+s) \cap (y'-w'-s,y'+w'+s) \neq \phi$, $|x_2-x'_1| \geq 2s$. The similar rule applies to vertical segments. Figure 2 gives an example of three horizontal segments. We say a routing solution is a clean solution if it has no overlap or wire separation

violations. Sometimes, we can simplify the presentation. For example, if we do not care the width of a horizontal segment, it is presented by (x_1, x_2, y).

Given a clean routing solution S with N signal nets, there are P power rails on the top layer M_5. Also each signal segment is associated with a non-negative number d called allowable deviation bound, i.e., for a horizontal segment (x_1, x_2, y, w), when it moves up/down, its new position $(x_1, x_2, \bar{y}, w)$ should satisfy that $|\bar{y} - y| \leq d$. Now if this design P is replaced by a new power rail design $\bar{P}$, the wire separation requirement might not be satisfied any more. How to modify the existing routing solution S so that the new routing solution $\bar{S}$ is a clean routing solution as well as satisfying the following constraints?

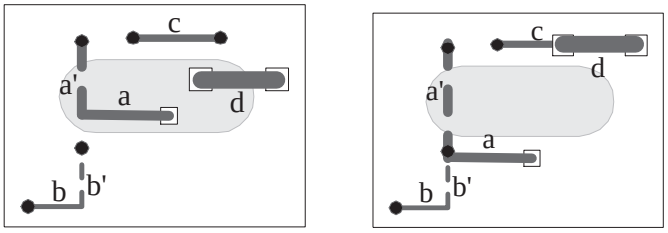
1. The power rails $\bar{P}$ on the top layer are not changed.
2. Only the routing of the top two layers M_4 and M_5 can be changed.
3. Horizontal signal wire segments on the top layer can only move up/down, i.e., the x-coordinate of the two end points of the segment keep unchanged. This is called "Shift movement".
4. The difference between the new position of a wire segment and its old location should not exceed its allowable deviation bound d.
5. If an end point of a signal wire segment on the top layer is a fixed pin, it is called "P-segment" and can not be moved. This property is called "P-constraint". All pins on lower layers are fixed pins and treated as as a vertical wire segment with a zero length.
6. Suppose any two horizontal signal wire segments on M_5 (x_1, x_2, y) and (x'_1, x'_2, y') (assume $y > y'$) have new positions $(x_1, x_2, \bar{y})$ and $(x'_1, x'_2, \bar{y}')$ in the new routing solution $\bar{S}$ respectively. If $(x_1 - s, x_2 + s) \cap (x'_1 - s, x'_2 + s) \neq \phi$, $\bar{y} > \bar{y}'$ must hold. This property is called "order consistency".
7. If two vertical signal wire segments (y_1, y_2, x, w) and (y'_1, y'_2, x', w') (assume $y_2 < y'_1$) belonging to different nets on the same layer satisfy $(x - w - s, x + w + s) \cap (x' - w' - s, x' + w' + s) \neq \phi$, then in the new design $\bar{S}$, if the two segments still exist, $y_2 < y'_1$ holds. This property is called "track consistency".

3. FP-Range (Fixed-Pin-decided Range)

In a PSO problem, since the original power rail design P is replaced by $\bar{P}$, we can just ignore P and simplify the problem as solving the overlaps between power rails and signal wire segments on M_5 as well as satisfying all of the constraints.

If we arbitrarily move one horizontal signal wire segment up or down, not only overlaps between horizontal segments on M_5, but also vertical overlaps on M_4 may be introduced. For example, in Figure 5(b), if horizontal segment d moves up, it overlaps with c. On the other hand, if a moves down, the vertical segments a' and b' on M_4 overlap with each other.

In this section, we discuss how to avoid vertical segment overlaps. The following theorem provides a rule of moving horizontal signal wire segments without introducing vertical wire separation violations. Also the theorem proves that if a horizontal signal wire segments moves out its FP-Range, at lease one of the moving requirements, i.e., order consistency, track consistency, or P-constraint, or wire separation requirement, does not hold any more.



(a) (b)

Figure 3: (a) A PSO problem; (b) Overlaps: vertical segments a and c on M_4; and horizontal segments b and d on M_5

To simplify the presentation, we neglect the widths of wire segments. It's easy to incorporate it into the following theorem. Each item is presented by its xy-coordinates, e.g., one segment is presented as (x_1, x_2, y) and one of its end point is denoted as (x_1, y).

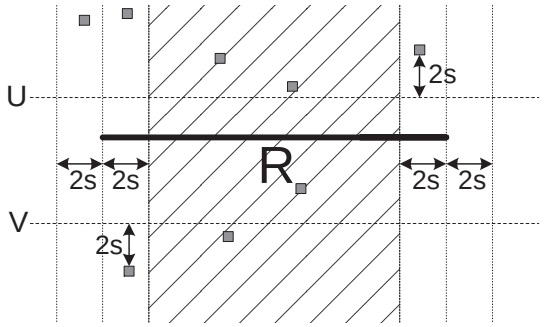


Figure 4: FP-Range illustration. (The tiny squares are fixed pins.)

Suppose the wire separation requirement is $2s$. A horizontal wire segment $R = (x_1, x_2, y_r)$ on M_5 belongs to net n_r. And its two end points are $r_1 = (x_1, y_r)$ and $r_2 = (x_2, y_r)$. If R is a P-segment, it can not be moved. Its movable range is $[y_r, y_r]$. Otherwise, calculate two pin sets $\tilde{P}$ and $\tilde{Q}$. If r_1 is a unfixed pin, $\tilde{P} = \phi$; otherwise let $\tilde{P}$ be the set of fixed pins whose x-coordinate falls in $(x_1 - 2s, x_1 + 2s)$ and do not belong to net n_r. Also if r_2 is a unfixed pin, $\tilde{Q} = \phi$; otherwise let $\tilde{Q}$ be the set of fixed pins whose x-coordinate fall in $(x_2 - 2s, x_2 + 2s)$ and do not belong to net n_r. Let $U = min\{\{y - 2s | y \in \tilde{P} \cup \tilde{Q} \wedge y \geq y_r\} \bigcup \{H - 2s\}\}$ and $V = max\{\{y + 2s | y \in \tilde{P} \cup \tilde{Q} \wedge y \leq y_r\} \bigcup \{2s\}\}$. The range $[V, U]$ is called "FP-Range". Figure 4 shows the FP-Range of a horizontal segment R. As we notice that, if a vertical segment is created or becomes longer/shorter, it is caused by the end points of a horizontal segment. Therefore vertical overlap or vertical wire separation violation is only related to the end points of horizontal segments. When moving R up/down, the pins or segments in the shadow area can not create vertical overlaps with R.

For any two end points a and b on layer M_4, suppose their coordinates are (x_a, y_a) and (x_b, y_b) respectively. And in a new routing solution, their positions are $(x_a, \bar{y}_a)$ and $(x_b, \bar{y}_b)$ respectively.

Lemma 1. *Let all horizontal segments on the top layer M_5 move up/down within their FP-Ranges $[V, U]$ and satisfy horizontal wire separation requirement and order consistency. For any two end points a and b on M_4, if $|x_a - x_b| \leq 2s$, then if $\bar{y}_a \geq \bar{y}_b$, $|\bar{y}_a - \bar{y}_b| \geq 2s$ and $y_a \geq y_b$.*

Proof: Each end point of a wire segment is a pin or it is connected to the other layer through a via. Due to the shift movement of

horizontal segments, some vertical segments are created and some disappear. If a vertical segment $T = (y_1, y_2, x_t)$ is created when a horizontal segment moves up/down, one end point of T must be a pin on M_4. Suppose the pin locates at (x_t, y_1). Since T does not exist in the original design, we let T's end points correspond to the end points of a empty vertical segment $E = (y_1, y_1, x_t)$, which connects to T through a via. In this way, for each end point in the new design, we can find its corresponding end point in the original one.

For convenience, if an end point is an end point of a horizontal segment or it is connected to a horizontal segment through a via, we call this kind of end points "turning point"; otherwise, it is called "fixed point". If an end point is a turning point in the new design, it must be a turning point in the original one since horizontal segments only move up/down. For a fixed point, there is no horizontal segments on M_5 connecting to it. So it must be a fixed pin on M_4 or connected to a fixed pin on M_5 through a via. Therefore, the location of a fixed point is not changed in the new design.

There are 4 cases:

1. Both a and b are fixed points. $y_a = \bar{y_a}$ and $y_b = \bar{y_b}$. Obviously, if $\bar{y_a} \geq \bar{y_b}$, $y_a \geq y_b$. Also in the original design, $|y_a - y_b| \geq 2s$, therefore, $|\bar{y_a} - \bar{y_b}| \geq 2s$.

2. a and b are both turning points. They are connected to horizontal segments through vias. Suppose a and b correspond to horizontal segments A and B respectively. Since $\bar{y_a} \geq \bar{y_b}$, A is above B in the new routing solution. Also the shift movements of A and B stick to "order consistency" as well as satisfying horizontal wire separation requirement, so $|\bar{y_a} - \bar{y_b}| \geq 2s$, and A must be above B in the original routing solution. Thus $y_a \geq y_b$.

3. a is a fixed point and b is a turning point. b must be connected to a horizontal segment through a via. Let the horizontal segment be B. Since a is fixed, $\bar{y_a} = y_a$. Suppose $y_a < y_b$. According to the calculation of B's FP-Range $[V,U]$, $y_a < V$. From $V \leq \bar{y_b}$, $y_a < \bar{y_b}$, i.e., $\bar{y_a} < \bar{y_b}$. This contradicts with our assumption that $\bar{y_a} \geq \bar{y_b}$. Therefore, $y_a \geq y_b$. Since P_v is a fixed pin, and $y_a \geq y_b$, we know $y_a \geq U + 2s > U \geq \bar{y_b}$ according to the calculation of FP-Range. Therefore $|\bar{y_a} - \bar{y_b}| \geq 2s$.

4. a is a turning point and b is a fixed point. The proof is similar to case (3). ¶

Theorem 1. *If all horizontal segments on the top layer M_5 move up/down within their FP-Ranges $[V,U]$ and satisfy horizontal wire separation requirement and order consistency, the new routing solution has no vertical wire separation violation as well as satisfying track consistency and P-constraint. On the other hand, if one horizontal segment moves out of its FP-Range, order consistency, wire separation or track consistency or P-constraint violation is introduced.*

Proof: First, we prove that if all horizontal segments move within their FP-Ranges as well as maintaining order consistency and horizontal wire separation, no violation of P-constraint or track consistency or vertical wire separation is introduced. (If two segments have wire separation violation, we also say they are overlapped.)

If a horizontal segment is a P-segment, its FP-Range makes it unmovable and causes no changes to the new routing solution. If both end points of a horizontal segment are floating pins, it can be moved up/down freely and causes no changes to M_4.

From Lemma 1, we know the relative positions of end points from different nets are not changed in the new design. Therefore, the track consistency is kept. Obviously, the P-constraint is satisfied. We only need to prove that if horizontal segments move within their FP-Range $[V,U]$ as well as keeping order consistency and horizontal wire separation, no vertical segment overlaps are introduced.

Suppose this claim does not hold. Then there exists a horizontal segment $A = (x_1, x_2, a)$ whose new position $(x_1, x_2, \bar{a})$ falls in its FP-Range $[V,U]$, and it causes overlaps between two vertical segments $(\bar{a}, b)$ and $(\bar{c}, d)$ on M_4 in the new routing solution. (We use y-coordinates to denote a vertical segment.) The two segments must belong to two different nets since overlap only occurs between two different nets. Suppose the two vertical segments in the original design is (a,b) and (c,d). They could be an empty segment. (For example, if no vertical segments are connected to A at (x_1, a) through a via, (x_1, a) is a pin on M_4. $(\bar{a}, b, x_1)$ is a new segment and $b = a$. Let it correspond to an empty segment (a, a, x_1) in the original design.) Without lost of generality, suppose $\bar{a} \leq \bar{c}$. Then their positions can be classified into 3 cases as shown in Figure 5.

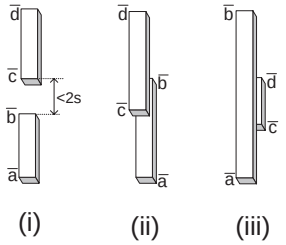


Figure 5: Three cases of vertical overlaps.

1. $|\bar{b} - \bar{c}| < 2s$, this case does not hold according to Lemma 1.

2. $\bar{a} \leq \bar{c} \leq \bar{b} \leq \bar{d}$. According to Lemma 1, we can conclude that $a \leq c \leq b \leq d$.

   i) $a \neq b$ and $c \neq d$. (a,b) and (c,d) are vertical segments in the original solution. But this contradicts the fact that the original one is a clean solution.

   ii) $a = b = c = d$. (a,b) and (c,d) are empty segments, suppose they are created from fixed pins P_a and P_c respectively. Since P_a and P_c belong to different nets, P_a and P_c have to be on different layers. Suppose P_a is on M_5 and P_c is on M_4. Then P_a is an end point of a horizontal segment A. However, A is a P-segment and can not be moved, therefore (a,b) can not be created. $a = b = c = d$ does not hold.

   iii) $a = b = c < d$. (c,d) is a vertical segment in the original design, P_a must be on M_5 above (c,d). Therefore, A is a P-segment, and the edge (a,b) can not be created. $a = b = c < d$ does not hold.

3. $\bar{a} \leq \bar{c} \leq \bar{d} \leq \bar{b}$. According to Lemma 1, we can conclude that $a \leq c \leq b$ and $a \leq d \leq b$. Still this case does not hold. The proof is similar to case (2).

Thus we have proved that no vertical overlaps, track consistency and P-constraint are introduced in the new design.

On the other hand, if a horizontal segment moves out its FP-Range, the constraints, i.e., order consistency, track consistency, P-constraint, wire separation, do not hold any more.

Suppose one horizontal segment $A = (x_1, x_2, y_a)$ moves out its FP-Range $[V,U]$ and all of the constraints still hold. Without lost

of generality, assume A moves below V to $(x_1, x_2, \bar{y_a})$. If A is a P-segment, it can not be moved. Thus A can not be a P-segment. Also if both of A's end points are floating pins, V is $2s$ and A can not go below V. Therefore, we assume at least one end point a of A is not a pin, i.e., a connects to a fixed pin on M_4 through a via or a vertical segment B through a via. Suppose this end point is $a = (x_1, y_a)$ and its new position is $\bar{a} = (x_1, \bar{y_a})$. Also suppose V is decided by a pin P_v below A and its x-coordinate falls in $(x_1 - 2s, x_1 + 2s)$. For convenience, P_v also denotes its y-coordinate. Further we may refer to a horizontal segment as its y-coordinate.

1. $P_v \leq \bar{A} < V$. If P_v is on M_5, it has wire separation violation with $\bar{A}$. Thus P_v is on M_4. However, if a connects to a fixed pin p on M_5 through a via, P_v has wire separation violation with p. If a connects to a vertical segment B through a via, P_v has wire separation violation with B. Therefore, $P_v \leq \bar{A} < V$ does not hold.

   In the following cases, we suppose $\bar{A} < P_v$.

2. a connects to a fixed pin p through a via. When A moves down, a new vertical segment B is created connecting a and $\bar{a}$. If P_v is on M_4 or it has connection to M_4 through a via, it overlaps with B. If P_v is on M_5 and have no connection to M_4, P_v must be an end point of a horizontal segment $\bar{C}$ in the new design and $\bar{C}$ is above the $\bar{A}$. So in the original design, C is above A and C is connected to a vertical segment B. Then B must overlaps with p. Therefore, this case does not hold.

3. a connects to a vertical segment B through a via.

   i)P_v is on M_4.

   (a) P_v is connected to a horizontal segment C through a via, C is below A in the original design. Let $\bar{C}$ be C's new position. To maintain order consistency, $\bar{C}$ is still below $\bar{A}$ in the new design. Then there must be a vertical segment D connecting $\bar{C}$ and P_v. $\bar{A}$ is between $\bar{C}$ and P_v. Therefore, $\bar{A}$ can not have connections to M_4, i.e., B disappears in the new design and $\bar{a}$ must be a pin. Thus in the original design, B connects $\bar{a}$ and a through vias. But P_v is between a and $\bar{a}$. This leads to contradiction.

   (b) P_v has no connection to M_5. P_v is an end point of a vertical segment D. If B still exists, it has to be above D in order to keep track consistency and A can not be below P_v. If B does not exist in the new design, it means B connects a and $\bar{a}$ in the original design. But P_v is between a and $\bar{a}$. This leads to contradiction.

   ii)P_v is on M_5.

   (a) P_v is an end point of a horizontal segment C. C is a P-segment and can not be moved. Therefore, A can not go below P_v in order to maintain order consistency.

   (b) P_v is connected to a vertical segment D through a via. D must still exist in the new design. If B still exists, it has to be above D in order to keep track consistency and A can not be below P_v. If B does not exist in the new design, it means B connects a and $\bar{a}$ in the original design. But B and D have overlap in the original design. This leads to contradiction. ¶

From the above discussion, we can conclude that each horizontal segment must satisfy its FP-Range in the solution of a PSO problem. In other words, if we can not find a solution which make all horizontal segments in their FP-Range as well as keeping order consistency and horizontal wire separation, the PSO problem has no solution.

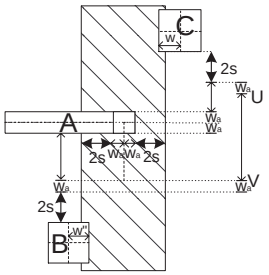


Figure 6: Illustration of the FP-Range calculation when the width is taken into consideration.

Since the locations of fixed pins are fixed, the FP-Range of each segment can be pre-calculated. And when searching for a solution of a PSO problem, we only need to consider order consistency, horizontal wire separation and FP-Range, and do not need to consider M_4 any more.

Suppose the number of fixed pins is N_p. To calculate the FP-Range of a segment, it takes $O(N_p)$. However, we can use a look-up table to speed up the searching instead of checking all of the fixed pins.

Given a routing region (W, H) (W and H could be quite huge), claim a two-dimension array MAP[W/R_w, H/R_h], where R_w and R_h are two positive numbers set by users. The elements of MAP are a set of pins . A pin with location (p_x, p_y) is put in MAP[p_x/R_w, p_y/R_h]. For any horizontal segment (x_1, x_2, y), we only need to search MAP[$(x_1-2s)/R_w \ldots (x_1+2s)/R_w$; $0 \ldots H/R_h$] and MAP[$(x_2-2s)/R_w \ldots (x_2+2s)/R_w$; $0 \ldots H/R_h$]. In this way, the running time can be greatly reduced.

Also this theorem can take width into consideration. Suppose pin width is the same as segment width. As illustrated in Figure 6, we only need to consider the fixed pins falling in the shadow area. Also the $[V, U]$ bound should take the width of segment A into consideration, that is $[V + w_a, U - w_a]$.

Further, this theorem can handle different spacing requirements of different layers without any extra work. Let s_5 and s_4 be the half minimum wire separation of M_5 and M_4 respectively, and usually the upper metal layer M_5 has larger spacing requirement than M_4. Since FP-Range is used to avoid vertical segment overlaps on M_4 under the assumption of no horizontal overlaps on M_5, if we use s_4 to do calculate FP-Range, the theorem still holds.

4. Consistency Graph

From the theorem, we know that the influence of M_4 can be totally reflected in FP-Range. Thus we only need to deal with horizontal signal wire segments on the top layer.

An important property of PSO problem is to keep "order consistency". Given any two horizontal segments $A = (x_{a1}, x_{a2}, y_a)$ and $B = (x_{b1}, x_{b2}, y_b)$, if $(x_{a1} - s, x_{a2} + s) \cap (x_{b1} - s, x_{b2} + s) \neq \phi$ ($2s$ is the wire separation requirement), we define segments A and B adjacent segments. According to order consistency, the relative positions of two adjacent segments should not be changed in the new routing solution. A good way to present their relative positions is to construct a directed graph "consistency graph".

In the consistency graph, each node presents a horizontal signal wire segment. (Without misunderstanding, we use the same notation for segments and nodes, and refer to a node as its corresponding segment, vice versa.) For any two adjacent segments $\bar{A}$ and $\bar{B}$, if A is above B, there must exist a path from $\bar{A}$ to $\bar{B}$.

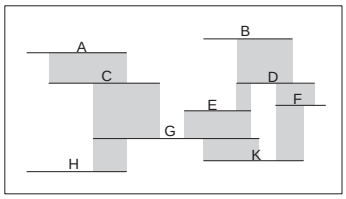
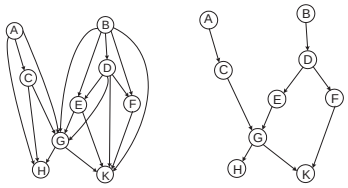


Figure 7: A routing solution of signal wires on the top layer.



(a) (b)

Figure 8: (a) Full connections of adjacent segments. (b) Consistency graph.

One simple way to set up the consistency graph is to create an edge for each pair of adjacent segments. Figure 7 gives a routing solution of signal wire segments on M_5. (Since we only consider horizontal segments, the picture only shows the top layer.) Figure 8(a) is its corresponding graph. But in this graph, a lot of edges are not necessary. For example, segment A is above C and C is above G, thus no necessary for edge (A,G).

For any two adjacent wire segments $A = (x_{a1}, x_{a2}, y_a)$ and $B = (x_{b1}, x_{b2}, y_b)$, let $[x_1, x_2] = [x_{a1} - s, x_{a2} + s] \cap [x_{b1} - s, x_{b2} + s]$ and $(y_a > y_b)$. If there is no other segments overlapped with the rectangle (x_1, y_b, x_2, y_a) where (x_1, y_b) and (x_2, y_a) are the coordinates of the bottom-left corner and up-right corner respectively, the two adjacent segments are called close adjacent segments, and one edge (A,B) is added. The rectangle (x_1, y_b, x_2, y_a) is called "clear box" if no other horizontal segments have overlaps with it. In Figure 7, the shadow areas are clear boxes. Figure 8(b) shows a consistency graph by adding edges for each pair of close adjacent segments.

The construction of consistency graph can be summarized as follows. S_h is the set of the horizontal signal wire segment on the top layer and a segment with index i is presented as s_i.

Function Consistency-Graph-Construction(S_h)
1. for each segment in S_h
2. create a node;
3.
4. for i=1 to $|S_h|$ do
5. for j= i+1 to $|S_h|$ do
6. if s_i and s_j are close adjacent segments
7. then if s_i is above s_j
8. then add_edge(s_i, s_j)
9. else add_edge(s_j, s_i)

For the consistency graph G, the number of nodes is $|S_h|$ and the number of edges is no more than $4|S_h|$. Given any two horizontal segments A and B, if there is an edge between them, there must be a clear box between A and B. Thus each edge corresponds to one clear box. However one end point of a horizontal segment belongs to at most two clear boxes. Since there are total $|S_h|$ segments and $2|S_h|$ end points, the number of edges in the consistency graph is bounded by $4|S_h|$.

It takes $O(|S_h|)$ to check if two segments are close adjacent segments, and the graph construction involves 2 loops. So its worse case runtime is $O(|S_h|^3)$. However if we use a look-up table to record segments (similar to the pin look-up table in section 3), the runtime can be greatly reduced.

5. The PSO-H Algorithm

To solve the PSO problem, we draw on the consistency graph G to maintain the order consistency. For convenience, for any two nodes A and B in G, if there is a path from A to B, we say A is B's parent, and B is A's child.

Each time, select the nodes which have no parent nodes, and move them to their highest available positions. These positions are their new locations. Then remove these nodes from the graph. Repeat this process until no nodes are left.

For each segment, its available position is decided by its FP-Range, allowable deviation bound, the distribution of power rails, fixed pins on M_5 and the positions of its parents. Let the wire separation requirement be $2s$. Suppose segment $A = (x_1, x_2, y, w)$ has a FP-Range $[V,U]$ and an allowable deviation bound d. If A moves in the range $[V,U] \cap [y-d, y+d]$, vertical wire separation, track consistency and P-constraint are satisfied according to Theorem 1. Obviously, the deviation bound is also satisfied. Also each node t records a value $Ubound$. $Ubound = min\{y_r - 2s - w_r | y_r$ is the y-coordinate of a t's parent node and w_r is its width $\}$. Thus if A moves in the range $[0, Ubound - w]$, the order consistency and horizontal signal wire separation are guaranteed. Let $[\bar{V},\bar{U}] = [V,U] \cap [y-d, y+d] \cap [0, Ubound - w]$. If no power rails fall in the rectangle region $(x_1 - 2s, \bar{U} - w - 2s, x_2 + 2s, \bar{U} + w + 2s)$, track $\bar{U}$ is the new position of the signal wire segment A. Otherwise, suppose a power rail segment $P = (x_{p1}, x_{p2}, y_p, w_p)$ has overlap with the rectangle region, let $\bar{U} = y_p - w_p - w - 2s$. Repeat the checking until a suitable position is found or $\bar{U} < \bar{V}$. The latter means no solution to the PSO problem. Further, since power rails are checked segment by segment, the shorts of two power rail segments have no effect on the calculation. For fixed pins on M_5, they are handled similar to power rails.

PSO-H Algorithm can be summarized as follows. S_h is the set of horizontal signal wire segments, P is the power rail set, R is the set of fixed pins, D records the allowable derivation bound for each segment. For each node t, its $Ubound$ is denoted as t.Ubound.

Algorithm PSO-H(S_h, P, R, D)
1. G = Consistency-Graph-Construction(S_h);
2. Calculate the FP-Range for each node;
3. Calculate [FP-Range] ∩ [allowable deviation];
4. Push all nodes without parent nodes into a List L;
5. For all nodes t in L , $t.Ubound = H$;
6.
7. While $L \neq \phi$ do
8. Remove a node q from L;
9. Calculate q's new position;
10. If no position is found, return "No Solution";
11. Update q's child nodes' $Ubound$;
12. Delete q from G;
13. Push the nodes without parent nodes into L;
14. end

In this algorithm, each time we always put a horizontal segment to its highest available position. This leaves more room for other segments since once one segment is processed, its location is fixed and other segments below it can not take the places above it. If we arbitrary assign a position in the available position, some segments may have no place to put.

In the calculation of available positions, FP-Range, deviation

bound and the distribution of power rails are decided by the problem itself. If no range satisfies these three constraints, no solution. On the other hand, if the problem has a solution, the position of each signal wire segment in this solution must fall in the range of the available position obtained in PSO-H since PSO-H always puts segments to their highest available positions, therefore PSO-H guarantees to find a solution as long as one exists.

To construct the consistency graph, it takes $O(|S_h|^3)$. The calculation of FP-Range may take $O(|R||S_h|)$. For the while loop, it has $|S_h|$ round. In each round, checking the intersection of power rails and fixed pins on M_5 may take $O(|P|+|R|)$. To update *Ubound*, each edge is visited only once for the whole loop. Since the number of edges is no more than $4|S_h|$, the runtime for PSO-H is $O(|S_h|^3 + |S_h||R| + 4|S_h||P| + 4|S_h||R|)$. Still, we can set up loop-up tables for pins, signal wire segments and power rails so that the searching time can be greatly reduced.

Theorem 2. *Given a PSO problem, PSO-H algorithm guarantees to find a feasible solution in polynomial time as long as one solution exists.*

6. PSO-G Algorithm

In Section 5, we propose an algorithm PSO-H to solve PSO problem. In that approach, all horizontal signal wire segments are put to their highest available positions. Surely for some segments, this is not necessary. And in many applications, we hope to make the changes as little as possible. So in this section, we propose another algorithm PSO-G which tries to reduce the total deviation. The "total deviation" is defined as the sum of the deviations of all horizontal segments. Also we define the node overlapped with power rails as Onode; if an Onode overlaps a power rail $\hat{P}$, and it has no parent nodes overlapped with $\hat{P}$, the node is called URnode; Similarly, if an Onode has no child nodes in the same power rail, the node is called DRnode. And a Rnode refers to either a URnode or a DRnode.

Figure 9: Illustration of Onodes/Rnodes. The shadow area is a power rail. All segments inside are Onodes. *A*, *B* and *D* have no parent nodes in this power rail. Thus *A*, *B* and *D* are URnodes. *F* and *D* have no child nodes in this power rail. They are DRnodes. A node can be both URnode and DRnode, like *D*.

Here are two observations:

1. Given a routing solution T, one solution T' is obtained by moving one Onode q outside power rail $\hat{P}$. To minimize the total deviation, the spacing between the new position of q and $\hat{P}$ must equal to the wire separation requirement.

2. Given a routing solution T, one solution T' is obtained by moving an Onode n_o which is not a Rnode outside power rails. Then there must be another solution T'' which is obtained by moving a Rnode outside power rails such that the total deviation of T'' is less than that of T'. This is because n_o has at least one parent and child in the same power rail. If n_o moves outside the power rail, it forces its parent/child nodes to move outside power rails in order to keep order consistency. Therefore, moving a n_o's parent/child node outside power rails leads to less total deviation. In Figure 9, the total deviation for moving the segment E must be larger than that for moving B or F.

Based on the two observations, we propose the PSO-G algorithm. In PSO-G, we need to search the graph in both directions(to parent nodes and to child nodes). To facilitate searching, another set of edges is added. If there is an edge (a,b) in G, add an edge (b,a). To separate the two sets of edges, assign a color "black" to the original edges and "white" to newly added edges. If a node searches for its parents, use white edges; if it searches for child nodes, use black edges.

First, we assign a cost to each Rnode r. Suppose r is a URnode. If r is moved outside the power rail, the new position of r may overlap with other segments or it is above its parents' position. Then the affected signal segments are forced to move up accordingly. The cost of a Rnode r is the total deviation caused by moving r outside power rails. Since r is a URnode, the affected segments can only be its parents. Let the node r be the starting point. Using BFS(Breath-first search) algorithm on white edges, we can identify all possible affected segments and mark them "red". Assume r is on power rail $\hat{P}$, then its new position is $y_p + w_p + w_r + 2s$ where y_p is the y-coordinate of the center of $\hat{P}$, w_p and w_r are the width of $\hat{P}$ and r respectively, and $2s$ is the wire separation requirement. If this position is still overlapped with an power rail $\tilde{P}$, test $y_{\tilde{P}} + w_{\tilde{P}} + w_r + 2s$. Repeat this process until no overlaps with power rails or the position is outside r's available position. r's available position is the intersection of r's FP-Range and its allowable deviation range. If no suitable position is found, set its cost ∞. Otherwise, go ahead to process the affected segments. The position of an affected segment is not calculated until all its red child nodes have calculated their new positions. Suppose an affected segment is $A = (x_1, x_2, y, w)$. Let $z = max\{y_c + w_c + 2s | y_c$ is the y-coordinate of a A's red child node and w_c is its width $\}$. If z is not a suitable position, use the above procedure until find an available position. If no suitable position is found, the cost is ∞. If all affected segments can find a position, the cost is the sum of the difference of their new positions and the old ones. The similar rule applies if r is a DRnode.

Each time, select one Rnode with the minimum cost, move it outside power rails and adjust the positions of affected segments if the minimum cost is not ∞. Once a Rnode is moved outside power rails, it is just an ordinary segment and it is not a Rnode any more. Further some of its child/parent Onodes may become a Rnode. For each Rnode, recalculate the cost and repeat this process until no Rnodes, i.e., no segments have overlap with power rails and the result is a solution to the PSO problem; or the minimum cost is ∞, i.e., no solution to the PSO problem. The algorithm is summarized as follows:

Algorithm PSO-G(S_h, P, R, D)
1. Construct consistency graph, mark Rnodes;
2. Calculate the FP-Range for each node;
3. Calculate [FP-Range] $\cap$ [allowable deviation];
4. Push all Rnodes into List and assign costs;
5.
6. while List $\neq \phi$ do
7. Select the Rnode r with the minimum cost;
8. If min-cost = ∞, return "No Solution";
9. Change positions of r and affected segments;
10. Push new Rnodes into List;
11. Adjust/assign costs to Rnodes in the List;
12. end

In the above procedure, the order consistency and horizontal wire separation are satisfied. Since all segments move within their FP-Range, no vertical wire separation or track consistency or P-constraint is violated according to theorem 1. Further, each segment is in its deviation bound and has no overlap with power rails. There-

Table 1: Average results of PSO-H and PSO-G for 5 times.

File		N3	S6	M8	F10
ECO Region Area(um^2)		4908.92x3295.52	3295.52x4908.92	10872.90x4799.54	4799.54x10872.90
Top layer Signal Segments		1601	2098	1266	726
Power Rail segments		166	1128	631	747
Overlapped Signal Segments		465	594	441	206
Allowable Deviation		2%	2%	2%	2%
Time (second)	PSO-H	5.62	9.17	3.81	3.26
	PSO-G	21.44	41.28	23.72	11.38
Max Deviation	PSO-H	1.987%	1.992%	1.991%	1.996%
	PSO-G	1.617%	0.231%	1.522%	0.944%
Total Deviation	PSO-H(um)	63029.58	126855.37	108874.92	120950.08
	PSO-G(um)	13097.40	1208.10	7066.87	4200.80
	PSO-G/PSO-H	20.780%	0.952%	6.491%	3.473%

fore, if PSO-G returns a solution, the solution is a correct one. On the other hand, if PSO-G can not find a solution, the PSO problem has no solution.

If a URnode u has a cost ∞, at least two parent nodes p_1 and p_2 of u are overlapped or their up/down order is disturbed. Suppose p_1 is above p_2 in the original design. Since p_1 can not move up further, it must have reached its highest possible position which is the intersection of FP-Range and allowable deviation bound excluding power rails. Also along the path from u to p_2, the spacing between two segments must be the required minimum spacing which is the sum of the widths of the two segments and 2s. Thus if the cost of a URnode is ∞, it can not be moved up outside power rails and this is totally decided by the problem itself instead of the processing method. Similarly, whether u can be moved down outside power rails is totally decided by the problem itself.

If PSO-G returns "No Solution", the minimum cost must be ∞. For any Rnode r left in List, there are two cases: 1) r is a URnode and DRnode, r can not be moved up or down outside power rails and it is decided by the problem itself. Therefore, no solution to PSO-problem. 2) r is a URnode and it has a child DRnode t. Both r and t have a cost of ∞ and can not be moved down outside power rails. Still the PSO problem has no solution. Thus if PSO-G algorithm can not find a solution, the PSO problem has no solution.

Suppose the number of segments overlapped with power rails is L. To construct the consistency graph and mark Rnodes, it takes $O(|S_h|^3+|S_h||P|)$. The calculation of FP-Range may take $O(|S_h||R|)$. To calculate the cost of one segment, each edge is visited at most twice(First for BFS, second for calculating the position) and it takes $O(|S_h||P|)$ since the edges of the consistency graph is at most $8|S_h|$ (including both black and white edges). Further, each Rnode can be in the List at most twice. Thus the while loop has at most $2L$ rounds, and each round can be finished in $O(L|P||S_h|)$ Thus the total runtime is $O(|S_h|^3+|S_h||R|+L^2|P||S_h|)$. By setting up look-up tables for pins, signal wire segments and power rails, the runtime can be greatly reduced.

Further, once a URnode(DRnode) is moved outside power rails, the segments affected can only be its parents(children). So if the cost calculation of a Rnode does not involve these segments, its cost will not be changed after the URnode(DRnode) moves out, i.e., no cost adjustment (Line 10) is needed for this node. Therefore, for each Rnode r, we record a bounding box $(x_{b1},y_{b1},x_{b2},y_{b2})$ where (x_{b1},y_{b1}) and (x_{b2},y_{b2}) are the coordinates of bottom left corner and up right corner. The bounding box covers all of the affected segments when r moves out. After one URnode/DRnode t is moved out, if the bounding box of a Rnode has no overlap with r's bounding box, the cost keeps the same and no need for calculation. In this way, a lot of calculation can be saved.

Theorem 3. *Given a PSO problem, PSO-H algorithm guarantees to find a feasible solution in polynomial time as long as one solution exists.*

7. Experimental Results

Our algorithms were implemented in C++ on PC(733MHz) with 128M memory. We tested PSO-H and PSO-G algorithms for four test files. These circuits were obtained from industry files and the top layer is for horizontal tracks. Both approaches were repeated 5 times. Table 1 lists the average results of these 5 trails. For all of the test circuits, we can find a clean routing solution and the derivation of each signal segment is bounded as 2% of the height of the ECO region area. For PSO-H algorithm, each top layer signal wire segment is moved only once. So it is much faster than PSO-G algorithm. If the requirement only wants a clean solution satisfying the deviation bound, PSO-H is preferred. But if no deviation bound is given or want to find a solution as close as possible to the original design, PSO-G algorithm always returns a solution with less total deviation and a smaller max-deviation.

8. Conclusion

In this paper, we have presented two polynomial-time algorithms to solve the overlaps between power rails and signal wires on the top layer as well as satisfying the allowable deviation bound, order consistency, track consistency, P-constraint and wire separation requirement. Both algorithms guarantee to find a feasible solution as long as one exists. One is faster, while the other makes effort to reduce total deviation. According to different application requirements, users can choose an appropriate one. Experimental results show the efficiency and effectiveness.

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