On the Interaction of Power Distribution Network with Substrate

Rajendran Panda, Savithri Sundareswaran, David Blaauw
Rajendran.Panda@motorola.com, Savithri_Sundareswaran-A12801@email.mot.com, David.Blaauw@motorola.com
Motorola, Inc., Austin, TX

ABSTRACT

In this paper, we investigate the interaction between a chip's power distribution network and its substrate to understand its impact on power supply noise and substrate-coupled noise. The study is set in the context of low-voltage, low-power, mixed signal chip designs based on low resistance, epitaxial process, substrate technology. We believe the findings of this study are significant to both the chip integration engineer and the analog circuit designer. We attempt here to answer two important questions: (1) To what extent can substrate modify the power supply noise, and what parameters of substrate design, if any, are salient? (2) What is the extent of coupling from the noisy digital power supply to the analog circuits through the substrate? We propose a method to simulate the power grid along with the substrate and present findings of case studies conducted on three low-power processor designs.

Keywords: substrate analysis, power grid analysis, substrate noise, substrate coupled noise

1. BACKGROUND

With continuing advances in process technology, on-chip power distribution network design has become a critical factor in the fabrication of microprocessors. Extensive work has focussed on analyzing the integrity of the supply voltage and on designing the power grid within voltage fluctuation specifications. The task of designing the power distribution network is especially challenging for low-power, mixed signal designs that operate at very low voltage and have a high noise sensitivity. Recently, several publications have focussed on constructing an accurate model of the on-chip power supply network, package model, and current consumption model for a design[1][2][3]. However, these models are limited in that they do not take into account the effect of the substrate on the power distribution network.

In modern VLSI designs, the substrate consists of either a lightly or highly doped P+ material. A number of digital designs use highly doped substrates to take advantage of their very low resistance (typically a few ohms per square). Low resistance substrates are used with a so-called epitaxial process where a thin, lightly doped layer resides on top of the highly doped substrate. Lightly doped substrates have a much higher resistance and have typically been favored for analog designs. In this paper, we consider only highly doped, low resistance substrates, such as those used in PowerPC^{tm} and Motorola DSP designs. However, the modeling approach presented here can be extended to highly resistive substrates as well, although the simulation results obtained will differ significantly.

ISLPED'01, August 6-7, 2001, Huntington Beach, California, USA.

The substrate is connected to the power supply network as shown schematically in Figure 1. The substrate-ties connect the ground distribution network to the substrate through ohmic contacts. The well-ties connect the VDD distribution network to the N-well. A parasitic capacitance at the junction between the N-well and the P substrate couples the N-well with the substrate. Current is injected into the substrate from the ground network through the substrate-ties or from the VDD network through the well-ties and the N-well/substrate junction capacitance. The source and drain junction capacitances can also inject current into the substrate. However, in the case of a low resistance substrate design, this current is negligible compared to the current injected from the power distribution network and can be ignored [4][5].

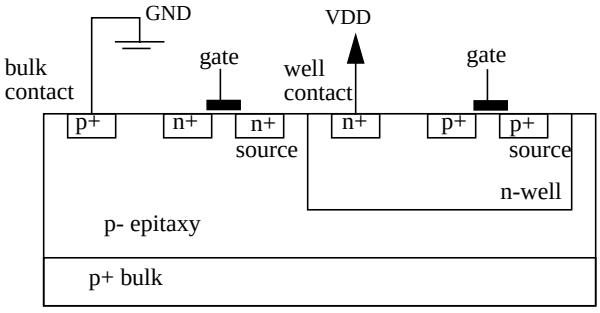

Figure 1. Low Resistance Epitaxial Substrate

The substrate impacts the power distribution network in two ways: First, the substrate provides an alternate path for the current to reach devices from the ground pads, and hence reduces the DC voltage drop of the ground distribution network. Second, the parasitic capacitance between the substrate and the N-wells act as decoupling capacitance between the power (VDD) and ground (GND) supply networks, and will reduce the AC voltage swings of both the VDD and GND supplies. The presence of the substrate therefore improves both the DC and AC voltage drop and, consequently, a power distribution analysis without modeling the substrate can lead to an over-designed distribution network and wasted chip resources.

As the substrate aids the integrity of the power distribution network, voltage fluctuations in the power distribution network also impact the integrity of voltages in the substrate. The current injected into the substrate from either the VDD or GND distribution networks causes the voltage of the substrate to vary both in time and in location on the die. This

voltage fluctuation results in a variation of the bulk to source voltage (Vbs) of the MOS devices which in turn results in a change of the threshold voltage in these devices. It is important to note that this threshold voltage fluctuation has both a temporal and spatial form. The threshold voltage fluctuation is sufficiently small to be negligible for the operation of digital circuits. However, it can have a significant impact on analog circuits that rely on accurately matched devices with identical threshold voltages. Therefore, in mixed signal designs, accurate simulation of the substrate voltage and analysis of the spatial and temporal behavior of this fluctuation is of critical importance.

In the past, much effort has been placed on the extraction of accurate substrate models[5,8-13]. A number of commercial solutions for extracting detailed substrate models are available [6-8]. These methods, however, do not include a detailed model of the power and ground distribution network. As such, they cannot model the impact of the substrate on power distribution integrity or the noise injected by power distribution into the substrate. More recently, a combined substrate and power grid model was introduced for low resistance substrates [5]. This model uses gate-level simulation to determine the current injected into the substrate due to gates switching. However, the VDD and GND networks are modeled as single nodes and, hence, the spatial variation of the substrate voltage cannot be obtained, nor can the impact the substrate has on the power distribution network integrity be calculated.

In this paper, we present a new analysis approach that combines detailed models of the power distribution network and the substrate. The power distribution network is represented with on-chip, package, and board level models. The substrate model consists of both a detailed extracted model for analog portions of the die and a simplified model for the digital portions of the design. Since the size of this combined power distribution and substrate model can be very large (50-100 Million elements for large designs), we propose a simulation approach based on waveform relaxation through iterative simulation of the different components until convergence.

Based on the proposed model and simulation approach we analyze three large designs, including one mixed signal design. We show how the substrate significantly improves the DC and AC voltage drop in their power distribution networks in these designs. Particularly, the voltage drop in the ground distribution networks is improved by the presence of the low impedance substrate. In some designs, this has lead to reallocation of metal routing resources from the ground distribution network to the VDD network. We also show how the proposed methods can effectively predict the noise in the analog sections of the substrate induced by noise in the distribution networks of the digital sections of a design.

Finally, we show that the placement of substrate ties is a critical factor in determining how the substrate impacts the integrity of the power distribution network, as well as the stability of the substrate voltage. We compare the substrate tie placement distribution of our three designs and show how their respective placement approaches impact the voltage stability in the power distribution network and substrate.

The remainder of this paper is organized as follows: Section 2 presents the models for the substrate, the on-chip and package power distribution networks, and the current consumption of the devices and also presents our simulation approach. Section 3 shows the impact that the low resistance substrate has on the power distribution network. Section 4 investigates the noise injected from the power distribution network into the substrate. In Section 5, we present our conclusions.

2. SUBSTRATE AND POWER GRID MODELS

In this section, we describe the electrical models used for simulating the substrate along with the chip's power distribution network. Originally, [1] proposed detailed models for the power distribution network in the chip and package, the switching currents, and the decoupling capacitance, and techniques for simulating the combined model. In this work, we adopt these models and extend them to include the substrate. The substrate model will be described in detail, and only a brief review of the power network, current, and decoupling capacitance models will be given.

2.1. Substrate

The substrate model that we use assumes an n-well process. However, the model is easily extensible to other processes, such as p-well process or the twin-tub processes. Figure 1 shows a cross section of the substrate. The substrate consists of a p- epitaxial layer and a low resistive p+ buried layer. The bulk is tied to the GND network through p+ bulk contacts. The n-well is likewise tied to the VDD network through the n+ well ties.

Noise is injected into the bulk by 3 mechanisms[4]: (1) resistive coupling, (2) capacitive coupling, and (3) impact ionization. Power supply noise in the GND network is injected into the bulk by the resistive coupling from bulk contacts to the bulk. Power supply noise in the VDD network couples resistively to the well through well ties which in turn couples to the bulk capacitive though the well barrier capacitance. The source and drain terminals of devices inject noise through capacitive coupling through the source/drain diffusion capacitance. Finally, impact ionization causes current flow from the pinch-off point of the NMOS channel to the bulk. Of these mechanisms, the impact ionization is the least significant in magnitude. The noise injected from power rails is much stronger than the noise from source/drain since power rails couple resistively to the

bulk/well and the well couples strongly to the bulk due to the large well capacitance. On the other hand, the source/drain couples to the bulk only through very small capacitances. Although the source/drain terminals can have voltage swings as large as the supply voltage, the amount of noise injected remains much smaller. For a comparison, the total diffusion capacitances of a chip is typically 5X smaller than the total well capacitance, and its admittance at the typical gate switching speeds is 100X smaller than the conductance between the bulk/well contact and the bulk/well. In view of this, our substrate noise model considers only the power supply noise injection.

Figure 2 shows the electrical model for the substrate. The p+ buried layer acts as a conducting plane and is modeled as a 2-D or 3-D mesh of resistors. The 2-D model is used for the digital circuit section of the substrate using a constant bulk profile. A more accurate 3-D model is used for the analog circuit section of the substrate using detailed substrate profile information at various depths. The lateral conduction through the highly resistive epitaxial is smaller than that of the p+ bulk by several orders of magnitude, and hence the effect of epitaxial is significant only as far as its vertical conduction from the bulk contacts to the p+ buried layer. Since the thickness of the epitaxial layer is much smaller in comparison to the distance between two adjacent bulk contacts, the effective resistance between two bulk contacts is dominated by the vertical resistances. As such, the epitaxial layer is modeled by vertical resistances between the bulk contacts and the bulk. The noise injected from source/drain terminals, as well as due to impact ionization, are ignored for the reasons discussed before, and the RC components corresponding to them are shown in dashed lines in Figure 2.

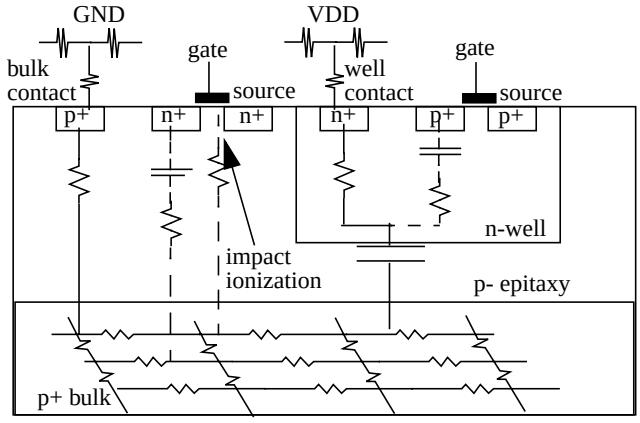

Figure 2. Electrical Model of the Substrate

A variety of techniques[9][10][11][12] and tools[6][7][8] are available to extract accurate RC models of substrates, and to further reduce the extracted models[13]. In this study, we constructed the 2-D resistive mesh of the bulk in the digital circuit section of the chip using the sheet resistance parameter of the bulk, and the vertical resistances of the ties using characteristic measurements of the process. Although one could alternatively use commercial extraction tools for this task, we have found our simpler model based on characteristic measurements of the bulk and well work adequately for estimating the noise injected by the digital section of the chip. For the analog circuit section of the substrate, however, we constructed a more accurate 3-D model using a commercial extraction tool.

2.2 Power network and substrate - combined model

The VDD and GND power networks on the chip are modeled as resistive networks using an accurate extraction tool. This network is then supplemented with distributed decoupling capacitances contributed by the devices, interconnects, and explicit decoupling structures. The intrinsic decoupling capacitance of the devices (when not switching) is estimated by SPICE simulation of the input impedance for representative circuit blocks set at random quiescent (stationary) states. The switching currents are modeled by a statistical distribution of triangular gate current pulses which together produce the specified total current profile at the input supply pins of the chip. An RLC model of the power supply system and package is also extracted from the board and package layouts using commercial extraction tools.

Figure 3 shows a simplified view of the complete model (power network and substrate) used in this work for simulation. The resulting network is an extremely large (10^6 - 10^8 nodes) linear network consisting of R,L, and C elements representing the power grid, package, and substrate modeling the power supply and independent, time-varying, current sources modeling the device switching currents.

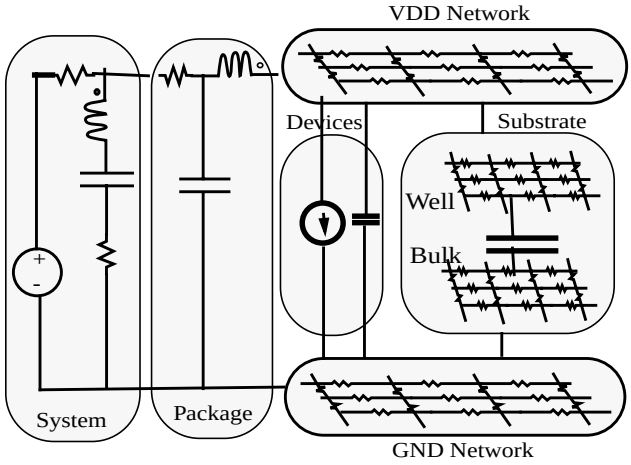

Figure 3. Simplified View of the Combined Model

3. SIMULATION METHODOLOGY

Several techniques were presented in [1] and [3] for efficient time domain simulation of very large RLC models such as the one shown in Figure 3. [1] extended the techniques for solving large RC power networks for the case when relatively few inductances (resulting from the package/board model) are included in the simulation. In this work, we use the techniques described in [1] and also introduce new techniques for addressing simulation requirements posed by the inclusion of the substrate in the model.

When analyzing very large power networks, it is customary to analyze the VDD and GND networks individually in order to limit the size of the network to be simulated. This approach causes some difficulty when a substrate is included in the simulation. Since the substrate couples to both the VDD and the GND networks (through bulk ties, well ties, and well capacitance), ideally one has to simulate the substrate and both power networks simultaneously. This is possible when the model is small as is the case for analog power network and substrate models for analog circuits. However, this is infeasible for simulating the digital section, given the limited memory/computing resources. We therefore propose an iterative approach in which the substrate will be simulated first with VDD and then with GND and this procedure is repeated until the voltages in the network converge. This approach is based on the waveform relaxation techniques [14]. This approach is used only for simulating the digital power supplies and the digital circuit sections of the substrate noise. The analog power supplies and analog circuit section of the substrate are simulated as a whole.

When simulating the VDD network with substrate, the noise in the GND network (obtained from the previous simulation) is injected at the bulk tie nodes. Likewise, the noise voltages at the well tie locations in the VDD network are injected at those nodes in the simulation of the GND network with the substrate. At the beginning of the iterative procedure, the noise from the other power rail is set to zero, and the iteration is terminated when the noise voltages do not change above a specified threshold. We observe that the iteration quickly converges in 1 or 2 iterations in all observed cases. The iterative simulation flow is shown in Figure 4.

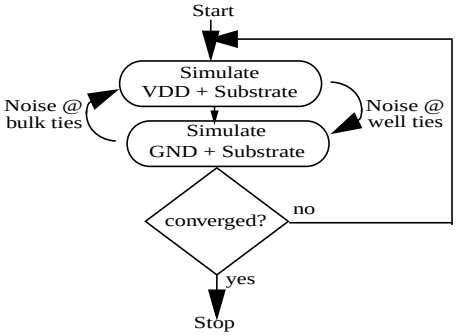

Figure 4. Iterative Simulation Procedure

4. SUBSTRATE EFFECT ON POWER SUPPLY NOISE

The proposed power distribution and substrate analysis approach was implemented and tested on three processor designs. Table 1 gives information on the number of nodes in the power network and the substrate, and the number of ties for each test case. The first two designs are low power communication processors and the third design is a mixed signal design. Table 2 compares the voltage drops in the power network with and without inclusion of the substrate. For the DC analysis (column 2 and 3), only the voltage drop in the ground network is reported, since the substrate has minimal impact on DC voltage drop in the VDD network. For AC analysis (column 4 and 5), a package RLC model was included in the simulation. The voltages shown are the maximum voltage fluctuation in time of a selected point in the VDD/GND network. The point that displayed worst DC drop was selected for tracking the AC voltage fluctuation. The results show that the substrate substantially improves

Chip	# Nodes VDD + GND grid	# Nodes Substrate	# Well Ties	# Bulk Ties
Chip-1	8.1M	0.7M	0.3M	0.2M
Chip-2	8.2M	0.3M	0.6M	1.3M
Chip-3 Digital	13.9M	0.3M	1.6M	0.6M
Chip-3 Analog	2.4M	0.06M	0.2M	0.5M

Table 1: Details of Test Cases

Design	Max DC Voltage Drop (mV)		Max AC Voltage Variation (mV)	
	Without Substrate	With Substrate	Without Substrate	With Substrate
Chip-1	155	131	220	37
Chip-2	333	91	300	100
Chip-3	102	20	119	23
Chip-3 Analog			51	24

Table 2: Power Supply Noise

the DC and AC voltage drops (15% - 80% for DC, and up to 83% for AC). In fact, some of these designs would have falsely appeared to fail their power distribution integrity requirements, if the analysis was performed without a substrate.

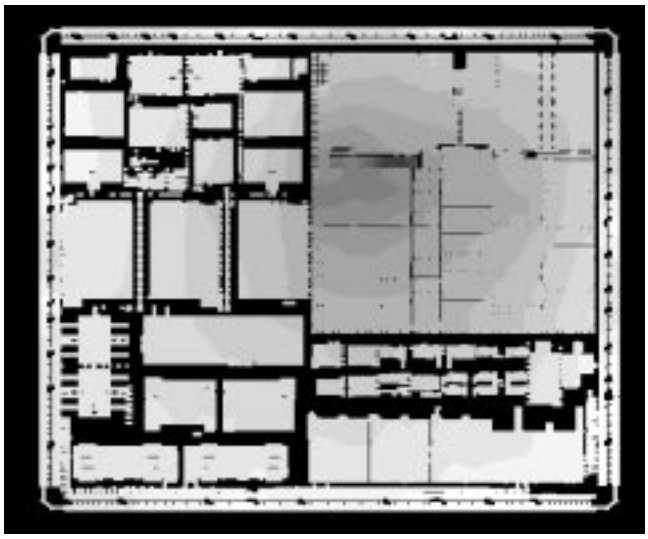

Figure 5. Voltage distribution in GND network for Chip-1 (without substrate)

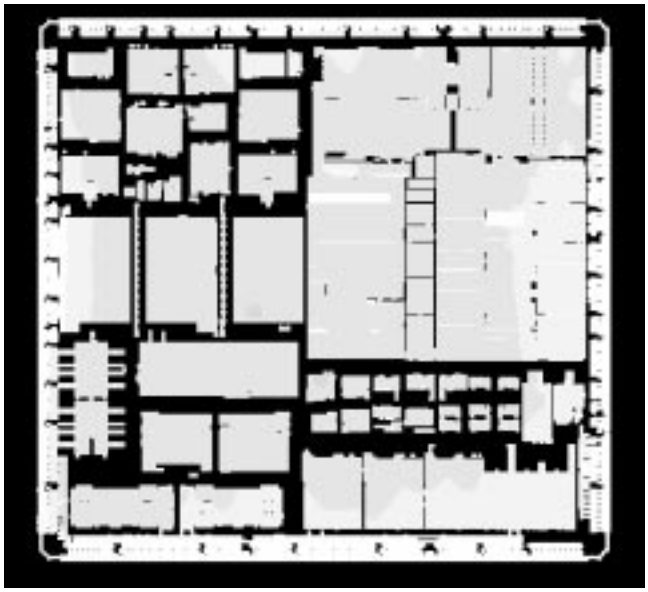

Figure 6.Voltage distribution in GND network for Chip-1 (with substrate)

Figures 5 and 6 show the voltage distribution in the GND network of one of the test cases at a typical time instance during AC simulation, both without and with the substrate respectively. In these pictures, a darker shade indicates a higher voltage drop. As expected, Figure 5 shows that the worst voltage drop occurs towards the center of the design. Figure 6 shows that the substrate substantially reduces this voltage drop and also creates a voltage drop that is relatively uniform across the die. This is particularly important for issues such as clock skew which rely on small spatial variation of the supply voltage.

5. SUBSTRATE COUPLED NOISE

The data given in this section pertains to the noise in the substrate nodes, and were obtained from the same simulations as for Section 4. Figure 7 shows the maximum temporal voltage variation (max. voltage - min. voltage) for all substrate nodes in Chip-1. The temporal variation data was collected over a simulation time period of 5 clock cycles. Table 3 shows the maximum temporal and spatial voltage variations for all three test cases. The temporal variation data correspond to voltages of a selected point, and likewise the spatial variation corresponds to a single time instance. The digital and analog portions of chip 3 are individually shown in Table 3. Although the temporal variation for Chip-3 is relatively small, the spatial variation is large, which could result in significant degradation in the quality of the analog circuit behavior.

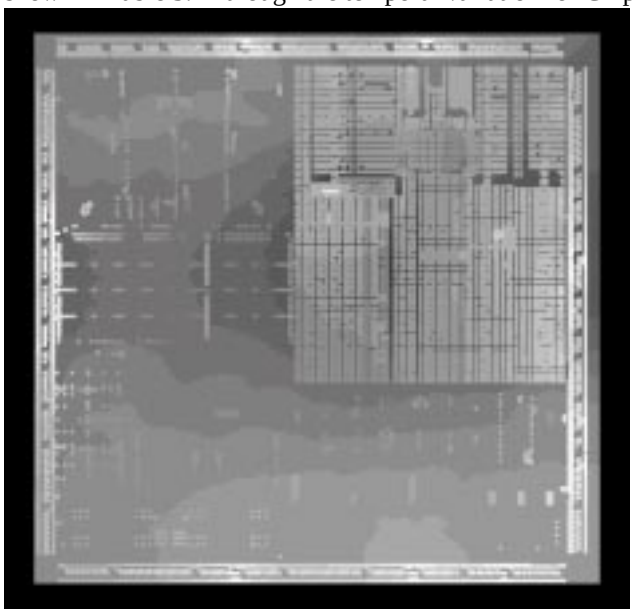

Figure 7. Maximum temporal voltage variation in substrate (for Chip-1)

Design	Max. Temporal Variation (mV)	Max. Spatial Variation (mV)
Chip-1	40.0	14.2
Chip-2	10.0	18.7
Chip-3 (Digital)	2.0	30.0
Chip-3 (Analog)	3.3	8.0

Table 3: Temporal and Spatial Noise in Substrate

It is interesting to note that temporal variation of the substrate for Chips 2 and 3 is significantly smaller than for Chip-1. Also, the improvement in the DC voltage drop due to inclusion of the substrate is significantly higher for these designs. This is caused by two factors. First, Chip 1 has significantly less substrate and well ties (Table 1). Therefore, the impedance between the substrate and power supply network is higher resulting in more substrate noise. However, the placement of the substrate ties is also significantly different between these designs. Figure 8 and 9 show the tie placement (shown as tie density per unit square) for Chips 1 and 3. These are the two cases that showed extreme values of temporal substrate voltage variation. Chip 3 has a high concentration of tie placements near the periphery of the design, which is close to the power supply pads. These ties will be very effective in maintaining good substrate voltage control. In Chip 1, the tie placement is more concentrated in the center of the design. Since these ties are far away from the power supply pads, they are not as effective in maintaining a constant substrate voltage. Therefore, not only the number of substrate ties, but also their placement plays an important role in the stability of both the power distribution network and the substrate.

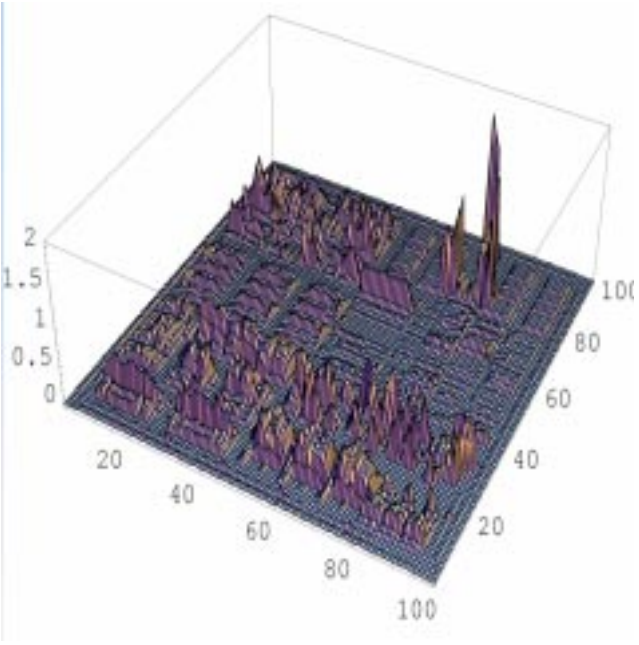

Figure 8. Tie placement for Chip-1

6. CONCLUSIONS

We presented a simulation methodology for studying the interaction of the power supply network and the substrate. The simulation results demonstrate our claim that the effect of substrate needs to be considered to estimate power supply noise more realistically and thus to avoid over-designing the power distribution network. The proposed methodology also enables estimation of noise in the substrate, a parameter

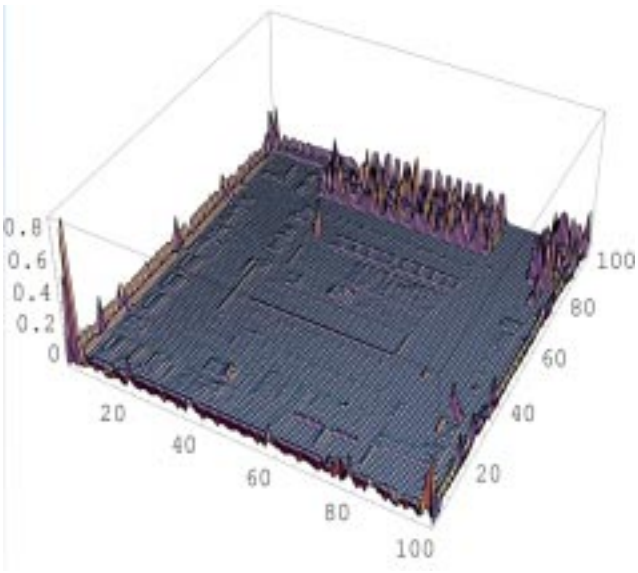

Figure 9. Tie placement for Chip-3

that is especially crucial in mixed signal designs. The study also explored the relation between the placement of the substrate ties and the amount of substrate noise.

References

[1] Rajendran Panda, et. al., Model and Analysis for Combined Package and On-chip Power Grid Simulation, Intl. Symposium on Low Power Electronics and Design, 2000, pp.179-184.

[2] Howard H. Chen, et. al., "Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design", 34th Design Automation Conference, 1997, pp.638-643.

[3] Abhijit Dharchoudhyry, et. al., "Design and Analysis of Power Distribution Networks in PowerPC Microprocessors", 35th Design Automation Conference, 1998, pp.738-743.

[4] Matt Felder, et.al., "Analysis of ground bounce induced substrate noise coupling in a low resistive bulk epitaxial process: Design strategies to minimize noise effects on a mixed signal chip", IEEE Trans. on Circuits and Systems, Nov. 99, pp.1427-1436.

[5] Marc van Heijningen, et. al., High-Level Simulation of Substrate Noise Generation Including Power Supply Noise Coupling, DAC 2000, pp.446-451.

[6] Layin, SnakeTech/Simplex Inc.

[7] Seismic, CadMos Design Technologies (now, Cadence Inc.).

[8] A.J. van Genderen, et. al., SPACE Substrate Resistance Extraction User's Manual, Dept. Elec. Engg., Delft University of Technology, Report ET-NS 96-03, June 1999.

[9] Mike Chou, et. al., "Multilevel Integral Equation Methods for the Extraction of Substrate Coupling Parameters in Mixed-Signal ICs", DAC 1998, pp.20-25.

[10] Edoardo Charbon, et. al., "Semi-Analytical Techniques for Substrate Characterization in the Design of Mixed-Signal ICs", ICCAD 1996, pp.455-462.

[11] Nishath K. Verghese, et. al., SUBTRACT: A Program for the Efficient Evaluation of Substrate Parasitics in Integrated Circuits, ICCAD 1995, pp. 194-198.

[12] T. Smedes, et. al., "Extraction of Circuit Models for Substrate Cross-talk", ICCAD 1995, pp. 199-206.

[13] Kevin J. Kerns, et. al., "Stable and Efficient Reduction of Substrate Model Networks Using Congruence Transforms", ICCAD 1995, pp. 207-214.

[14] Lawrence T. Pillage, Ronald A. Rohrer and Chandramouli Visweswariah, "Electronic Circut and system simulation methods", McGraw Hill publications, 1995.