Optimizing Bias-circuit Design of Cascode Operational Amplifier for Wide Dynamic Range Operations

Takeshi Fukumoto Hiroyuki Okada* Kazuyuki Nakamura

Silicon Systems Research Laboratories, NEC Corporation
1120 Shimokuzawa, Sagamihara, Kanagawa, 229-1198 Japan

{fukumoto,h-okada,nakamura}@mel.cl.nec.co.jp

ABSTRACT

Proposed here is a bias circuit for use in a cascode operational amplifier to provide a wide output dynamic range. The bias circuit has been designed so that the drain-source voltage of each MOS transistor used in the gain stage is minimized to V_{dsat} automatically, making it possible to widen the output dynamic range.

Keywords

Amplifier, CMOS, Analog, Low voltage, Dynamic range, Cascode, Bias-circuit.

1. INTRODUCTION

Analog LSIs have recently come to be designed with lower voltage supplies for decreased power consumption, but the analog CMOS circuits they employ tend to encounter a number of problems at these lower voltages. One of the most serious problems is reduced output dynamic range, which results in decreased S/N ratio.

Figure 1(a) shows a conventional output N-channel cascode current mirror, and Figure 1(b) shows the cascode amplifier in which it is used. The output dynamic range here is mainly limited by the gate voltage of M14 (VBIAS1). If VBIAS1 is set too high, the lowest output voltage will not be a theoretical minimum value, and if, as a correction, VBIAS1 is set too low, transistors M16 and M17 will operate in a linear domain and the cascode operational amplifier will not work. While a number of operational amplifiers with improved output dynamic ranges have been developed [1]-[6], none of the reports concerning these conventional amplifiers describes a voltage bias circuit, and it is impossible to verify whether or not any of them achieves a minimum output voltage.

This work presents an automatically optimized voltage bias circuit for an operational amplifier. Section 2 describes the structure of an operational amplifier designed to achieve maximum output dynamic range with the proposed bias circuit, and it also describes the method used for the maximization. Section 3 presents an evaluation of the design: we simulate and measure the performance of an operational amplifier of the proposed design that has a 2.5V source voltage and has been fabricated with 0.25μm CMOS technology. The minimum output voltage achieved is 0.3V. These results appear theoretically sound, since V_{dsat} of the N-channel transistor is 0.15V.

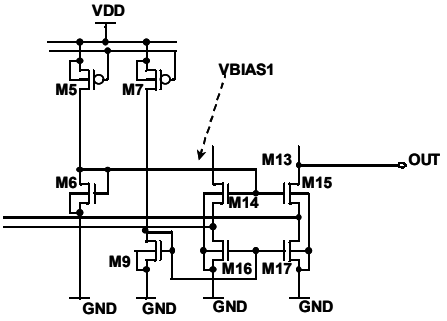

Figure 1(a): Conventional N-channel cascode current mirror

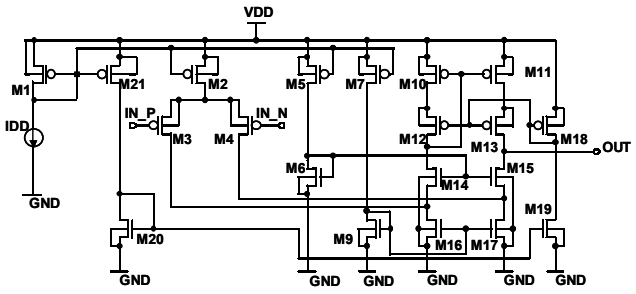

Figure 1(b): Conventional cascode operational amplifier employing mirror

ISLPED '01, August 6-7, 2001, Huntington Beach, California, USA.

*Presently with Semiconductor Technology Academic Research Center (STARC).

2. DESIGN OF A WIDE DYNAMIC RANGE OPERATIONAL AMPLIFIER

The output dynamic range of an operational amplifier is mainly determined in the gain stage. Figure 2(a) shows a proposed wide-swing cascode current mirror containing the voltage bias circuit. Figure 2(b) shows a proposed amplifier circuit employing the mirror. The circuit generates an optimum voltage bias to minimize the voltage differences generated by the internal mirrors. These functions have maximum output dynamic range. In order to minimize the voltage differences, each gate voltage is set so that each drain-source voltage will equal V_{dsat}, which represents the minimum drain-source voltage necessary for a MOS transistor to operate in a saturation domain. The letters a, b, c, and d shown in Figure 2(b) beside their respective current sources represent real constants that express individual current ratios with respect to reference current I.

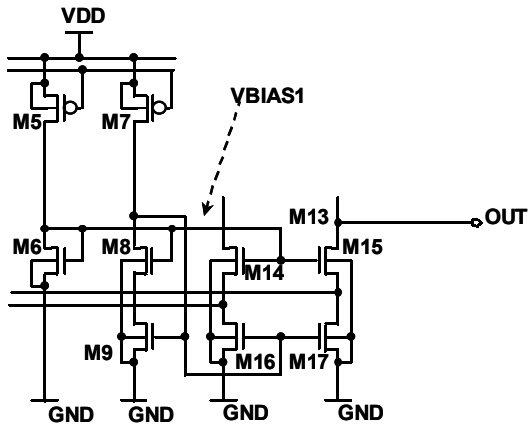

Figure 2(a): N-channel cascode current mirror for proposed operational amplifier

Gate length L and threshold voltage V_{th}, are assumed to be the same for each transistor. Since the respective gate voltages of M9, M16, and M17 are the same, i.e.

$$V_{GS9} = V_{GS16} = V_{GS17},$$

then

$$V_{dsat9} + V_{th} = V_{dsat16} + V_{th} = V_{dsat17} + V_{th}. \quad (1)$$

Further, from the relationship between M6, M8, and M9,

$$V_{DS9} = V_{GS6} - V_{GS8}$$

and

$$V_{dsat9} = (V_{dsat6} + V_{th}) - (V_{dsat8} + V_{th}). \quad (2)$$

In the same way,

$$V_{DS16} = V_{GS6} - V_{GS14}$$

and

$$V_{dsat16} = (V_{dsat6} + V_{th}) - (V_{dsat14} + V_{th}) \quad (3)$$

Then

$$V_{dsatn} = \sqrt{\frac{2I_{dn}}{\mu C_{OX} W/L}} \quad (4)$$

In Equation (4), suffix *n* denotes the number of MOS transistors in Figure 2(b). Equation (4) can be substituted into Equations (1) - (3).

In order to determine the V_{ds} for M16 and M17, it is necessary to take into consideration the current flow from M3 and M4. For example, when V_{dsat16} is at its maximum value, i.e., when aI is flowing through M16, the current from M3 will be maximum. If M16 operates in a saturation domain under these conditions, it will operate in a saturation domain no matter what the current from M3 is. Further, Equation (3) it was assumed that M6 would operate on the boundary of a saturation domain and a linear domain. In order to guarantee that it will operate in a saturation domain, taking into consideration process variations etc., the value of V_{ds16} has been set slightly greater than V_{dsat16}. If Equations (1) - (4) are adjusted in consideration of these conditions, they will reflect the conditions under which each N-channel transistor in the current mirror will operate in a saturation domain, and under which the smallest potential difference will be achieved.

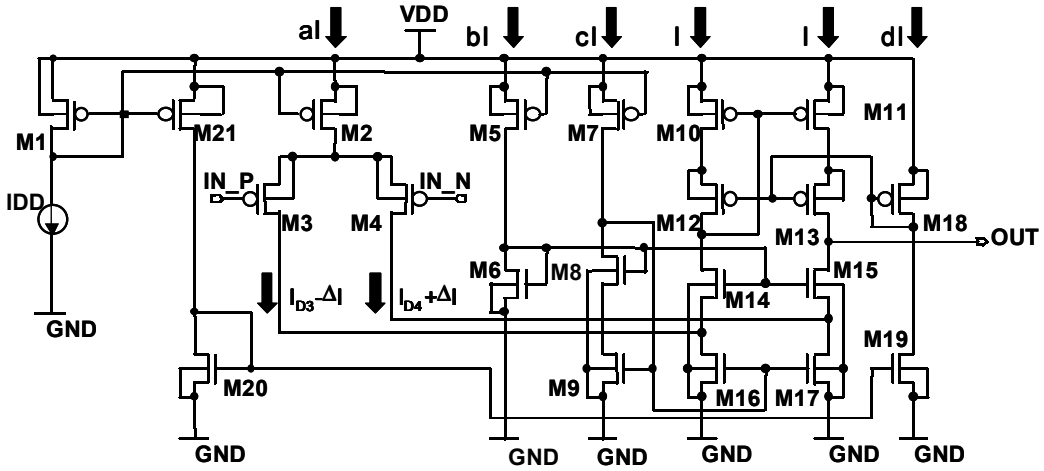

Figure 2(b): Proposed circuit of operational amplifier

Thus,

$$W_9 = \frac{c}{1+a} W_{16} = \frac{c}{1+a} W_{17} \quad (1')$$

$$\sqrt{\frac{b}{W_6}} \geq \sqrt{\frac{c}{W_8}} + \sqrt{\frac{c}{W_9}} \quad (2')$$

$$\sqrt{\frac{b}{W_6}} \geq \sqrt{\frac{1}{W_{14}}} + \sqrt{\frac{1+a}{W_{16}}} . \quad (3')$$

Equations (1') - (3') can be transformed into

$$\sqrt{\frac{b}{W_6}} - \sqrt{\frac{c}{W_8}} \geq \sqrt{\frac{1+a}{W_{16}}} \quad (5)$$

$$W_8 \leq cW_{14}. \quad (6)$$

By performing these same operations for the P-channel current mirror, we obtain the following equation, which represents a wide-swing cascode current mirror:

$$W_{10} : W_{11} : W_{12} : W_{13} : W_{18}$$
$$= 1 : 1 : 1/k^2 : 1/k^2 : 1/(k+1)^2, \quad (7)$$

where k represents an arbitrary positive number. With these equations it is possible, by determining parameters W_n, a, b, c, and d, to design an operational amplifier having maximum output dynamic range. The minimum output voltage will be $2V_{dsat}$. In addition, by having two cascode current mirrors, upper and lower, in the gain stage, this design achieves high output load resistance.

3. SIMULATION AND MEASUREMENT RESULTS

3.1 Simulation results

To evaluate the proposed circuit, an operational amplifier was designed and then simulated in SPICE. Table 1 shows individual MOS transistor gate sizes. Simulation conditions were a 2.5V supply voltage and 0.25μm CMOS technology. In SPICE simulations, the operational amplifier was operated with a voltage follower circuit.

Figure 3 shows DC analysis results for the proposed design. The minimum output voltage was 0.3V. These results appear theoretically sound, since V_{dsat} of the N-channel transistor was 0.15V.

Figure 4 shows the lowest output voltages of the proposed and conventional circuits while Figure 5 shows their output dynamic ranges. Here input / output voltage error was less than 1%. The base value for VBIAS1 was determined in accord with the operating voltage of the proposed circuit. Figure 4 shows the clear superior its of the proposed design with respect to output dynamic range. In Figure 5, the conventional circuit slightly exceeds the proposed circuit in output dynamic range because in our design we have added a margin for M6 in a saturation domain.

Total power consumption was 1.83mW with 4.1pF load capacitance C_L.

3.2 Measurement results

Figure 6 shows measurement results for triangular pulse input. Input conditions were 2.5V amplitude, 500μs rise (=fall) time. The minimum output voltage was about 0.3V. The results in Figure 6 agree well with the simulation results shown in Figure 4.

Table 1 MOS transistor gate sizes

(L=0.24μm for M3, M4, L=1μm for other Tr.)

Tr.	W[μm]	Tr.	W[μm]
M1	32	M11	200
M2	800	M12	200
M3	800	M13	200
M4	800	M14	260
M5	8	M15	260
M6	1	M16	200
M7	8	M17	200
M8	5	M18	1
M9	3.27	M19	8
M10	200	M20	32
		M21	32

Figure 7 shows the layout of the proposed operational amplifier.

4. SUMMARY

A novel circuit design has been proposed here for use in a cascode operational amplifier in which importance has been given to maximizing the output dynamic range. SPICE simulations show that when the proposed circuit is used in a cascode operational amplifier, the minimum output voltage is 0.3V, and a maximum output dynamic range is achieved.

5. ACKNOWLEDGMENTS

The authors gratefully acknowledge the important support given to our work by Dr. M. Fujiwara, Dr. K. Kurata, T. Yoshikawa, I. Hatakeyama, Dr. M. Fukuma, Dr. M. Yamashina, Y. Hirota, Y. Nakazawa and S. Hattori.

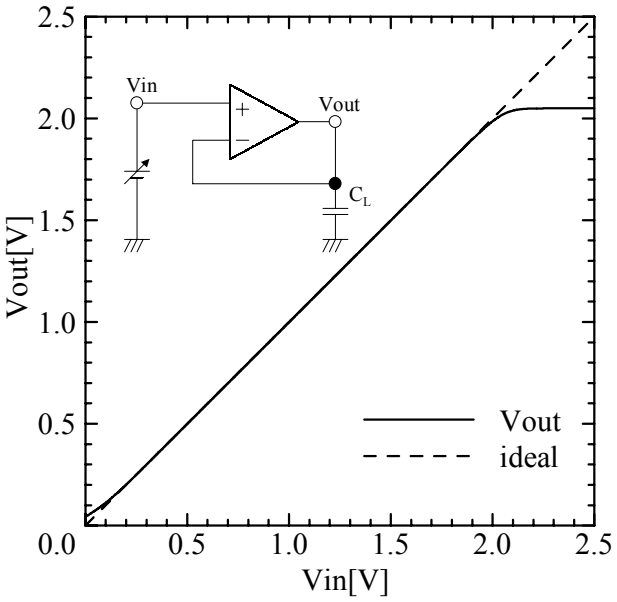

Figure 3: DC analysis results

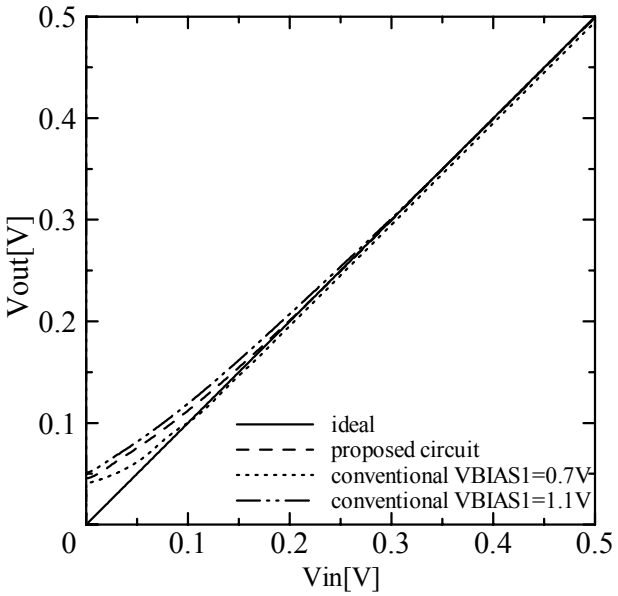

Figure 4: Lowest output dynamic ranges with VBIAS1 as a variable parameter

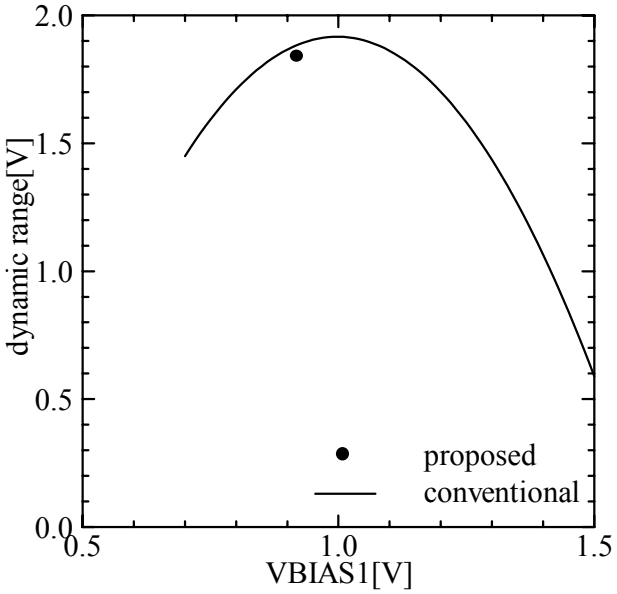

Figure 5: Output dynamic ranges with VBIAS1 as a variable parameter

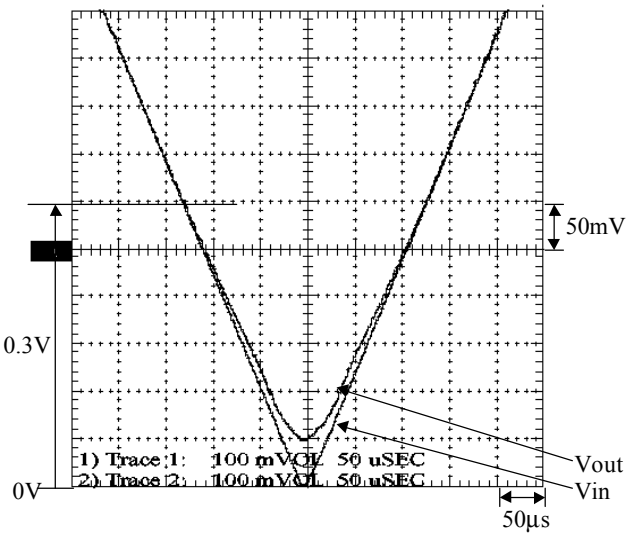

Figure 6: Measurement results for triangular pulse input

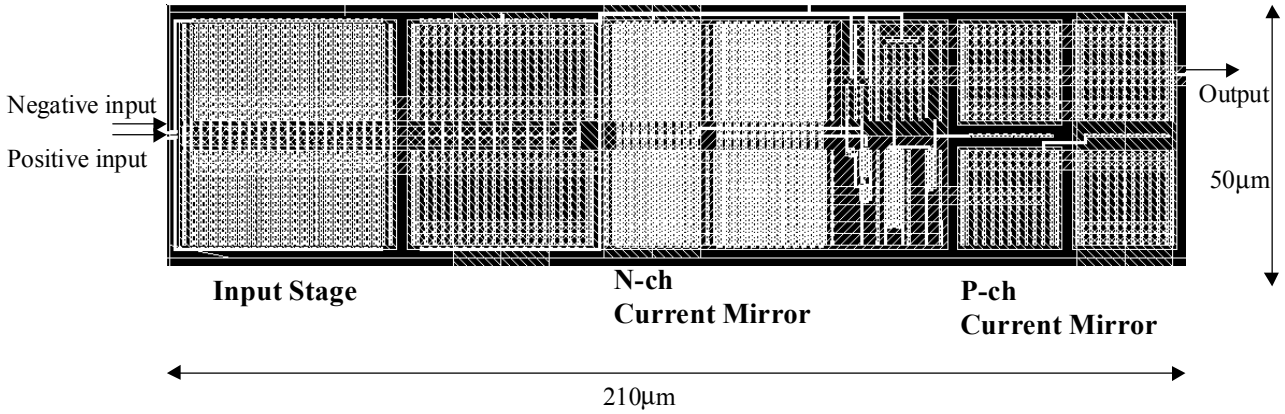

Figure 7: Layout of proposed amplifier

6. REFERENCES

[1] J. F. Duque-Carrillo, J. L. Ausin, G. Torelli, J. M. Valverde, and M. A. Domínguez, "1-V rail-to-rail operational amplifiers in standard CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp.33-44, Jan. 2000.

[2] S. Yan, and E. Sánchez-Sinencio, "A programmable rail-to-rail constant-G_M input structure for LV amplifier," *IEEE ISCAS 2000*, vol. 5, pp.645-648, May 2000.

[3] G. Ferri, A. Costa and A. Baschirotto, "A 1.2 V rail-to-rail switched buffer," *IEEE ICECS '98*, vol. 1, pp.45-48, 1998.

[4] . Ramírez-Angulo, A. Torralba, R. G. Carvajal, and J. Tombs, "Low-voltage CMOS operational amplifiers with wide input-output swing based on a novel scheme," *IEEE Trans. Circuit and Systems-I*, vol. 47, no. 5, pp.772-774, May 2000.

[5] J. Ramírez-Angulo, A. Torralba, R. G. Carvajal, and J. Tombs, "Simple technique for opamp continuous-time 1V supply operation," *Electron Lett.*, vol. 35, no. 4, pp.263-264, Feb. 1999.

[6] D. Schmitt and T. S. Fiez, "A low voltage CMOS current source," *IEEE Proc. ISLPED '97*, vol. 3, pp.13445-1349, 1997.