A Low-Power, 5-70MHz, 7th-Order Filter with Programmable Boost, Group Delay, and Gain Using Instantaneous Companding

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ABSTRACT

A seventh-order 0.05° equiripple linear-phase continuous-time filter employing, for the first time, instantaneous companding, was designed and integrated in a mature bipolar process. The amount of boost (up to 13dB) and group-delay adjustment (30%) are digitally programmable. The DC gain is controllable up to 10dB, and the -3dB frequency (f_c) is tunable from 5 to 70MHz. The output swing for 1% THD is higher than 100mV$_{pp}$, with a 1.5V supply. The filter consumes very low power (5-13mW for f_c= 70MHz) compared to conventional implementations (e.g. 120mW for f_c= 100MHz [1]).

1. INTRODUCTION

The continuous decrease of the supply voltages of modern integrated circuit technologies often necessitates an increase in the power consumption of conventional analog circuit processors, in order to maintain the same Dynamic Range (DR) and chip area for a given bandwidth [2]. To mitigate this restriction, the use of companding-based signal processors was proposed [3]-[4]. The last ten years have seen a growing interest in employing companding for continuous-time filtering. This was paralleled by the design and fabrication of several integrated log-domain filter circuits in a variety of technologies (e.g. [5]-[11]). These implementations were mostly low-order filters for proof of concept and / or performance exploration; they did not target particular applications or specifications. In order to gain industrial acceptance, the performance of companding-based filters needs to match, if not exceed, the performance of conventional filtering schemes, and should be evaluated in the context of concrete applications. Recently, a micropower log-domain filter for the Digital European Cordless Telephone (DECT) standard was reported [10].

Hard-disk-drive (HDD) read channels is another application where the requirements on filtering is constantly on the rise in terms of power consumption, tunability, speed, and robustness [12]. The objective of the work presented in this paper is to design a companding-based prefilter for HDD applications which exceeds state-of-the-art bipolar/BiCMOS designs in terms of voltage supply and power consumption (5mW without boost and equalization for f_c = 70MHz versus 120mW for f_c = 100MHz in [1]), while satisfying the requirements of partial response maximum likelihood (PRML) read channel front-ends. In servo mode, the filter has a cutoff frequency as low as 5MHz and dissipates less than 500µW.

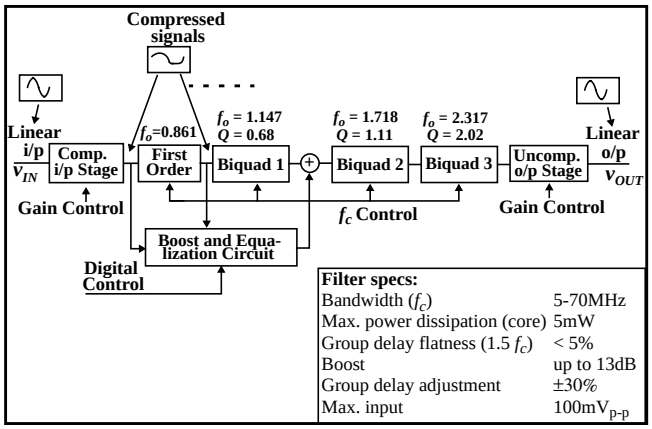

Fig. 1. 7th-order companding-based filter block diagram.

Figure 1 shows the overall structure of the 7th-order filter presented in this paper, along with a summary of the system specifications (details in Section 5). The input signal is compressed before being processed, which ensures signal integrity over a large range of signal levels. At the output, the signal is expanded to restore its DR. When the compression / uncompression are logarithmic / exponential, the resulting filter is known as a "log-domain filter" [13].

2. CONCEPT OF LOG-DOMAIN FILTERING

The concept of log-domain filtering is illustrated in Fig. 2 (a) for a simple first-order filter. The input signal v_{IN}, in voltage format, is first converted to a current signal i_I by a voltage-to-current converter (V / I). In its simplest implementation, this V / I can be a linear resistor R, resulting in an input linear current signal $i_I = v_{IN} / R$. This current signal is then logarithmically compressed using a LOG pre-processor. This can be practically achieved by pushing i_I into the collector of a bipolar transistor with a grounded emitter terminal. The compressed signal will appear at the base of the transistor in voltage format, and is given by[1]:

$$\hat{v}_I = V_T \ln\frac{i_I}{I_S} = V_T \ln\frac{(v_{IN}/R)}{I_S}, \qquad (1)$$

1. We will use the hat symbol (^) to denote nonlinear (log-domain) compressed voltage signals.

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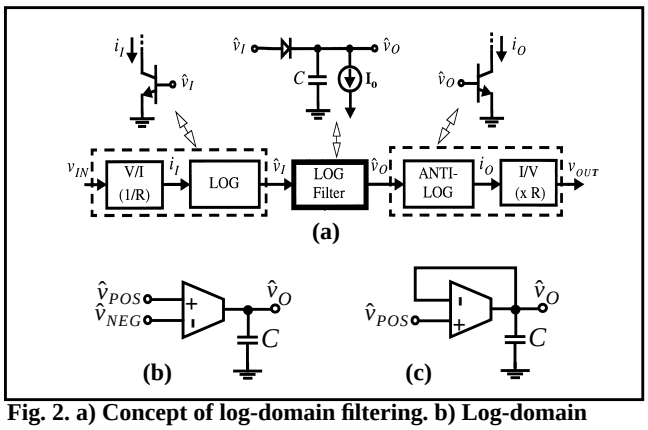

Fig. 2. a) Concept of log-domain filtering. b) Log-domain integrator symbol. c) Damped integrator symbol.

where V_T denotes the thermal voltage, and I_S is the bipolar saturation current. This signal is then applied to a nonlinear signal processor block denoted by the "LOG filter". The characteristics of this LOG filter will be discussed shortly. At this point, we will assume that the LOG filter can be designed such that the output nonlinear signal $\hat{v}_O$ will be some form of a filtered version of $\hat{v}_I$ and that, when logarithmically uncompressed, it will result in a perfectly linear signal i_O. This uncompression is performed by the ANTI-LOG post-processor. Practically, it can be achieved by applying $\hat{v}_O$ to the base of a bipolar transistor with a grounded emitter terminal. The current i_O will be the collector current of the bipolar transistor, and is given by

$$i_O = I_S e^{\hat{v}_O / V_T}. \quad (2)$$

In many cases, it will be necessary to convert the output current i_O to a voltage signal, for example for measurement purposes, using a current-to-voltage converter (*I/V*). The latter can be a linear resistor *R*, resulting in an output voltage signal $v_{OUT} = R\, i_O$. In order to maintain an overall linear input(i_I)-output(i_O) transfer function, the large-signal behavior of the "LOG filter" needs to satisfy very specific requirements.

For simplicity, we will consider a first-order LOG filter example. As for conventional filters, it would consist of one integrator block (Fig. 2(b)). This integrator, known as a log-domain integrator, has positive and negative inputs ($\hat{v}_{POS}$, $\hat{v}_{NEG}$), and a single-ended output ($\hat{v}_O$) connected to an integrating capacitor *C*. In order to ensure an overall linear input-output filter transfer function, it has been shown in earlier publications ([7], [9]) that the large-signal behavior of such an integrator should satisfy an equation, relating its input and output voltages to the current ($C\,(d\hat{v}_O/dt)$) flowing in the integrating capacitor, of the following format

$$C\frac{d\hat{v}_O}{dt} = I_o \cdot e^{(\hat{v}_{POS}-\hat{v}_O)/V_T} - I_o \cdot e^{(\hat{v}_{NEG}-\hat{v}_O)/V_T}. \quad (3)$$

As in conventional filters, in order to implement a first-order system, the output voltage is fed back to the negative input terminal ($\hat{v}_{NEG} = \hat{v}_O$), resulting in a damped integrator (Fig. 2(c)). Equation (3) will therefore be reduced to

$$C\frac{d\hat{v}_O}{dt} = I_o \cdot e^{(\hat{v}_{POS}-\hat{v}_O)/V_T} - I_o. \quad (4)$$

A simple circuit that realizes a transfer function of the same format as (4) is the "diode-capacitor-current source" shown in Fig. 2(a). With ($\hat{v}_{POS} = \hat{v}_I$), the current flowing into the capacitor of Fig. 2(a) is given by

$$C\frac{d\hat{v}_O}{dt} = I_S \cdot e^{(\hat{v}_I-\hat{v}_O)/V_T} - I_o. \quad (5)$$

Multiplying through by $e^{\hat{v}_O/V_T}$, using the chain rule, and rearranging, equation (5) can be written as

$$e^{\hat{v}_I/V_T} = \frac{V_T}{I_S}\left(C\frac{d}{dt}e^{\hat{v}_O/V_T}\right) + \frac{I_o}{I_S}e^{\hat{v}_O/V_T}. \quad (6)$$

From (1) and (2) we have ($e^{\hat{v}_I/V_T} = i_I/I_S$) and ($e^{\hat{v}_O/V_T} = i_O/I_S$). Substituting in (6) results in

$$i_I = \frac{V_T}{I_S}C\frac{d}{dt}i_O + \frac{I_o}{I_S}i_O, \quad (7)$$

which describes a linear input-output first-order filter with a tunable cutoff frequency proportional to I_o.

Higher order filters can be synthesized using a state-space based approach [13], or the less component-sensitive LC-ladder based approach [8], as long as the transfer function of the log-domain integrator used has a general format similar to (3).

3. THE INTEGRATOR

The class-AB log-domain integrator used to implement the 7th-order companding-based filter of Fig. 1 is shown in Fig. 3 [5]-[6]. This integrator structure was chosen among others due to the fact that, in addition to its low-voltage and high-frequency potential, it features immunity to crosstalk thanks to its differential structure. Rejection of common-mode interference becomes a critical issue as operating speeds increase [14].

Writing a loop equation around L1, the current in Q_2 is given by $i_{Q2} = I_o e^{(\hat{v}_{INP}-\hat{v}_{OUTP})/V_T}$. Transistors Q_3 and Q_4 are biased at a constant current I_o. Any large AC signal appearing at node $\hat{v}_{OUTP}$ will be copied to the base of Q_3 then duplicated at node P1 by Q_4. Therefore, transistors Q_3-Q_4 form a low-voltage buffer. Since Q_{10} is also biased at a constant current I_o, the AC voltage at its base will follow $\hat{v}_{INN}$. The AC base-emitter voltage of Q_6 is therefore given by $\hat{v}_{INN} - \hat{v}_{P1} = \hat{v}_{INN} - \hat{v}_{OUTP}$, resulting in a total current

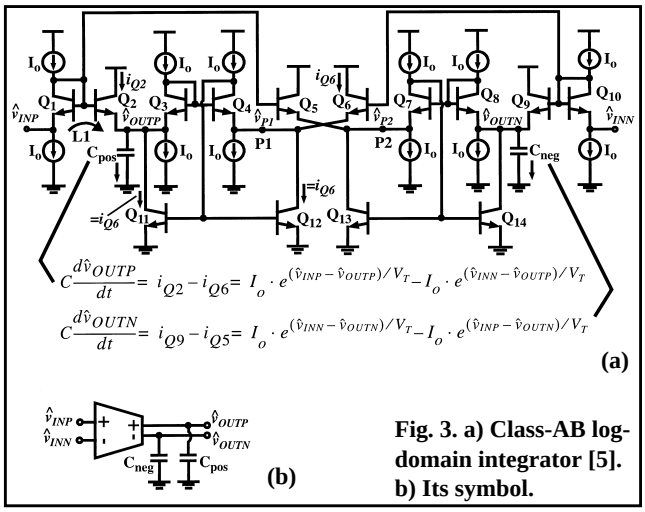

Fig. 3. a) Class-AB log-domain integrator [5]. b) Its symbol.

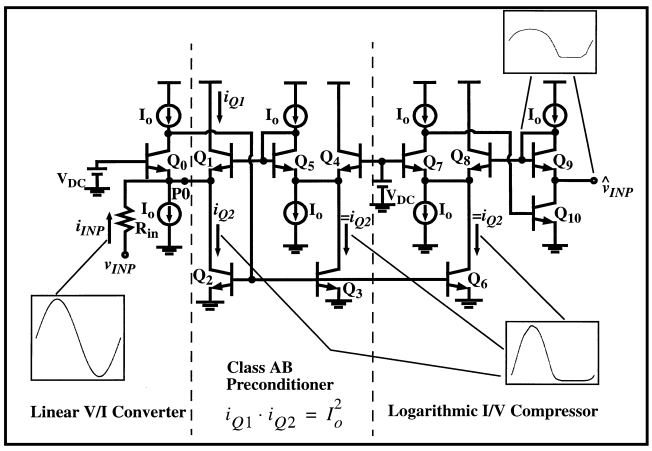

Fig. 4. One half of the input stage.

$i_{Q6} = I_o e^{(\hat{v}_{INN} - \hat{v}_{OUTP})/V_T}$ flowing in Q_6, in Q_{12}, and subsequently in Q_{11}. The current flowing in capacitor C_{pos} is given by $i_{Cpos} = i_{Q2} - i_{Q11} = i_{Q2} - i_{Q6}$. This results in an expression for i_{Cpos} of the same format as equation (3). A similar expression can be obtained for the current in C_{neg} (Fig. 3). Constant current sources (I_o/β) were used to compensate for the finite betas (β) of the transistors, in order to increase the integrator gain and reduce distortion.

4. THE INPUT AND OUTPUT INTERFACE CIRCUITRY

The currents in transistors Q_2 and Q_6, as well as in Q_9 and Q_5 in Fig. 3, are restricted to positive values. In order to benefit from class AB operation, the differential input voltages need to be split into two strictly positive signals. A "constant-product" preprocessing input stage was chosen to perform this operation in order to minimize the distortion that a simple rectifier would introduce, especially for high-frequency signals. Figure 4 shows the details of the input preprocessing stage. Transistor Q_0 is biased at a constant current and has a fixed base voltage; this makes the node P0 at its emitter behave as an AC virtual ground. The V/I conversion is simply performed by a resistor R_{in} connected to P0. This V/I converter is a modified version of the CMOS I/I converter discussed in [15]. Analysis of the feedback loop composed of Q_1-Q_5 shows that $i_{Q1} \cdot i_{Q2} = I_o^2$ [6]. Transistor Q_8 carries the same current as Q_2. With its emitter set to virtual ground by Q_7, transistor Q_8 performs the input I/V logarithmic compression with the compressed voltage appearing at its base. This voltage is then level shifted using Q_9 and applied as input to the filter.

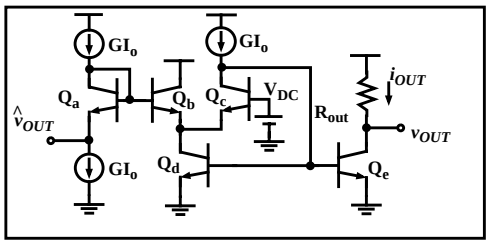

Fig. 5. One half of the output stage.

The last stage used in the 7th-order filter shown in Fig. 1 is the uncompressing stage. The operation of this stage is reciprocal to that of the last stage of the input preconditioner. The circuit used for this purpose is shown in Fig. 5. By varying the current sources of the output stage with a factor G, it was shown that the DC gain of the filter could be controlled [6].

5. MINIMIZING POWER CONSUMPTION: DAMPED INTEGRATOR AND COMPACT BIQUAD

Figure 6 shows the details of the biquad circuits used in Fig. 1. The upper half of the schematic, excluding the components drawn in thick wires, is the class-AB log-domain integrator shown in Fig. 3. The power consumption and die area of the biquad were minimized in two ways: first, two integrators sharing the same output nodes are reduced to a one multi-input integrator by simply augmenting the integrator of Fig. 3 with the components drawn in thick wires in

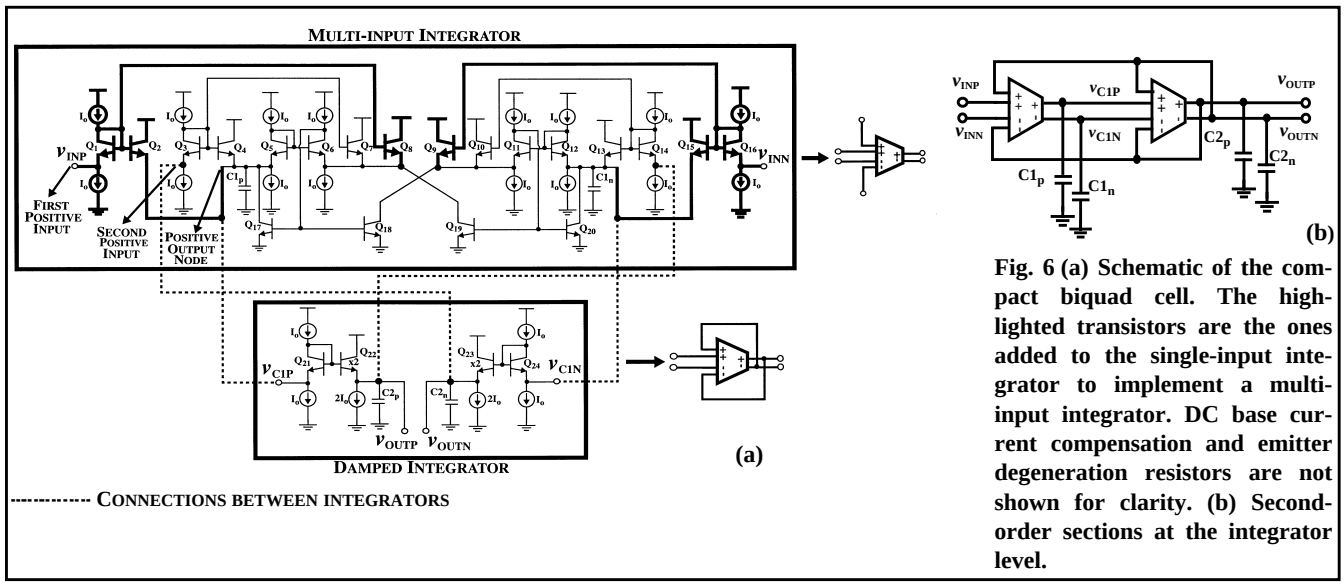

Fig. 6 (a) Schematic of the compact biquad cell. The highlighted transistors are the ones added to the single-input integrator to implement a multi-input integrator. DC base current compensation and emitter degeneration resistors are not shown for clarity. (b) Second-order sections at the integrator level.

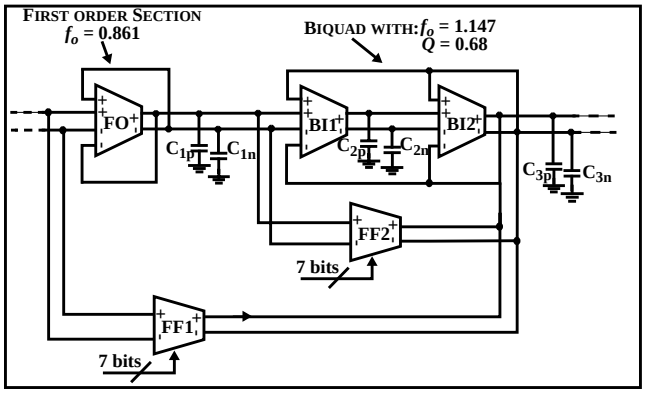

Fig. 7. Realization of phase equalization and magnitude boosting. The log-domain integrator cells FF1 and FF2 add two asymmetric zeros and are digitally programmable via 7-bit DAC's.

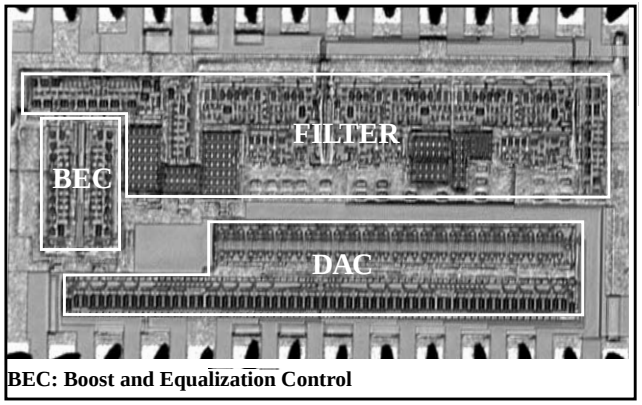

Fig. 8. Chip photomicrograph.

Fig. 6. Second, as was proposed in [8] and done in [7] for a *damped integrator*, a large portion of the circuitry can be replaced by simple current sources, as shown in the lower half of Fig. 6.

6. FILTER STRUCTURE AND SPECIFICATIONS

Unlike all log-domain filter implementations reported to date, which were based on LC-ladder structures (e.g. [5]-[11]), the filter in this paper consists of a cascade of first and second-order sections (Fig. 1), all employing identical nonlinear integrators. This choice of a cascaded structure was made to benefit from the low-sensitivity of its phase response, and to simplify programming [16]. The design specifications of the filter, and the corresponding normalized pole frequencies and quality factors Q of its cascaded sections necessary to realize the 0.05^o equiripple linear phase response are shown in Fig. 1. The pole frequencies are set by the ratios of the integrators' bias currents I_o to the capacitor values. Owing to their exponential input-output transfer functions, log-domain integrators are highly sensitive to DC offsets [7]. For this reason, we chose to use identical bias currents for all integrators, and use capacitor ratios to set f_o and Q. The -3dB frequency of the entire filter (f_c) is tunable from 5 to 70MHz via the integrators' biasing currents I_o. This wide tuning range is necessary to accommodate different data rates and to allow compensation for process and temperature variations. In order to achieve the targeted maximum frequency of operation, the sizes of the capacitors at the integrating nodes had to be minimized. Thanks to the very low *parasitic* capacitors of the 25GHz f_T bipolar transistors used, the smallest integrating capacitor value could be made as low as 0.3pF, while keeping the total parasitic, at all filter nodes, less than 25% of the total capacitance. The final values of the capacitors used were optimized to minimize Q-factor degradation at maximum cutoff frequency. With the values of the total capacitances at each node varied by 20% in Monte Carlo-like simulations, it was verified that the group-delay variation in the filter remained below 5%. Tighter performance can further be obtained using one-time trim at wafer sort to compensate for the spread of capacitor values [14].

In order to compensate for the phase distortion of the head, the medium, and the electronics preceding the filter, and to provide partial equalization, both group delay adjustment and high-frequency boost are commonly used in HDD prefiltering. As shown in Fig. 7, these functions are implemented using two log-domain integrators FF1 and FF2 in the feedfoward paths of the first two sections of the filter. The output currents of those integrators are directly added to the current in C_3 from the first biquad. A complete *large-signal* analysis of the *entire filter* in Fig. 1 was performed to ensure the overall linearity of the system. The resulting transfer function is described by equation (8) at the bottom of the page, where I_1 and I_2 are the bias currents of cells FF1 and FF2 respectively, and I_o is the bias current of the remaining cells of the filter. Equation (8) shows that the system in Fig. 1 is linear, with two asymmetric zeros, tunable through I_1 and I_2.

In order to further reduce power consumption, the order of the different sections of the filter in Fig. 1 was chosen such that equalization is performed by the first-order section and the biquad with lowest Q-factor. For the same reason, the biquads were ordered with increasing Q and f_o. The amount of boost (up to 13dB at f_c = 70MHz) and group-delay adjustment (±30%) are digitally programmable via 7-bit digital-to-analog converters (DAC's).

Finally, in order to accommodate the different flying heights, disk velocities, head temperature, and other head/media variations , the gain of the filter needs to be made controllable [12]. As explained in Section 4, this variable gain is obtained, at the output of the filter, by varying the DC bias currents of the output stage.

7. MEASURED RESULTS

A prototype chip was implemented in a 0.5µm emitter width 25GHz bipolar process (Fig. 8). It occupies $1.4mm^2$, partly consumed by the digital circuitry and by the fourteen integrating capacitors. The circuit operates with a 1.5V supply. Figure 9

$$H(s) = \frac{v_{OUT}(s)}{v_{IN}(s)} = G^2 \frac{1 + s(V_T C_2/2I_o)(I_1/I_o - I_2/I_o) - s^2 V_T^2 C_1 C_2 I_1/4I_o^3}{\left(1 + s\frac{V_T C_1}{2I_o}\right)\left(1 + s\frac{V_T C_2}{2I_o} + s^2\frac{V_T^2 C_2 C_3}{4I_o^2}\right)\left(1 + s\frac{V_T C_4}{2I_o} + s^2\frac{V_T^2 C_4 C_5}{4I_o^2}\right)\left(1 + s\frac{V_T C_6}{2I_o} + s^2\frac{V_T^2 C_6 C_7}{4I_o^2}\right)} \quad (8)$$

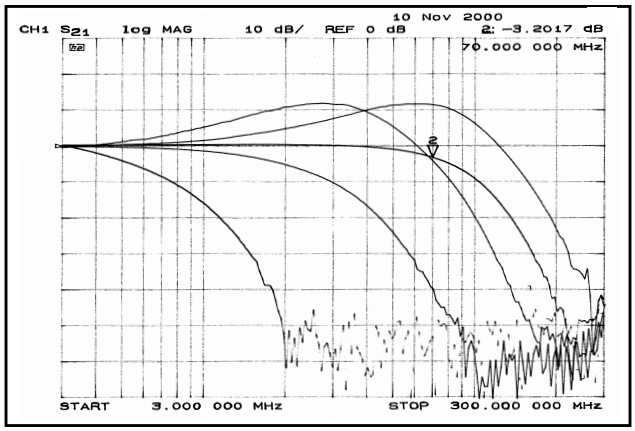

Fig. 9. Frequency tuning (5-70MHz), and boost control (0-13dB).

shows the wide frequency tuning range of the filter. Also shown in the figure is the 13dB maximum amount of boost obtained for low and high frequency operations, satisfying the system's requirements. The tunable gain of the filter (±10dB) for a 70MHz cutoff frequency is shown in Fig. 10.

The group delay variation with 0dB boost for a 70MHz cut-off frequency, shown in Fig. 11, is within ±2.5% up to 1.5 f_c, and within ±5% for frequencies between 1.5 to 2 f_c. Similar results were obtained for lower cutoff frequencies (Fig. 11(b)). The filter exhibits 1% THD for a 140mV$_{p\text{-}p}$ output voltage (exceeding specs.), when set to its maximum cutoff frequency, with $f_{in}/f_c \approx 2/3$ (Fig. 12). Additional THD measurements are shown in Fig. 13. The output noise spectrum, with the input voltage grounded, is shown in Fig. 14. A summary of the filter performance is listed in Table 1.

8. CONCLUSION

This paper demonstrated, for the first time, the use of companding-based filters in hard-disk drive applications. Conventional techniques used to design this type of filters were applied to design a 7th-order companding-based prototype. Power consumption is a key design feature in HDD applications [17]. Experimental results showed that the stringent system specifications could be met, while consuming considerably lower power

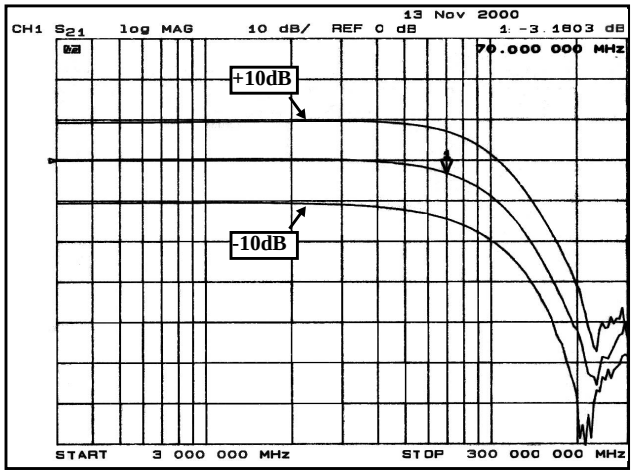

Fig. 10. Tunable gain (±10dB).

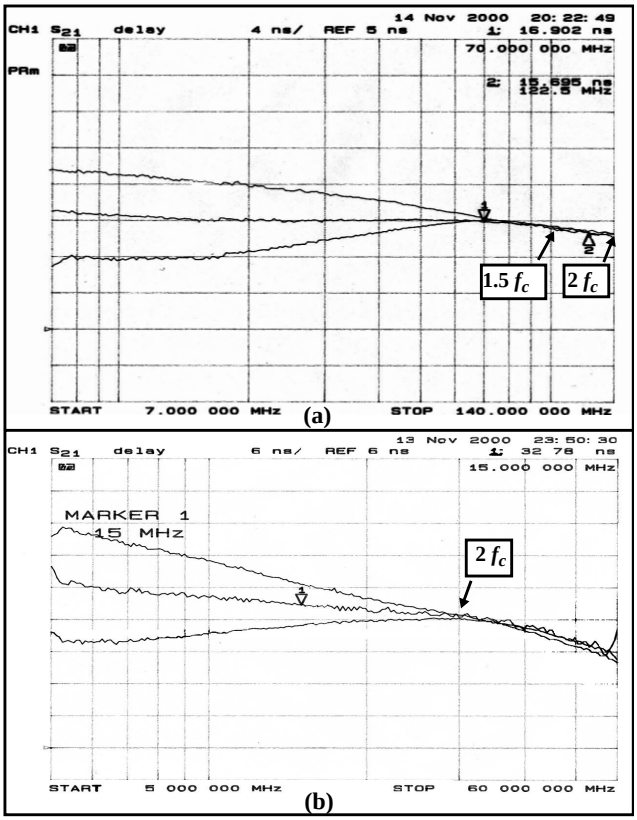

Fig. 11. Group delay variations for (a) f_c = 70MHz, and (b) f_c = 15MHz, showing ±30% low frequency group delay adjustment.

(5-13mW for f_c= 70MHz) compared to state-of-the-art conventional implementations [1].

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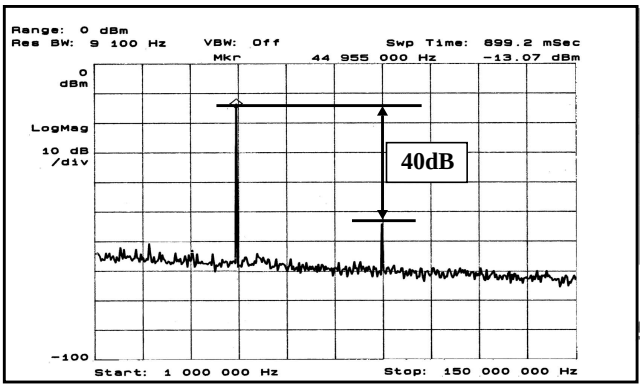

Fig. 12. Output spectrum for a 140mV$_{p\text{-}p}$ input, and 50MHz test signal with f_c= 70MHz.

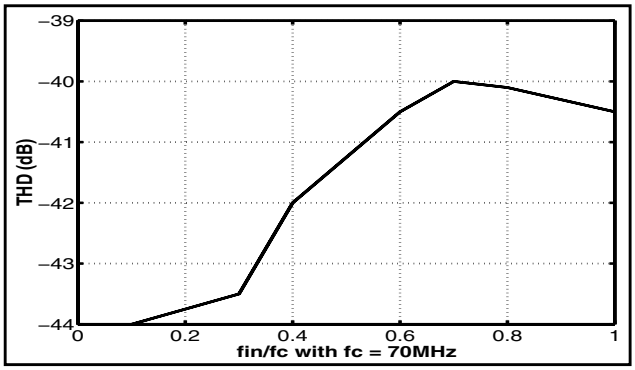

Fig. 13. THD versus f_{in}/f_c, with f_c = 70MHz and V_{in} = 140mV$_{p-p}$.

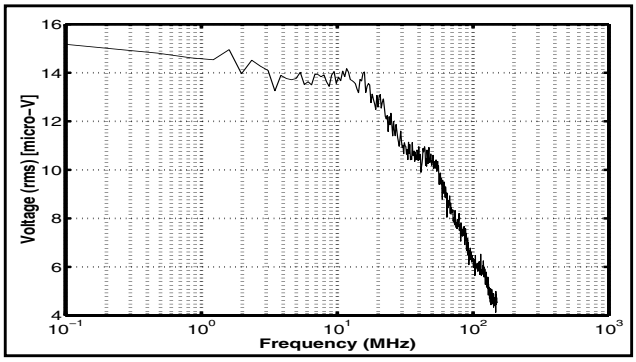

Fig. 14. Spectrum of output noise with f_c = 70MHz, and a Resolution Bandwidth RBW = 17kHz.

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Table 1: Summary of measured filter performance.

	Specifications
Filter Type	7th-order, 0.05° equiripple
Power supply	1.5V
Frequency tunability (f_c)	5-70MHz
Boost programmability	0-13dB (7-bit DAC)
Group delay flatness	±2.5% up to 1.5 f_c
Group delay adjustment at f = 0.1 f_c	±30% (7-bit DAC)
Integrated output noise (f_c = 70MHz)	181μV$_{RMS}$
Output resulting in 1% THD for f_{in} = 50MHz with f_c = 70MHz	140mV$_{p-p}$ (exceeding 100mV$_{p-p}$ spec.)
Dynamic range for 1% THD when f_{in} = 50MHz with f_c = 70MHz	48.7dB
Power consumption (idle channel) Servo mode Without boost and equalization With maximum boost and equalization	 500μW at f_c= 5MHz 5mW at f_c= 70MHz 13mW at f_c= 70MHz
Technology	Nortel 25GHz Bipolar (0.5μm)
Area	1.4 mm^2

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