Synthesis of Low-Leakage PD-SOI Circuits with Body-Biasing

Mario R. Casu
Politecnico di Torino
C.so Duca degli Abruzzi, 24
I-10129 Torino, Italy
casu@polito.it

Gianluca Piccinini
Politecnico di Torino
C.so Duca degli Abruzzi, 24
I-10129 Torino, Italy
piccinini@polito.it

ABSTRACT

In this work we propose a methodology for the reduction of leakage power dissipation through the use of smart body contacts in a partially depleted Silicon-on-Insulator (PD-SOI) technology. Reverse body biasing is used to increase threshold voltage in standby while in active mode PD-SOI gates switch with nominal Vth. As opposed to standard dual-Vth techniques used in CMOS bulk circuits, PD-SOI enables the application of body-bias to all gates included those in critical paths without delay penalties. Results are reported for the ISCAS85 combinational benchmarks.

1. INTRODUCTION

The increase in subthreshold leakage of CMOS IC's is the consequence of reduced supply voltages for power saving and of threshold voltage scaling necessary to prevent from excessive delay degradation. The SIA roadmap forecasts for year 2002 a need for more than 50% reduction of static power and more than 80% for 2005 [1] and points out that this must be achieved not only through technology improvements but that circuit and system level solutions must be adopted.

Several recent papers faced the issue of reducing leakage consumption. The search of the minimum leakage input to be applied in standby is only effective for logic circuits with few levels while for combinational circuits with a large number of levels like the ISCAS85 suite there is a little difference between maximum and minimum leakage [2, 3, 4]. The use of two threshold voltages is one of the most effective methods to reduce subthreshold leakage [5]. A few ways of using a dual-Vth process have been successfully proven. The first one, Multi-Threshold CMOS (MTCMOS), uses a high-Vth "sleep" transistor that provides power supply to low-Vth logic gates in series with the high-Vth sleep MOSFET [6, 7]. The second one uses high-leakage low-Vth gates in critical paths and low-leakage high-Vth gates in the non-critical ones [8]. Another one, Mixed-Vth CMOS (MVTCMOS), allows the use in the same gate of transistors with two different thresholds [9]. MTCMOS has the problem of delay increase and area consumption due to the large sleep transistor [10]. In addition, the use of a gating transistor in series with Vdd creates or increments power supply noise problems and limits the applicability of CAD tools for automated design and verification. The other two techniques can be applied with effectiveness only to circuits having a small portion of the overall gates in critical paths. Moreover, MVTCMOS requires an accurate modeling of the delays at the transistor level to be used in conjunction with algorithms of high/low-Vth selection.

Two thresholds can be obtained through different levels of implantation or different body biasing. The first technique requires additional masks while the second one needs a triple well process in a CMOS bulk technology. In Partially-Depleted SOI (PD-SOI) it is possible to bias the body of single devices because they are isolated by the field oxide [11] such that Vth modification can be obtained without any additional process costs. Moreover simple biasing circuits using pass-gates can remove body bias when exiting from standby to active mode. As a consequence the bias can be applied to all gates because delays, that are in turns directly related to the Vth value, are not modified. This property should be considered together with the fact that SOI circuits are better in terms of delay and dynamic power [11, 12, 13]. Therefore we propose PD-SOI circuits with smart body contacts for leakage reduction in standby mode.

In section 2 our methodology for the reduction of leakage currents through the use of body contacts in a PD-SOI technology is explained. In section 3 we propose a method to be applied after the logic synthesis for choosing the correct instance of gates with optimal body contacts. The results of the application of the methodology to a suite of benchmarks are presented in section 4 while the conclusions are carried out in section 5.

2. LOW LEAKAGE THROUGH BODY BIASING

PD-SOI MOSFET's are usually designed with floating bodies in high performance designs such as microprocessors because the body contacts consume area [13]. They can be instead aggressively used in ultra low power designs where area and time constraints are often of less concern. In order to reduce leakage while saving area we propose a smart body contacts approach consisting in placing them when-

ISLPED'01, August 6-7, 2001, Huntington Beach, California, USA.

ever necessary, exploiting the fact that the leakage through a series of MOSFET's can be reduced by modifying Vth of a single device. Such an approach has a degree of similarity with MTCMOS where a single high-Vth "sleep" MOSFET is placed in series with the low-Vth cells that perform logic operations. Our technique consists instead in assigning a "sleep" function to some normal low-Vth transistors through a proper body biasing. This solution avoids the series connection of an *ad hoc* sleep transistor which affects delay and increases power supply noise [10]. In order to better explain our approach let's consider a simple nand-2 gate like in Fig. 2(a). If the input in standby mode is known it is possible to place the body contacts that minimize leakage in that state. For instance, if $(A, B) = (0, 1)$ the leakage current is reduced by contacting the body of M1 as indicated in Fig. 2(b). If $(A, B) = (1, 1)$ both M3 and M4 bodies must be contacted.

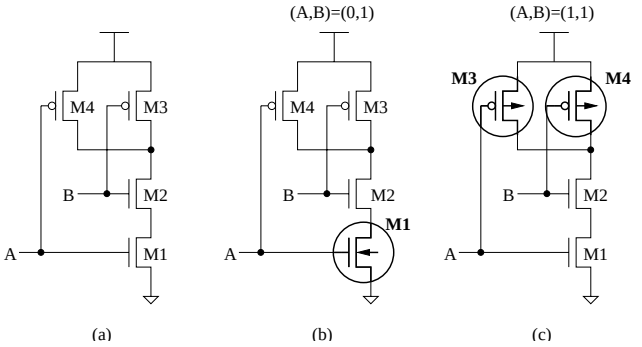

Figure 1: (a) original nand, (b) minimum leakage when (A,B)=(0,1), (c) when (A,B)=(1,1).

In a large circuit consisting of several gates the state in standby can be forced by applying a special "sleep input pattern" multiplexed with the normal inputs or by using special flip-flops that can be forced in a "sleep state" without loss of data, like it was shown in previous works focused on the minimum leakage state search [2]. If the input in standby cannot be known *a priori*, the most probable input for each gate after the technology mapping can be computed and the body contacts assignment minimizing the average leakage current can be chosen. This is possible in PD-SOI because the MOSFET body biased in standby can be left floating in active mode. This can be achieved through a simple low area circuit using pass-gates. The delay is not affected by the Vth increase since it is applied only in standby. Hence, the standard synthesis step in the design flow can be done while the leakage reduction can be obtained through a post-synthesis optimization process. This is the main difference from other proposed algorithms of dual threshold synthesis where the use of high-Vth gates for leakage reduction affects the circuit delays such that a simultaneous optimization of delay and leakage power must be performed [8, 9]. Using PD-SOI with our method, all the gates, included those in critical paths, become low leakage gates in standby such that the leakage saving is improved with respect to previous approaches. Our approach does not exclude the application of the already proposed algorithms since at the present stage only leakage in standby is reduced. It is well known that a higher Vth reduces also short-circuit power. An improvement could be that of fixing Vth high in non-critical paths through static body biasing while leaving the gates in critical paths free from body biasing in active mode. However we will concentrate the following analysis on the leakage dissipation when the circuit is in standby mode.

3. POST-SYNTHESIS OPTIMIZATION

In order to prove the effectiveness of our approach we have considered a small library consisting of NAND, NOR and INVERTER. Each gate has functionally equivalent views with different body contacts such that each one minimizes leakage for a single input configuration. An "all body contacts" view is used when input static probabilities are not given or are near 0.5. In table 1 are reported the leakage values and the number of body contacts for the 2-inputs nand with six different views

$$V = \{\text{nd2Orig}, \text{nd200}, \text{nd201}, \text{nd210}, \text{nd211}, \text{nd2All}\}.$$

The first and the last one are respectively the original 0-body contacts and all-body contacts views while the others are identified by a 2-bits ending meaning the input state in which that view minimizes the leakage current. Table 1 has been obtained through Spice simulations (BSIMSOI model) at Vdd=1 V and applying to body-contacted NMOSFET's -0.5 V and Vdd+0.5 V to PMOSFET's. Similar tables can be given for all our gates. The leakage saving achievable depends on the bias applied. As opposed to dual-Vth CMOS bulk processes, where there is an optimal high threshold at which leakage is minimum [8], the amount of body biasing can be chosen in a large range and only technology and/or design dependent limits do exist.

Table 1: Body contacts (BC) and leakage (L, in pW) of the six nand-2 views for each input.

	view	BC	L(00)	L(01)	L(10)	L(11)
1	nd2Orig	0	1.2	39	60	141
2	nd200	1	0.9	6.6	66	141
3	nd201	1	0.9	6.6	66	141
4	nd210	1	7.4	21	12	141
5	nd211	2	2.4	42	64	37
6	nd2All	4	0.9	15	9	38

The choice of the optimal view for a gate in the library requires a former knowledge of the input state. If input probabilities $p(i \in I)$ of a gate are known we can choose the view $v \in V$ such that the average leakage

$$\overline{L}_v = \sum_{i \in I} p(i) L_v(i) \qquad (1)$$

is minimum. When the input state is known, let's say $i = k$, only one term in (1) is non-zero since $p(i) = \delta(i - k)$. Otherwise we use the input distribution, and if that is the case we assume all inputs $i \in I$ equally probable. Examples of application of (1) are given in the following.

3.1 Case of unknown inputs

Let's consider a tree and a chain implementation in our library of the eight inputs "and" function as shown in Fig. 2. Assuming equiprobable inputs we obtain the numbers in figure representing the probability for a given net to be at logic "1". Application of (1) leads to table 2 indicating the optimal choice for every instance in two cases:

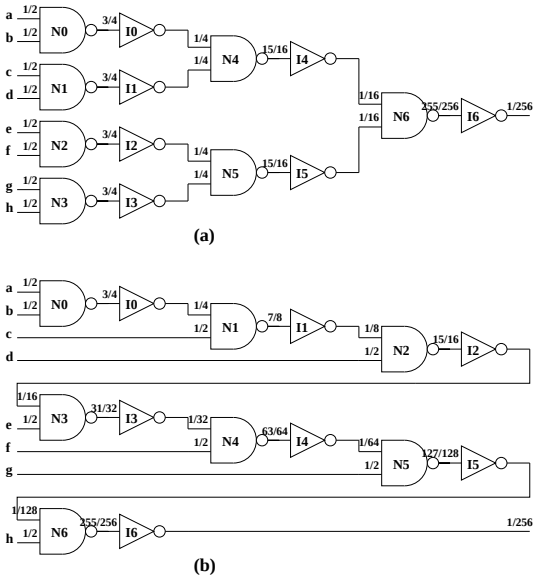

Figure 2: Tree (a) and chain (b) implementations of and-8 and net probabilities.

a) no limits on body contacts number, i.e. nd2All, invAll and nr2All views of the cells in our library can be used;
b) body contacts constraint of at most one per input of each gate.

In table 3 the leakage of the synthesis results reported

Table 2: Optimal choice of instances for minimum leakage for circuits in Fig. 2 (a) without and (b) with body contacts constraints.

Instance	tree (a)	chain (a)	tree (b)	chain (b)
N0	nd2All	nd2All	nd211	nd211
N1÷3	nd2All	nd2All	nd211	nd200
I0÷3	invAll	invAll	inv1	inv1
N4÷5	nd2All	nd201	nd200	nd200
I4÷5	invAll	invAll	inv1	inv1
N6	nd2All	nd201	nd200	nd200
I6	invAll	invAll	inv1	inv1

in table 2 are compared with the leakage dissipation of the original solution without any contacts. The number of body contacts is reported as index of the area overhead.

Without constraints (a), all the gates are of type "All" in the tree implementation because net probabilities are not too distant from 0.5. In the chain, probabilities near the output are such unbalanced that "nd201" is needed. If a constraint is set (b) the leakage reduction is lower but still much better than the original case (c). This means that area and leakage can be well traded-off.

3.2 Case of a priori known inputs

If standby inputs are fixed, each net logic value is known such that it is possible to minimize the true leakage and not its average. Tables 4-5 are like tables 2-3 for fixed standby input $i = \{00000000\}$. In this case constraints are not necessary since we have verified that one or two body contacts per gate can block leakage.

Table 3: Leakage (L, in pW) of circuits in Fig. 2 and body contacts (BC): (a) without and (b) with constraints, and (c) without body contacts. The power is also reported as percentage of the original solution (c).

	L(a)	L(b)	L(c)	BC(a)	BC(b)	BC(c)
tree	100	280	787	42	18	0
chain	88	152	707	42	15	0
tree	13%	36%	100%	–	–	–
chain	12%	21%	100%	–	–	–

Table 4: Optimal instances for circuits in Fig. 2 and input $i = \{00000000\}$.

Instance	tree	chain
N0÷6	nd200	nd200
I0÷6	inv1	inv1

It can be remarked that fixing the input can be useful under two aspects:
1) Leakage can be made lower than the average leakage for equiprobable inputs, both for original and optimized cases.
2) The optimization is much more effective since with less body contacts the same percentage reduction as with inputs and no-constraints can be achieved, while with not dissimilar number of body contacts a reduction better than the constrained case can be obtained.
As a consequence, if input fixing in standby is allowed, this option should be certainly used.

4. RESULTS

We have applied our methodology to the ISCAS85 benchmarks. A tool that processes a synthesized netlist annotated with net probabilities or fixed values and applies the leakage minimization has been developed. In Fig. 3 the average leakage values for equiprobable inputs in the optimal solutions with and without body contacts constraints are reported and compared to the non-optimized leakage of the circuits with floating bodies. The number of body contacts is also given. With constraints the leakage saving is on the order of 50% while about 75% can be obtained without constraints.

It could be interesting to quantify the deviation from these average results. However, this verification requires an exhaustive simulation with all possible inputs or additional methods to evaluate not only the static probability of each net but also its distribution. We have done a simple verification with randomly chosen subsets of all possible inputs to estimate the leakage average and standard deviation. Results seem acceptable since the discrepancy between estimated and measured average is less than 1% for all the ISCAS suite while the measured standard deviation is on the order of 3%. In addition, the deviation is such that the maximum (minimum) measured leakage is near the average plus (minus) three times the standard deviation meaning that true leakage will not be more than 10% larger than the design value.

In Fig. 4 are reported the leakage values obtained when the input is fixed in "standby state". For sake of simplicity,

Table 5: Leakage (L, in pW) of circuits in Fig. 2 and body contacts (BC) for input $i = \{00000000\}$; comparison with original case (L_{orig}, BC_{orig}) is provided.

	L	L_{orig}	BC	BC_{orig}
tree	20	148	14	0
chain	20	148	14	0
tree	13%	100%	–	–
chain	13%	100%	–	–

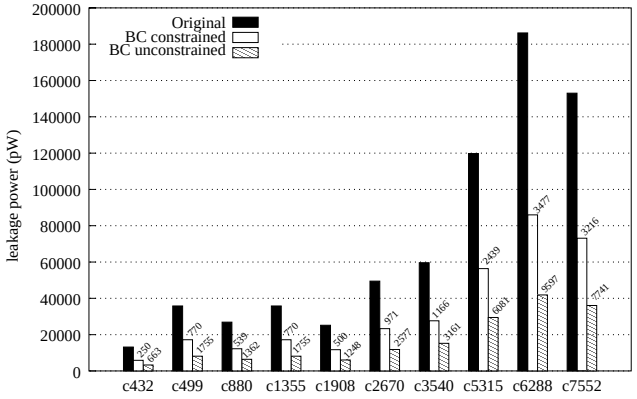

Figure 3: AVG leakage and body contacts for ISCAS benchmarks and equiprobable inputs.

inputs have been fixed to $\{000\ldots00\}$. Results in Fig. 4 con-

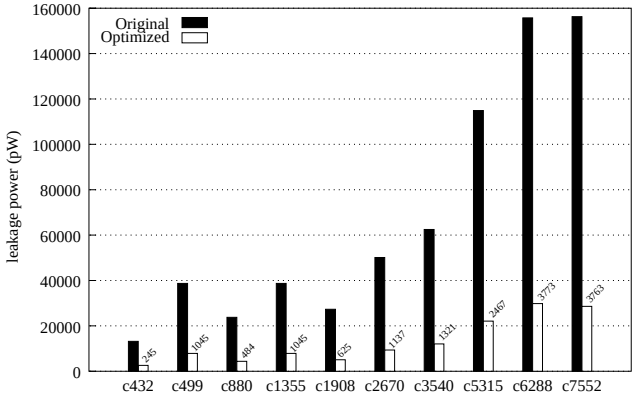

Figure 4: Leakage and number of body contacts for ISCAS benchmarks in case of fixed inputs.

firm that leakage reduction achievable with fixed standby inputs is about 50% better than the case with equiprobable inputs. It must be said that the obtained values are dependent on the amount of reverse bias applied and a different choice from −0.5 V and Vdd+0.5 V could lead to slight different results.

5. CONCLUSIONS

In this work we have proposed a methodology for leakage power saving in partially depleted SOI (PD-SOI) circuits. In PD-SOI it is possible to increase the Vth of single MOSFETs through reverse body biasing in standby and remove the alteration in active mode such that gates can switch at nominal low Vth. As opposed to previous works on dual-Vth we propose the application of the standby body bias to all gates included those belonging to critical paths without affecting active mode timing. A simple library of gates having different body contacts to minimize leakage in each possible input configuration has been used to synthesize the ISCAS85 suite in case of equiprobable or deterministic standby inputs. In the first case up to 75% leakage reduction can be obtained without any constraint on the number of body contacts and 50% with constraint of at most two per gate. In the second case the leakage saving can be on the order or more than 75% with less body contacts. We conclude that area and leakage can be well traded and it could be possible to synthesize with power constraint for minimum area or vice-versa.

6. ADDITIONAL AUTHORS

Additional authors: Guido Masera (Politecnico di Torino, email: `masera@polito.it`) and Maurizio Zamboni (Politecnico di Torino, email: `zamboni@polito.it`).

7. REFERENCES

[1] *The National Technology Roadmap for Semiconductors*. SIA, 1999.

[2] J. Halter and F. Najm. A gate-level leakage power reduction method for ultra-low power cmos circuits. In *Proc. of CICC97*. IEEE.

[3] Z. Chen *et alii*. Estimation of standby leakage power in cmos circuits considering accurate modeling of transistor stacks. In *Proc. of ISLPED98*. IEEE.

[4] M.C. Johnson *et alii*. Models and algorithms for bounds on leakage in cmos circuits. *IEEE Trans. on CAD*, 18(6):714–725, June 1999.

[5] J. Kao and A. Chandrakasan. Dual-threshold voltage techniques for low-power digital circuits. *IEEE JSSC*, 35(7):1009–1018, July 2000.

[6] S. Mutoh *et alii*. A 1-V multithreshold-voltage cmos digital signal processor for mobile phone application. *IEEE JSSC*, 31(11):1795–1802, November 1996.

[7] T. Douseki *et alii*. A 0.5-V mtcmos/simox logic gate. *IEEE JSSC*, 32(10):1604–1609, October 1997.

[8] L. Wey *et alii*. Design and optimization of dual-threshold circuits for low-voltage low-power applications. *IEEE Trans. on VLSI*, 7(1):16–24, March 1999.

[9] L. Wey *et alii*. Mixed-vth (MVT) cmos circuit design methodology for low power applications. In *Proc. of DAC99*. IEEE.

[10] J. Kao *et alii*. Transistor sizing issues and tool for multi-threshold cmos technology. In *Proc. of DAC97*. IEEE.

[11] J.P. Colinge. *Silicon-on-Insulator Technology: Materials to VLSI, 2nd ed.* Kluwer, Boston, MA, 1997.

[12] C.T. Chuang *et alii*. Soi for digital cmos vlsi: Considerations and advances. *Proc. of the IEEE*, 86:689–720, 1998.

[13] C.T. Chuang and R. Puri. Soi digital cmos vlsi - a design perspective. In *Proc. of DAC99*. IEEE.