Design Methodology and Optimization Strategy for Dual-V_{TH} Scheme using Commercially Available Tools

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ABSTRACT

Design methodology for dual-V_{TH} scheme using commercially available tools is presented and optimization strategy for the dual-V_{TH} scheme is discussed. In order to suppress the power consumption, it is shown that using library cells that have various combinations of V_{TH}'s is not needed. The cell library, which contains logic gates with all high V_{TH} transistors and all low V_{TH} transistors, is sufficient to reduce leakage power. 0.1V is shown to be the optimum value for V_{TH} difference between $V_{TH,HIGH}$ and $V_{TH,LOW}$ in terms of power reduction.

1. Introduction

High-performance VLSI design with low supply voltage (V_{DD}) becomes one of the most important issues in CMOS VLSI's, since mainstream V_{DD} will be scaled down to below 0.5V in the coming years. The power and the delay dependence on the threshold voltage (V_{TH}) at 0.5V V_{DD} is shown in Fig. 1. In order to achieve high performance, V_{TH} has to be decreased. Reducing V_{TH}, however, could cause a significant increase in a static leakage power component.

Leakage current is especially important in burst-mode integrated circuits where for a majority of time the system is either in an idle mode, or in a sleep mode where no computation takes place. For example, a cellular phone, pager, or a mobile computer will spend more than 90% of time in a standby mode where a processor is waiting for user input. For these burst-mode applications, it may be acceptable to have large leakage current during an active mode. It is extremely wasteful to have large leakage current during the standby mode because power will be continuously consumed with no useful work being done.

There have been several proposals to reduce the standby leakage current, for example, MTCMOS [1] and VTCMOS [2]. These schemes, however, cannot suppress the active leakage power. Another approach is a dual-threshold voltage (dual-V_{TH}) technique [3], which is quite effective in reducing subthreshold leakage current in the active mode. $V_{TH,HIGH}$ (high V_{TH}) devices can be used to reduce leakage current while $V_{TH,LOW}$ (low V_{TH}) devices can be used whenever high performance is required.

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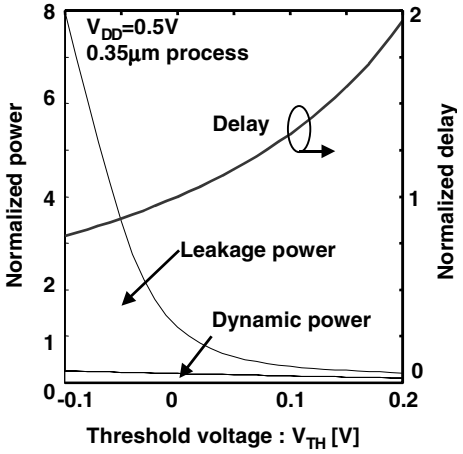

Fig.1 Power and delay dependence on V_{TH}

In the dual-V_{TH} a circuit is partitioned into critical and non-critical paths, and use $V_{TH,LOW}$ transistors only for gates in the critical paths. This approach will reduce subthreshold leakage current both in the active mode and the standby mode. It may achieve large leakage power reduction if the circuit contains many gates in non-critical paths. Thus, dual-V_{TH} scheme is efficient in realizing high-speed and low-power systems.

This paper describes a simple yet effective design methodology for the dual-V_{TH} scheme using commercially available CAD tools. Combinations of V_{TH}'s in a library cell and the optimum value for V_{TH} are presented in the following sections.

2. Design Methodology for Dual-V_{TH} Scheme

VLSI design using the dual-V_{TH} scheme is usually complicated and needs special tools that are specific for the scheme. In this session, a simple and comprehensive methodology is described to realize the dual-V_{TH} scheme. Commercially available tools such as Synopsys Design Compiler (SDC) [4] are used for this methodology. Figure 2 shows a flowchart of this design methodology. First, a cell library for the dual-V_{TH} scheme is

constructed. Then, commercially available CAD tools such as SDC synthesize circuits using the library.

Building the cell library for realizing the dual-V_{TH} scheme is straightforward. In the dual-V_{TH} scheme, at least two kinds of cells are needed. One is a $V_{TH,HIGH}$ cell, where all transistors in a gate cell use $V_{TH,HIGH}$, and the other is a $V_{TH,LOW}$ cell of which all transistors are $V_{TH,LOW}$. $V_{TH,HIGH}$ cells have the larger delay but show the lower power consumption. On the other hand, the $V_{TH,LOW}$ cells have the smaller delay but show the large power consumption. If there are two kinds of cells for synthesis, SDC can optimize delay, dynamic power, leakage power and area as parameters. In the dual-V_{TH} scheme, a path which is not critical in delay should include as many $V_{TH,HIGH}$ cells as possible for realizing low power. SDC takes care if a path meets the timing restriction or not, and makes the power consumption as low as possible.

For the precise synthesis, the cell library must include accurate delay information. In the SDC, a cell delay is composed by four parameters (D_S, D_I, D_T and D_C), which is shown in Fig.3. The figure shows the delay elements used in SDC. Total cell delay is written as

$$D_{TOTAL} = D_S + D_I + D_T + D_C \quad . \qquad (1)$$

Eq.(1) represents a total cell delay that is the sum of four components. The meaning of each component is given below.

D_S: Slope delay of an element (D_S) is the incremental time delay caused by slowly changing input signals. Normally, library cells are characterized with a nominal ramp time to determine the delay from input pin to output pin.

D_I: Intrinsic delay of a circuit element (D_I) is the portion of the total delay that is independent of the circuit element's usage. This portion is the fixed delay form input pin to output pin of a circuit element.

D_T: Transition delay of a circuit element (D_T) is the time it takes the driving pin to change state. The transition time of the output pin on a net is a function of the capacitance of all pins on the net, and capacitance of the interconnect network that ties the pins together.

D_C: Connect delay of an element (D_C) is the time the voltage at an input pin takes to charge after the driving output pin has made a transition. This delay is also known as time-of-flight delay, which is the time it takes a waveform to travel along a wire.

$V_{TH,LOW}$ cells have the smaller value in D_I and D_C than $V_{TH,HIGH}$ cells. These parameters are characterized by SPICE simulation.

New library cells for dual-V_{TH} are added to the existing library. After these procedures, HDL descriptions can be synthesized as usual with the dual-V_{TH} scheme using SDC.

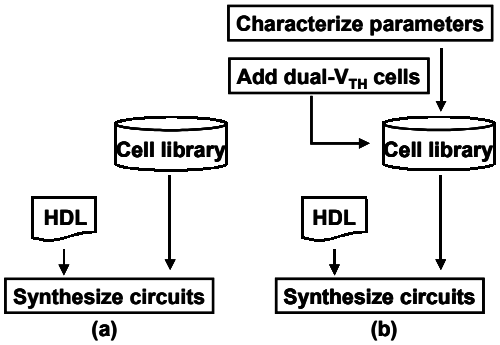

Fig.2 Design flow chart (a) Normal CMOS synthesis flow (b) Dual-V_{TH} synthesis flow

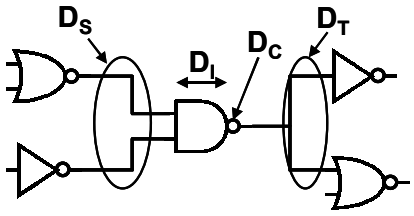

Fig.3 Delay elements in a cell library

3. V_{TH} Combinations in Library Cells

Two V_{TH}'s, namely, $V_{TH,LOW}$ and $V_{TH,HIGH}$, are applied to the MOSFET's in the dual-V_{TH} scheme. Variations of V_{TH} combinations for a library cell can be possible. A part of V_{TH} combinations in a library cell are shown in Fig.4. Circuits shown in the figure all represent NOR function, and have four transistors. Two kinds of V_{TH}'s can be applied to each transistor. Therefore, there are 16 (2^4) candidates for a NOR cell, important variations of which are depicted in Fig.4. If each cell has more than 16 variations, the library size will become more than sixteen times. The size is not acceptable for efficient synthesis.

Cell (c) has larger rise time compared with cell (a) and the leakage power in the worst case is the same as cell (a). Therefore, cell (c) is not needed if cell (a) is included. Thus, the cells in which $V_{TH,HIGH}$ and $V_{TH,LOW}$ are connected in series can be omitted from a library. Cell (d) and cell (e) are symmetrical with respect to the input pins, One of them can be removed. After less usefull cells are removed, 6 candidates, cells (a), (b), (d), (e), (g) and (f) are left for meaningful combination for two V_{TH}'s. The smaller the number of library cells is, the faster and the more efficiently circuits are synthesized. Even if useless cells are removed, the library size is still more than six times, since for other type of functions, there are more variations. Let's call the library which includes many variations of V_{TH} assignment for each logic function, a "complex V_{TH} library"

If a library has only two types for each logic function, where one type is a cell with all $V_{TH,HIGH}$ transistors, and the other is a cell with all $V_{TH,LOW}$ transistors, the number of cells in a library becomes doubled compared with an existing library which is not dual-V_{TH} ready. Let's call the library, a "double sized library".

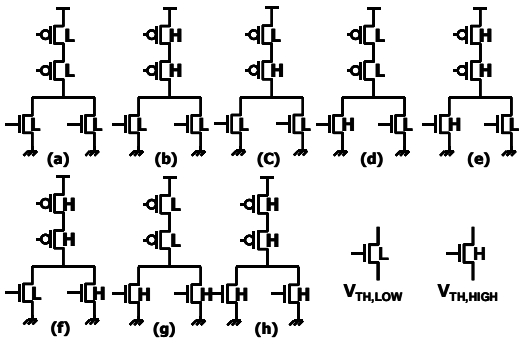

Fig.4 Examples of V_{TH} combination in a library cell

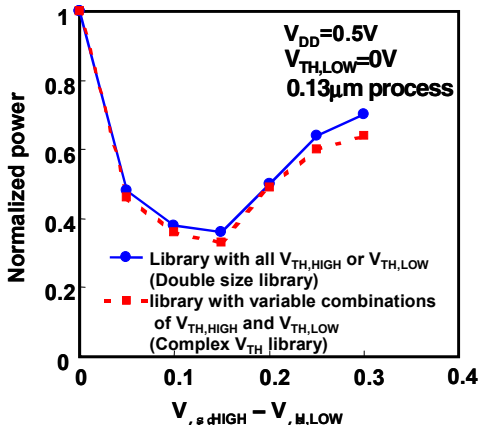

Fig.5 V_{TH} combinations in a cell library

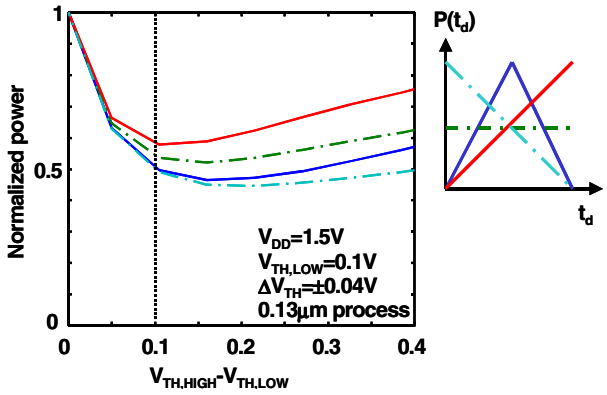

Fig.6 Calculated results of power reduction (V_{DD}=1.5V)

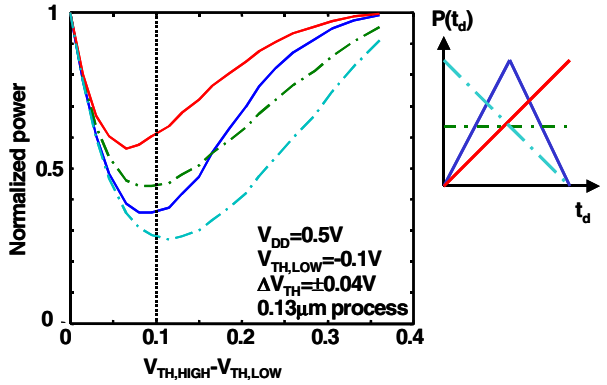

Fig.7 Calculated results of power reduction (V_{DD}=0.5V)

The cell library which is double in size, is still reasonable in size in synthesizing circuits efficiently. The leakage power of two types of cell libraries, the "complex V_{TH} library" and the "double sized library", are compared in Fig.5. The target circuit is a simple processor. As is shown in the figure, the "complex V_{TH} library" consumes less power but the improvement is minor (only 4~7%). Thus it is reasonable to use "double sized library" instead of more complete "complex V_{TH} library".

4. Optimization of $V_{TH,LOW}$ and $V_{TH,HIGH}$ in the Dual-V_{TH} Scheme

$V_{TH,LOW}$ is determined from timing restriction. $V_{TH,HIGH}$, however, is not settled uniquely. There will be an optimum value for $V_{TH,HIGH}$. In this section, optimization of $V_{TH,HIGH}$ and $V_{TH,LOW}$ using analytical formulas and SDC simulation are described.

Calculated results for power reduction are shown in Fig.6 and Fig.7 as a function of $V_{TH,HIGH} - V_{TH,LOW}$. The power consumption is calculated using the formulas which are proposed in [5]. In Fig.6, V_{DD} is 1.5V and $V_{TH,LOW}$ is 0.1V. In Fig.7, V_{DD} is 0.5V and $V_{TH,LOW}$ is -0.1V. Variations of V_{TH}'s and critical paths are taken into account in both figures. As shown in Figs 6 and 7, the optimum difference between $V_{TH,HIGH}$ and $V_{TH,LOW}$ exists. A rule of thumb for optimized V_{TH}'s is written as

$$V_{TH,HIGH} - V_{TH,LOW} = 0.1V \,. \qquad (2)$$

It can be understood in the following way. If the difference is very large, the effect of using $V_{TH,HIGH}$ is very eminent and the transistor with $V_{TH,HIGH}$ completely cuts off the leakage. In this case, however, the number of those transistors used in the design gets small because the $V_{TH,HIGH}$ shows large delay. Thus, the contribution of the dual-V_{TH} scheme is small. On the other hand, if difference is too small, the effect of using $V_{TH,HIGH}$ is not so much and the transistor with $V_{TH,HIGH}$ can not cut off the leakage completely. In this way, there is an optimum value for the difference.

Simulation results with SDC are given in Fig.8. A simple 8bit RISC processor is synthesized with the library generated by the method. (0.18µm process, 3K logic gates) Simulation results show the same tendency as calculated results. That is, power dissipation is optimized at the point where difference of two V_{TH}'s is 0.1V again.

About 80% power reduction is shown to be possible in case of $V_{TH,LOW}$ being –0.1V, which is a possible setting for future high-performance processors with 0.5V supply voltage.

5. Designing A RISC Processor

In order to suppress the leakage power further, combining the dual-V_{TH} scheme and the variable V_{TH} scheme [2] is useful.

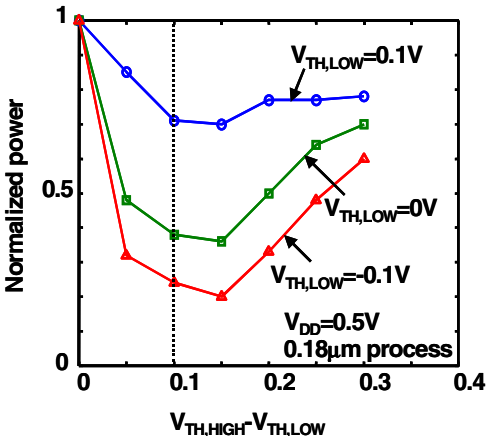

Fig.8 Synopsys simulation results

Variable V_{TH} is a stand-by leakage power reduction technique. V_{TH} is dynamically controlled to be high in a standby mode through a back-gate bias control. This variable V_{TH} scheme needs additional V_{BSP} and V_{BSN} lines in the standard cell area, which are used to control the back-gate bias. In this study, a small scale RISC processor with the variable V_{TH} scheme whose netlist is used for Synopsys simulation is fabricated in a 0.6μm CMOS technology. A microphotograph of the RISC processor appears in Fig. 9. The size of RISC core is 2.1 mm x 2.0 mm and the size of V_{BS} selector is 0.2mm x 0.6mm.

In order to design the processor, the commercially available place and route (P&R) tool [6] was adopted. The only modifications are around substrate/well contacts after P&R is performed. The detailed process of the P&R is shown in Fig.10. First, the P&R is executed using the "double sized library". In order to add metal lines for V_{BSP} and V_{BSN}, the standard cells are placed at appropriate intervals, which can be done by using the conventional P&R tool with an appropriate parameters (see Fig.10(a)). Next, well contacts located on the V_{DD} line and substrate contacts located on the ground line are removed by using SKILL script [7] (see Fig.10(b)). Finally, the n-well pattern, p-well pattern, V_{BSP} lines, V_{BSN} lines and well/substrate contacts are added in the gap between the standard cells (see Fig.10(c)). The area overhead was 9%.

6. Conclusion

A simple yet effective design methodology in designing dual-V_{TH} VLSI's using commercially available CAD tools is proposed. In order to achieve power reduction and efficient synthesis, it is not necessary to use the library cell that has variable combinations of V_{TH}'s. The cell with all $V_{TH,HIGH}$ and all $V_{TH,LOW}$ transistors can be sufficient. 0.1V is shown to be the optimum value for V_{TH} difference between $V_{TH,HIGH}$ and $V_{TH,LOW}$. By using the dual-V_{TH} scheme, 80% power reduction is shown to be possible in case of $V_{TH,LOW}$ being –0.1V, which is a possible setting for future high-performance processors with 0.5V supply voltage.

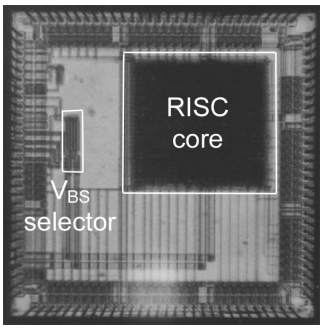

Fig. 9 Microphotograph of RISC processor

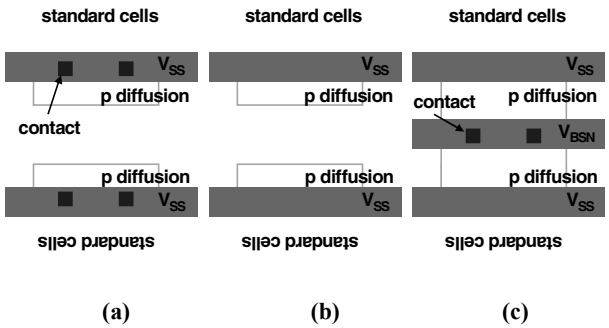

Fig. 10 Place and route using conventional standard cells

Acknowledgement

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References

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