Mixed Multi-Threshold Differential Cascode Voltage Switch (MT-DCVS) Circuit Styles and Strategies for Low Power VLSI Design

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ABSTRACT

This paper presents mixed multi-threshold differential cascode voltage switch (MT-DCVS) circuits for low-power, high performance and deep- submicron VLSI design. These logic circuits incorporate two different sets of CMOS devices, low-V_t and regular high-V_t CMOS devices. By appropriately selecting the low-V_t and high-V_t devices and configurations in a circuit, we can gain performance of circuit while keeping the leakage current and power low. The key approaches are using low-V_t devices to gain performance, using high-V_t devices to cut off the leakage path and also using the reverse- biased low-V_t devices in their standby state. The methodology and algorithm are developed and simulated. The applications of such multi-V_t circuit techniques to the static, domino NORA DCVS and delayed reset circuits are described. The use of footer / header devices, gated-Vdd and a mixture of low-V_t and high-V_t devices to reduce power dissipation and subthreshold leakage current during standby and active modes, and the global design issues are also discussed.

1. INTRODUCTION

The most common used to approach to achieve a low power design is reduce power supply voltage V_{dd}. However, in order to maintain performance, the threshold voltage V_t should also be scaled down so that the overdrive (V_{dd}-V_t) remains large enough. A reduction of V_t causes an exponential increase in the subthreshold leakage current. As V_{dd} and V_t are scaled down, the increased leakage power can begin to dominate the dynamic switching power.

Differential cascode voltage switch (DCVS) logic is a dual-rail CMOS technique which has advantages over single-rail tranditional logic techniques in term of circuit delay, layout area and logic flexibility [1,2]. A further advantages to DCVS circuits is the fact that they can be readily designed for a complex Boolean logic function within single gate delay using straight forward procedures based on Karnaugh maps and tabular methods. The logic function may also be synthesized. Static DCVS circuits may consume more power, however, than traditional CMOS circuits because the charging and discharging times depend on the turn-on and the turn-off paths within the DCVS tree and these are generally not symmetrical. This asymmetry prolongs the period of current flow through the latch of the DCVS circuit during the transient state, thus increasing the power dissipation. Dynamic DCVS circuits, such DOMINA and NORA circuits, often suffer from accidental current discharge due to mismatches in pulldown for the drain nodes.

DCVS logic offers the opptunity to realize faster circuits than are possible with conventional forms of CMOS logic, but the speed advantage is gained at the expensive of power consumption and accidental current discharge. Therefore, a need exists for a DCVS circuits having low leakage and power dissipation, yet providing the increased speed over tranditional CMOS logic circuits.

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2. MT-DCVS DESIGN METHODOLOGY

In this section, we present mixed multi-threshold DCVS (MT-DCVS) circuits for low-power, high performance and deep-submicron VLSI design and methodology. These logic circuits incorporate two different sets of CMOS devices [3-5], low-V_t and regular high-V_t CMOS devices. Based on a mixed V_t approach, performance may be achieved while maintaing a low leakage power for DCVS circuits. Several circuits within the DCVS family are described including dynamic versions of MT-DCVS circuits. A methodology for selecting low-V_t devices is also described.

In Fig. 1a, a MT-DCVS circuit schemetic is illustrated. The MT-DCVS circuit consists of a mult-V_t DCVS tree logic block and a loading circuitry. Both true and complement output (Q and Q') are generated. One important characteristics of the multi-V_t DCVS tree logic block is the mixed use of both low-V_t and high-V_t devices. Low-V_t devices are used to gain speed, and high-V_t devices are used to keep the leakage current low. Using a mixture of low and high V_t devices provides the advantage of gaining speed while keeping the leakage current low. The tree logic block may have any number of inputs for example, A, A', B, B' etc. and can be designed to perform any logic function for example, a sum and carry function in an adder.

A static multi-V_t DCVS circuit is shown in Fig. 1b. In static MT-DCVS circuit, cross-couple latch PFETs are used for the loading circuitry. dual-rail outputs of a MT-DCVS logic tree are connected to Q and Q'. Depending on differential inputs A, A', B, B', etc., either Q and Q' is pulled down by MT-DCVS circuit. In the static state, the logic tree does not pass any direct current except the residue leakage current after the latch sets (P5 and P6). PFETs have high-V_t and are normally used for loading to minimize the leakage current to V_{dd}. In cases where where the leakage current to V_{dd} is not important, low-V_t PFETs may be used for loading. A single-rail CMOS static logic gate with N inputs requires a total $2N$ transistors. A dual-rail DCVS static logic gate with N inputs variables requires only $N+2$ transistors. Hence, the circuit area, device count and power may be reduced in the DCVS logic gate.

The DOMINO versions of MT-DCVS circuits are shown in Fig. 2a-c respectively. For dynamic versions of MT-DCVS gate, the dual-rail outputs may generate true and comple-

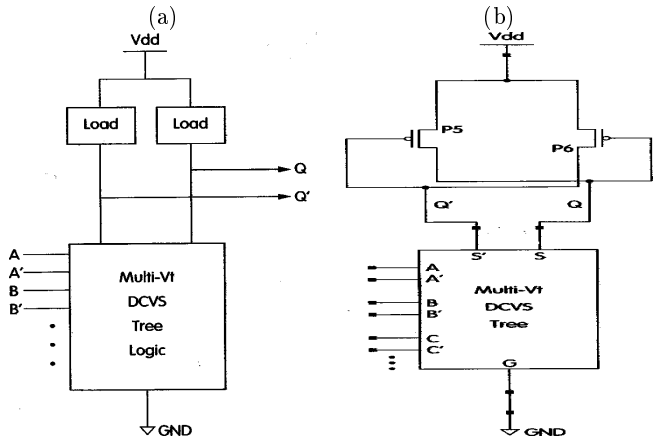

Figure 1: Schematic diagrams of (a) basic (b) static MT-DCVS circuit.

ment signal, F and F', as shown in Fig. 2a. A CLK signal goes HIGH, signaling the initiation a cycle. An NFET pull down tree is evaluated and one of the precharges nodes is lowered with corresponding output going HIGH. As shown in Fig. 2a a low-V_t DCVS n-tree block is used to gain speed and high-V_t clock NFET "footer" device is used to cut down the standby leakage current. Inverters are used at DCVS circuit output to allow signal cascade along the domino chain. PFET keeper devices and inverts are formed as a half latch and used to improve circuit noise margin. An alternate design is shown in Fig. 2b, where MT-DCVS logic tree is used to gain speed and to cut down leakage current and power. An application of this type circuit to a "footless" DOMINO circuit is shown in Fig. 2c. In this case, a MT-DCVS trees is used to minimized the leakage.

Designs of of MT-DCVS tree are illustrated in Fig. 3a-d. Fig. 3a and 3b are circuits designed for a sum and carry operation in a 1-bit adder. The Boolean functions for the circuits shown in Figs. 3a and 3b are $Sum = AB'C' + A'B'C + A'BC + ABC$ and $Carry = AB + BC + AC$. Fig. 3c is a 4-way parity function. Fig. 3d is an arbitrarily chosen Boolean function, $Y = AB'C'D' + A'B + A'C + A'D$. As a convention, the low-V_t NFETs are circled. A', B', C' and D' are complements of A, B, C and D, respectively. Fig. 3a-d collectively illustrate examples of the implementation of mixing low-V_t devices with high-V_t devices.

The optimization algorithm converts arbitrary regular/high V_t into mixed V_t logic circuits which perform the same logic and are optimized for speed, leakage current and power criteria. The algorithm forms the foundation for mixed V_t computer optimization. The optimization criteria are composed of two main factors: speed, standby power and can be extended to cover other factors for example, up/down switching, short-circuit power and transient switching power. Other criterion can be set forth, that no single path from V_{dd} to ground can be made of all low-V_t devices without at least one high-V_t device. A more restrictive criterion is to search all possible paths and no single path should be made exclusively with low-V_t devices. Another important criterion is that the most critical path in the logic tree should be made from mostly low-V_t devices. The low-V_t device is preferably reverse biased in its off state, whenever possible.

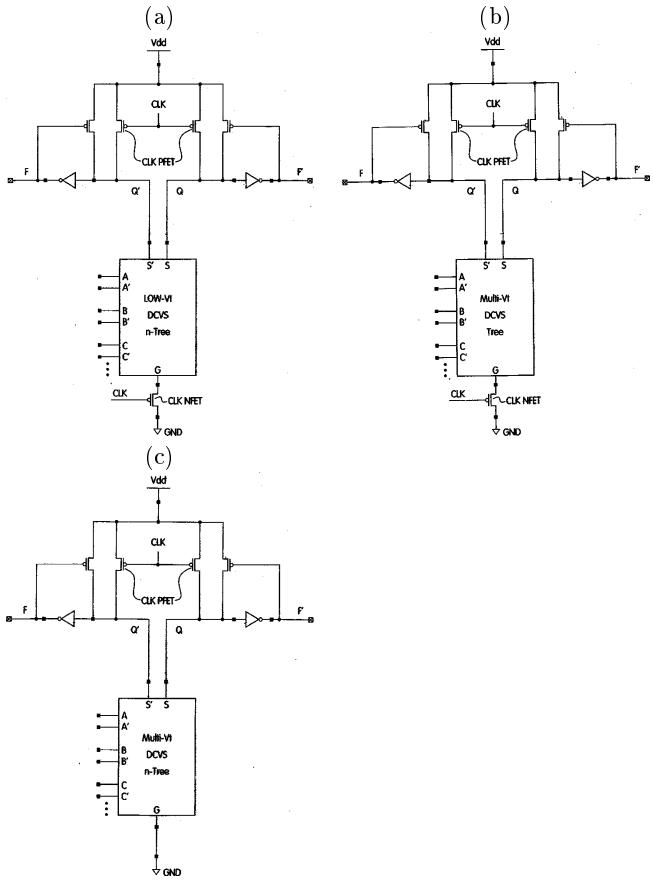

Figure 2: Schematic diagram of Domino MT-DCVS circuit having (a) low-V_t (b) multi-V_t (c) "footless" logic tree with high-V_t clock transistors.

A flow chart of the above algorithm for determining which devices may be defined as low-V_t devices is shown in Fig. 4. The process begins by loading the design circuits. Then the control parameters are input. To complete the initialization process, key word, device group and device block are created. At this point, the process enters a processing loop which tests each configuration in sequence. A test is made to determined if the current configuration passes the rules. If not, the process loops back to retrieve the next configuration to be tested. If the current configuration passes the rules, a test is made to determine if the current configuration also passes the criteria. This is determined by simulation, static timer, delay rules and access to a database of other properties. If not, the process loops back to retrieve the next configuration to be tested. If the current configuration passes the criteria, access is again made to determine the best configuration. If a best configuration is not found, the process loops back to retrieve the next configuration to be tested. When the best configuration is found, it is output as optimized solution.

If no prior knowledge of the standby state input pattern or critical path is known, the general approach described in the above algorithm can be used to select and compare different multi-V_t structures. However, if we have some knowledge of standby state input patterns, a much more effective method

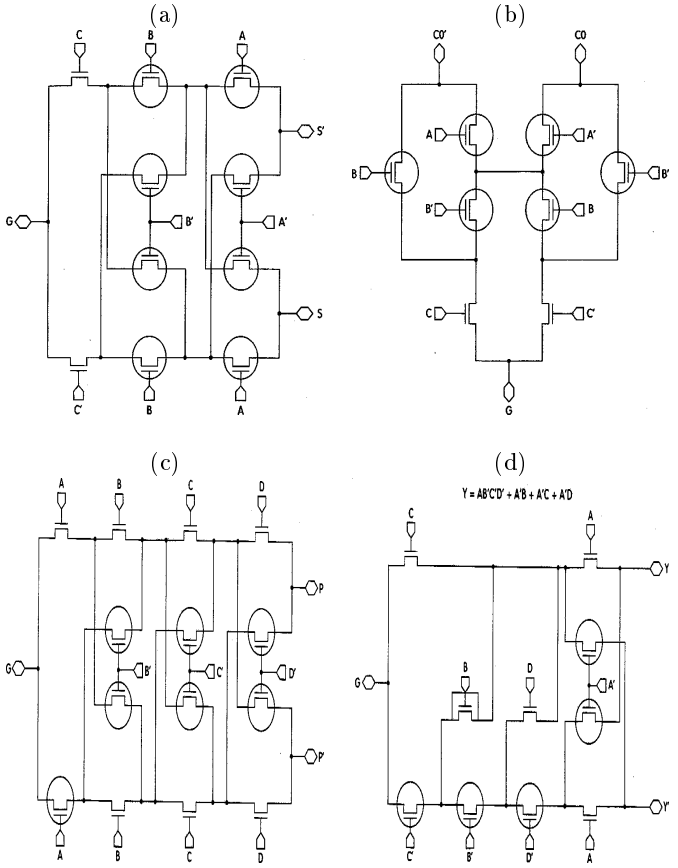

Figure 3: Schematic diagrams of various logic circuits having mixed multi-V_t devices.

for selecting low-V_t devices can be applied to the DCVS tree block. It is as described below and Fig. 3c and 3d show examples of mult-V_t DCVS tree structures that are optimized by this method.

In many applications, the standby state of the DCVS tree is known to be limited to a few input vectors or is known to be limited statistically to a few vectors. A method can derive the best configuration mixed V_t from these input vectors. A SUM circuit shown in Fig. 5a is used to illustrate this method. The following notation will be used, 0 means low-voltage state, i.e. ground, often labeled as L, and 1 means high voltage state, i.e. V_{dd}, often labeled as H. Suppose the input vector of the standby state of this circuit is known to be $(ABC) = (000)$. We then have $S = 0$ and $S' = 1$ and $(A'B'C') = (111)$. All the gates with inputs A', B' or C' will be on, and their source and drain will have equal voltages. Following in this way, as many internal nodes' voltage states as possible are determined and labeled as either L and H. This is indicated in Fig. 5c. (Note that the labels are enclosed in the squares). The general rules as described above are implemented: (1) between any L and H nodes at lease one regular V_t device with a source that should be connected to node L; and (2) between any L and L or H and H all devices can be made low-V_t without affecting the standby state leakage current. The final result is shown in Fig. 5c for circuit with mixed V_t devices. This approach can be applied to any DCVS tree structure. Another example is shown in Fig. 5b and 5d for Boolean function, $Y = AB'C'D' + A'B' + A'C + A'D$. Suppose that standby state input vector is known to be $ABCD = 0000$. The final result is shown in Fig. 5d for circuit with mixed V_t devices.

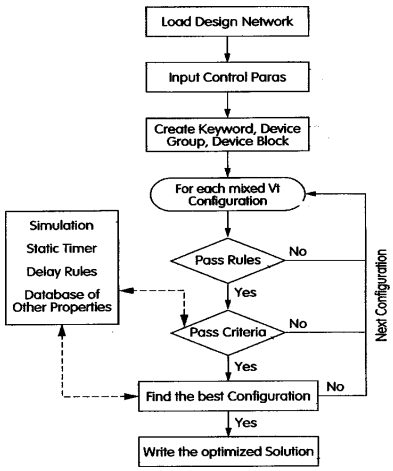

Figure 4: Flow chart for determining low-V_t devices

Fig. 6 is a flow chart to find optimized mixed V_t in DCVS tree structure. Fig. 7 is a block diagram showing a method for producing a multi-V_t circuit. These two figures are self-explained.

3. SIMULATION RESULTS

The correct logic behavior of the MT-DCVS tree configuration has been confirmed by simulation results. The device model parameters used are based on multi-V_t 1.8V 0.25μm bulk CMOS technology. The delay, leakage current, and switch power simulation results for typical DCVS circuits with and without mixed-V_t devices are summarized in Table 1. The base DCVS tree structure is a SUM as shown in Fig. 5a. The multi-V_t DCVS tree is constructed according to the method described above and for condition $ABC = 000$ while the low-V_t DCVS tree is made of all low-V_t devices and the regular devices are made of all regular V_t devices. The structures used for comparison all have identical sizes. The transition that is considered in the delay and switching power simulation is from $ABC = 000$ to $ABC = 001$. The standby-state is assumed $ABC = 000$. The output loading is 10pF and the clock cycle is 4ns in period and 10ps in skew. As shown in Table 1, the low-V_t DCVS circuits are fastest among the three type compared. However, its standby leakage current is also the highest, about 6 times as much as that for regular (high) V_t and mixed V_t. The mixed muti-V_t DCVS is almost as fast as low-V_t DCVS, yet its leakage current is approximately as low as for the regular V_t DCVS. For applications which require low standby power, multi-V_t DCVS is clearly the best choice. Also as shown in Table 1, the NORA and DOMINO versions are much faster than static version. The multi-V_t DCVS DOMINO and NORA circuits show improved characteristics such as higher speed, lower leakage and smaller layout area.

Table 1: Frequency of Special Characters

	Delay (ps)			Leakage Current (nA)			Switching Power(pJ/per Switch)		
	Static	Domino	NORA	Static	Domino	NORA	Static	Domino	NORA
Reg-vt	107	75	67	35	6.7	6.7	0.64	0.353	0.37
Multi-vt	85	68	62	36	7.2	7.2	0.64	0.366	0.38
log-vt	81	66	61	214	40	40	0.63	0.372	0.39

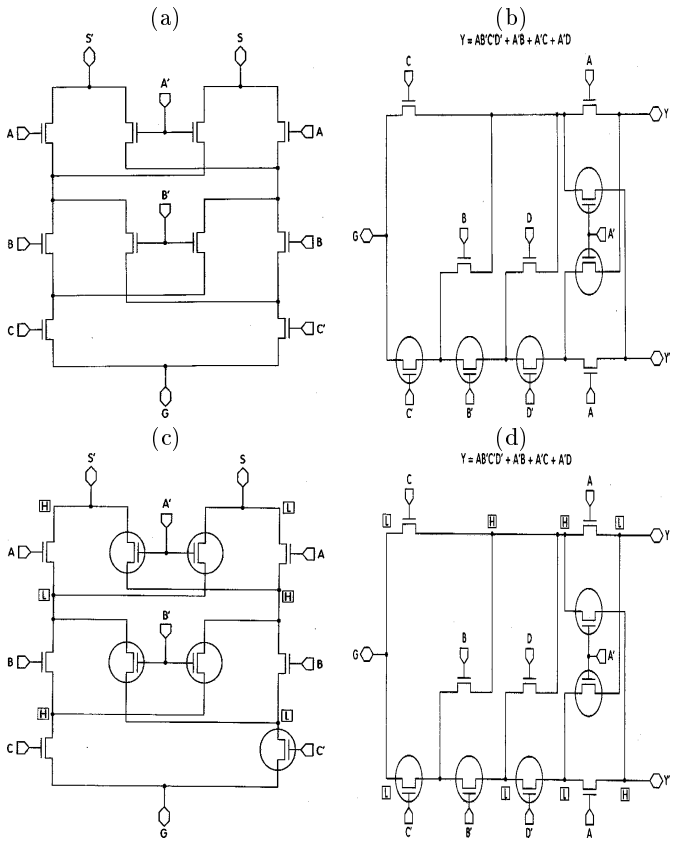

Figure 5: Schematic diagrams of DCVS circuits having (a-b) regular-V_t (c-d) mixed-V_t devices.

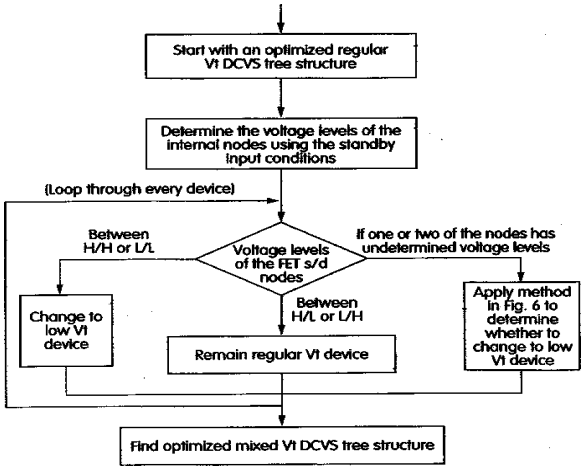

Figure 6: Optimizing a multi-V_t DCVS tree.

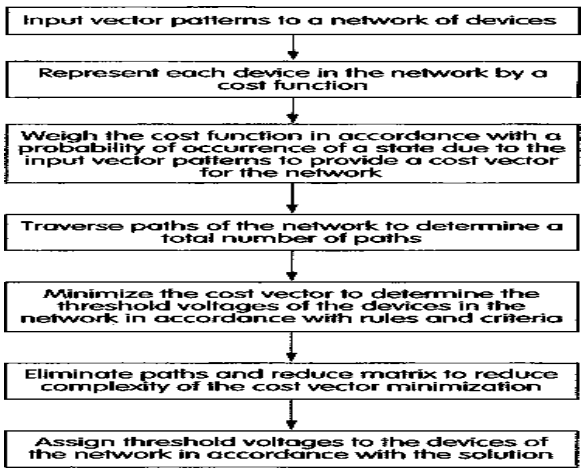

Figure 7: Method for creating MT-DCVS circuit.

4. CONCLUSION

A mixed multi-threshold DCVS (MT-DCVS) logic circuit family has been investigated. These logic circuits incorporate two different sets of CMOS devices, low-V_t and regular high-V_t CMOS devices. circuits. By appropriately selecting the low-V_t and high-V_t devices and configurations in a circuit, we can gain performance of circuit while keeping the leakage current and power low. The key approaches are using low-V_t devices to gain performance, using high-V_t devices to cut off the leakage path and also using the reverse- biased low-V_t devices in their standby state. The methodology and algorithm are developed and simulated. The applications of such multi-V_t circuit techniques to the static, domino NORA DCVS and delay-reset circuits are described.

5. REFERENCES

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