A Sub-1V Dual-Threshold Domino Circuit Using Product-of-Sum Logic

Koji Fujii, Takakuni Douseki and Yuichi Kado
NTT Telecommunications Energy Laboratories.
3-1, Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-0198, Japan
(fujii,douse,kado)@aecl.ntt.co.jp

ABSTRACT

A sub-1 V dual-threshold Domino circuit is proposed to accelerate the operation of CMOS digital circuits at below 1 V. The circuit combines a low and high threshold-voltage (Vt) MOSFET with standby control to make it possible to achieve high-speed evaluation and low standby leakage current. A low-Vt foot nMOSFET is used to shorten precharge time and increase throughput. A product-of-sum logic form is used for implementation of a pull-down logic to increase the noise margin. An experimental 64-bit carry-look-ahead (CLA) adder demonstrated a 0.6-V operation with a standby power of 0.4 μW and a delay time of 4.8 ns.

1. INTRODUCTION

Sub-1V CMOS LSIs are suitable for use in ultra-low-power battery-operated portable applications. Reducing the supply voltage below 1 V significantly decreases the power consumption of CMOS LSIs since the major component of the total power dissipation decreases in proportion to the square of the supply voltage. Conventional sub-1V CMOS LSIs use a circuit technique based on a static CMOS circuit. A multi-threshold CMOS (MTCMOS) circuit combines low-Vt static CMOS gates and high-Vt power switch transistors and thereby achieves fast circuit operation and low standby leakage current [1, 2]. However, below 1 V, the LSIs will not be able to operate fast enough to handle the increasing computing load expected in future portable applications. One way to solve this problem is to use a dynamic circuit, which operates faster than a static circuit due to the small input load capacitance. The Domino circuit is a dynamic circuit, which has been commonly used in the design of high-speed microprocessors.

A dual-threshold Domino circuit, which is intended to operate at voltages down to 1 V, has been reported [3, 4]. It uses a low-Vt MOSFET in the evaluation path and a high-Vt MOSFET in the precharge path to achieve both fast logic operation and low stand-by leakage current. However, the circuit has two drawbacks: long precharge time and a small noise margin. The former is due to the slow high-Vt device in the precharge path and the latter is due to a strong charge sharing in the large pull-down network. Therefore, it is difficult to integrate the circuit on one chip, and to make matters worse, at sub-1 V, these drawbacks become more serious, preventing the correct circuit operation.

This paper describes a sub-1 V dual-Vt Domino circuit with shortened precharge time and an increased noise margin. A foot evaluation nMOSFET is used to suppress the increase of precharge time caused by the high-Vt precharge path. A product-of-sum logic is employed to implement a nMOS pull-down network with a decomposed small pull-down logic. The rest of this paper is organized as follows. First, the configuration and operation of the sub-1V dual-Vt Domino circuit are described. Then, the advantages of using a foot nMOSFET and product-of-sum logic are discussed. Then, an experimental 64-bit CLA adder is described along with some results of a fabricated chip. Finally, the paper is summarized with some conclusions.

2. DUAL-Vt DOMINO CIRCUIT

A schematic diagram of a 2-input dual-Vt Domino circuit is shown in Fig. 1. It consists of low-Vt product-of-sum pull-down logic, a low-Vt foot nMOSFET, a high-Vt precharge pMOSFET, and a static CMOS gate with high-Vt nMOSFETs and low-Vt pMOSFETs. The logic operation is accelerated since the evaluation path contains only a low-Vt device. The leakage current is reduced in the standby mode where the evaluation path and precharge path are controlled to be on and off, respectively.

To shorten precharge time, the low-Vt foot nMOSFET is used for turning off the evaluation path at each Domino stage soon after the clock signal CK falls. Each dynamic

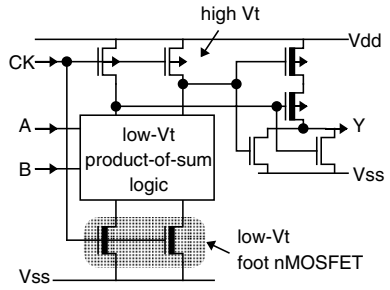


Figure 1: A dual-Vt Domino circuit

ISLPED'01, August 6-7, 2001, Huntington Beach, California, USA.

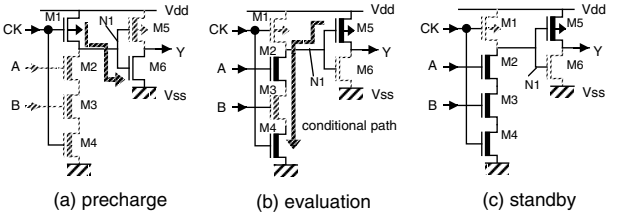


Figure 2: Operation of a dual-Vt Domino circuit

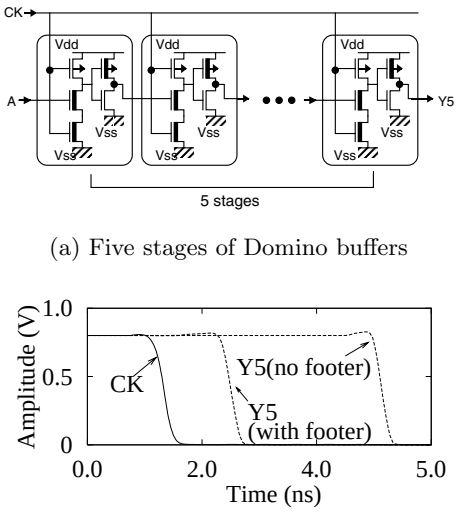
node of a chain of Domino circuits starts to be precharged at the same time and the precharging complete in short time even with a slow high-Vt precharge path. To increase the noise margin at the dynamic node, a product-of-sum logic is used for implementing the nMOS pull-down logic network. This helps to decompose a large pull-down network to a set of small ones followed by the static CMOS NOR gate. The keeper transistor is eliminated to reduce the contention that slows down the evaluation. The resulting weak robustness to charge sharing and charge leakage is suppressed by using the product-of-sum pull-down logic.

2.1 Operation of dual-V_t Domino Circuit

The operation of the Domino circuit during precharge, evaluation, and the standby period is shown in Fig. 2. The Domino circuit operates as a 2-input AND gate with A and B as inputs, Y as an output, and CK as a clock signal. During the precharge period, a falling clock signal CK turns on precharge transistor M1 and turns off foot nMOSFET M4. A precharge path immediately becomes conducting after the evaluation path is shut off. Thus, in the chain of the Domino circuit, the dynamic node N1 rises to high simultaneously at any stage of the Domino circuit. This suppresses the increase of precharge time caused by the slow high-Vt device and prevents the loss of throughput. During the evaluation period, a rising clock signal CK turns off the precharge transistor and turns on the foot nMOSFET. This conditionally turns on the devices in the evaluation path, thereby discharging dynamic node N1 and pulling up output node Y. The evaluation is fast since all the transistors in the path are low-Vt devices. During the standby period, clock CK and all the primary inputs to a Domino circuit are set high [3]. This is done by adding some extra gating logic to an input of the Domino circuit and the clock. Then, high-Vt MOSFETs M1 and M6 are turned off while low-Vt MOSFET M2 through M5 are turned on. Since each of the turned-off high-Vt devices are connected in series to the low-Vt devices, leakage current caused by a low-Vt device is effectively cut off.

2.2 Role of a foot nMOSFET

To verify the effectiveness of the foot transistor, we simulated five stages of Domino buffers with or without the foot device using 0.25-μm CMOS technology. The supply voltage was 0.8 V. The tested circuit configuration and the simulated transient response during the precharge period is shown in Figs. 3(a) and (b), respectively. The precharge starts at the negative edge of the clock signal CK and finishes at the negative edge of the Domno chain's output Y5. The fall of Y5 indicates that precharging of all the intermediate dynamic nodes is completed. The simulation result shows that the precharge time of the Domino chain with a foot nMOSFET is about four times smaller. The foot nMOSFET immediately shuts off the evaluation path at the falling CK and allows a simultaneous start of precharge at any dynamic node of the Domino chain. This minimizes the disadvantage of using a slow high-Vt precharge path since all the dynamic nodes are precharged in parallel. Conversely, without the foot device, the start of precharge at each dynamic node ripples through a slow high-Vt path from one Domino stage to another, increasing the total precharge time.



(a) Five stages of Domino buffers

(b) Simulated transient responses

Figure 3: Effect of a foot nMOSFET

2.3 Product-of-Sum Logic

Charge sharing and charge leakage are major problems in a sub-1V, dual-Vt Domino circuit [4]. The resulting voltage drop at the dynamic node easily causes an erroneous logic transition of the consecutive static logic gate since the switching threshold becomes high due to the combination of low-Vt pMOSFETs and high-Vt nMOSFETs. One way to solve these problems is to break up a wide, deep pull-down network into a few narrow, shallow ones. The small internal capacitance of such a small pull-down network can suppress charge redistribution from the dynamic node to an internal node and reduce the voltage drop at the dynamic node. The small pull-down network also reduces charge leakage from the dynamic node since the effective channel width of pull-down network decreases.

A product-of-sum logic allows us to apply the above idea to implement a Domino circuit. Each sum term can be assigned to a pull-down network of a parallel connection of nMOSFETs. Then, their dynamic nodes are connected to a static NOR gate, constructing a complete Domino circuit. For example, the logic function $(a + b) * (c + d + e)$ is implemented with two different pull-down networks, each of which implements $\overline{a + b}$ and $\overline{c + d + e}$. Then, those dynamic nodes are connected to a 2-input static NOR gate, which realizes a logic function $(a + b) * (c + d + e)$.

This methodology takes advantage of short chains of series nMOSFETs in the pull-down logic network at the cost of long chains of series pMOSFETs in the consecutive static NOR gate. The former contributes to suppressing charge sharing while the latter slows down the circuit operation. So,

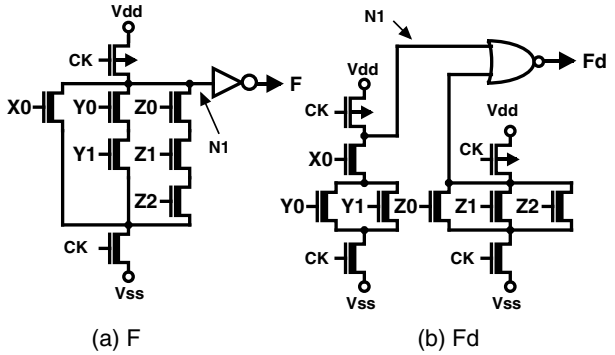


Figure 4: Comparison of pull-down logic

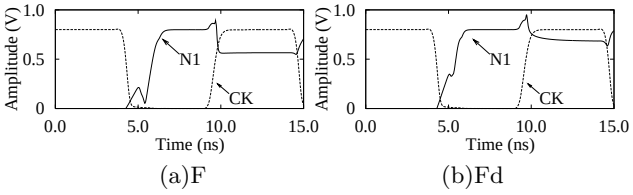


Figure 5: Simulated transient responses

a trade-off exists between them, and the number of stacks required in the nMOS pull-down network depends on the applications.

A product-of-sum logic is obtained by converting a standard sum-of-product logic to its dual logic function. The conversion is done by changing a Boolean logic operation to its dual one, for example, from NOT to NOT, from AND to OR, and vice versa. To guarantee the same logic operation, an additional inverter is required at a primary input and output of the converted function.

To demonstrate the effectiveness of our idea, logic function F=X0+Y0*Y1+Z0*Z1*Z2 and its dual logic function Fd=X0*(Y0+Y1)*(Z0+Z1+Z2) were implemented in a dual-Vt Domino circuit and studied by circuit simulation. The circuit configuration for the logic function F and Fd are shown in Figs. 4(a) and (b). Logic function F was implemented with one dynamic node, which is connected to a wide and deep pull-down network. On the other hand, logic function Fd was implemented with two dynamic nodes, each of which is connected to a pull-down network with less than two series nMOSFETs.

The simulated transient responses of the circuits F and Fd are shown in Fig. 5(a) and (b), where CK denotes a clock signal and N1 a dynamic node. We simulated the worst voltage drop that could be caused by charge sharing. The voltage drop is observed for both circuits at the rising CK. The drop for the circuit Fd, however, is smaller than that for F. The voltage drop is 14 % of the supply voltage for Fd while it is 29 % for F. Therefore, using Fd rather than F, a Domino circuit can suppress a voltage drop at a dynamic node.

3. DESIGN OF A 64-BIT CLA ADDER

To evaluate our circuit technique, a 64-bit carry-look-ahead (CLA) adder was designed using the dual-Vt Domino circuit. The organization of the CLA scheme, which consists of three stages of Domino circuits, is shown in Fig. 6. All

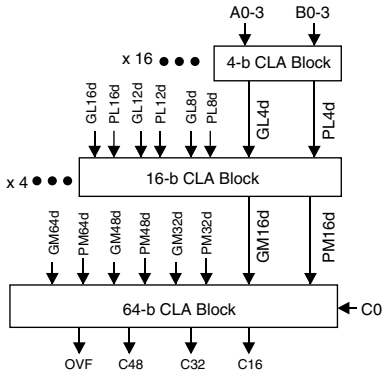


Figure 6: Organization of 64-bit CLA scheme

the intermediate logic functions are obtained in product-of-sum form by converting a conventional sum-of-product logic to its dual logic function. The first stage creates a dual logic function of a 4-bit *group carry generate* (G4) and *propagate* (P4), which are denoted as GL4d and PL4d, respectively. The second stage makes a dual logic function of a 16-bit *group carry generate* (G16) and *propagate* (P16), which are denoted as GM16d and PM16d. The final stage creates carry signals every 16 bits. They are denoted as C16, C32, C48, and OVF. An additional inverter for guaranteeing the same logic function is not needed since a carry function is identical to its own dual logic function. Some of logic functions implemented in each Domino stage are shown in the following logic equations.

$$\begin{aligned}
\text{GL4d} &= \{A3*B3+(A2+B2)*(A3+B3)\} \\
&\quad *\{A3*B3+A2*B2+A1*B1 \\
&\quad +(A1+B1)*(A0+B0)\} \\
\text{PL4d} &= A3*B3+A2*B2+A1*B1+A0*B0 \\
\text{GM16d} &= \text{GL16d}*(\text{PL16d}+\text{GL12d}) \\
&\quad *\{\text{PL16d}+\text{PL12d}+\text{GL8d}*(\text{PL8d}+\text{GL4d})\} \\
\text{PM16d} &= \text{PL16d}+\text{PL12d}+\text{PL8d}+\text{PL4d} \\
\text{C48} &= \text{GM48d}*(\text{PM48d}+\text{GM32d}) \\
&\quad *(\text{PM48d}+\text{PM32d}+\text{GM16d}) \\
&\quad *(\text{PM48d}+\text{PM32d}+\text{PM16d}+\text{C0})
\end{aligned}$$

All of the above intermediate logic functions were implemented in a dual-Vt Domino circuit with at most two series-connected pull-down nMOSFETs. For example, the circuit configuration for GL4d is shown in Fig. 7(a). For comparison, the circuit configuration for a conventional function GL4 is shown in Fig. 7(b). In GL4d, each nMOS pull-down network is organized with at most three nMOSFETs connected in parallel, and with at most two nMOSFETs connected in series. These small pull-down networks effectively suppress the voltage drops at each dynamic node and prevent erroneous logic transition. The simulated delay time of the 64-bit CLA adder is shown in Fig. 8. The delay time was measured from the positive edge of CK to the positive edge of the sum result at MSB, S63, for an input pattern that activates a critical path. For comparison, the delay time of two other types of 64-b CLA adder is shown in Fig. 8, one implemented on a MTCMOS circuit and the other on a dual-Vt Domino circuit with a conventional sum-of-

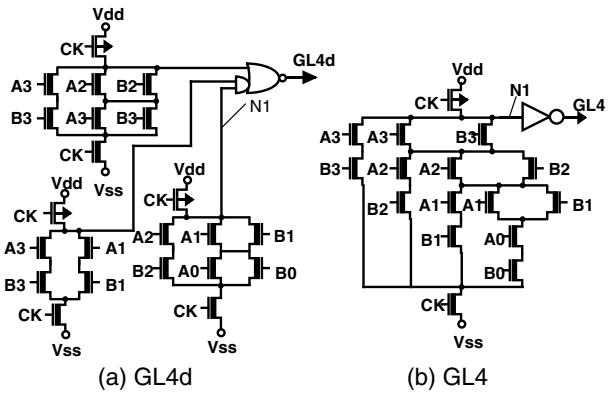


Figure 7: Comparison of dual-Vt Domino circuits

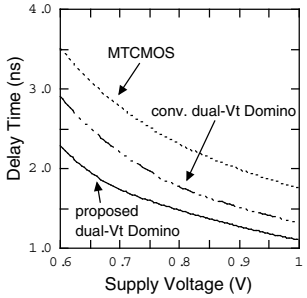


Figure 8: Simulated delay time of 64-bit CLA adders

product pull-down logic. The delay time of the proposed dual-Vt Domino adder is smaller than that of conventional one. Changing the logic expression from sum-of-product to product-of-sum does not deteriorate the circuit speed. This means that the short chain of series nMOSFETs in product-of-sum pull-down logic outweighs the long series pMOSFETs in the static NOR gate. Therefore, in this adder application, the proposed dual-Vt Domino circuit can enjoy the larger robustness to charge sharing without sacrificing speed. Furthermore, the proposed adder is 35 % faster than the MTCMOS adder at 0.6 V. This demonstrates that changing the logic style from static to dynamic is effective for enhancing circuit speed at sub-1 V.

4. EXPERIMENTAL RESULTS

The 64-b CLA adder was fabricated using 0.25-μm CMOS/SIMOX technology with three metal levels. The chip was laid out using an automatic placement and routing tool based on a customized Domino cell. The threshold voltages are 0.1 and -0.1 V for the low-Vt n- and pMOSFETs, and 0.5 and -0.5 V for high-Vt n- and pMOSFETs. A microphotograph of the chip is shown in Fig. 9. The adder core is 1.3 mm x 0.06 mm. The shmoo plot is shown in Fig. 10. The adder operates down to 0.6 V with a delay time of 4.8 ns. The dynamic power dissipation at 0.6-V, 100-MHz operation is 4.3 mW. The static power dissipations during the precharge and standby period are 27 μW and 0.42 μW, respectively. Entering the standby mode, the circuit decreases the static power dissipation by two orders of magnitude. The features of the 64-b CLA adder are summarized in Table 1.

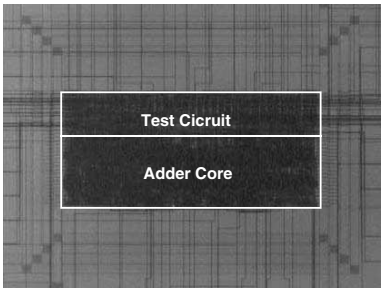


Figure 9: Microphotograph of the fabricated chip

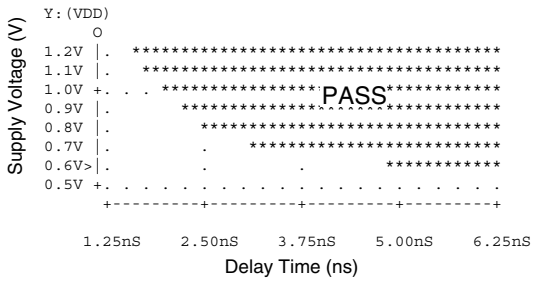


Figure 10: Shmoo plots

Table 1: Features of 64-b CLA adder

Technology	0.25-μm 2-Metal, MTCMOS/SIMOX
Supply Voltage	0.6 V
Delay time	4.8 ns
Power dissipation	4.3 mW (at 100 MHz) 27 μW (precharge period) 0.42 μW (standby period)
Core area	1.3 x 0.06 mm^2
Transistor count	27K

5. CONCLUSIONS

A sub-1 V, dual-Vt Domino circuit was developed to accelerate the operation of CMOS digital circuits at a supply voltage below 1 V. The fabricated chip demonstrated high-speed operation down to 0.6 V with reduced standby leakage current. This circuit technique provides much faster, much less power-consuming CMOS LSIs, which allows more functionality with longer battery life in advanced portable applications.

6. REFERENCES

[1] T. Douseki, et. al., "A 0.5 V SIMOX-MTCMOS Circuit with a 200-ps Logic Gate,"in ISSCC Dig. of Tech. Papers, pp.84-85, Feb. 1996

[2] K. Fujii, et. al., "A Sub-1 V Triple-Threshold CMOS/SIMOX Circuit for Active Power Reduction," in ISSCC Dig. Tech. Papers, pp. 190-191, Feb. 1998

[3] J. Kao and A. Chandrakasan, "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE J. Solid-State Circuits, vol. 35, pp. 1009-1018, Jul. 1998

[4] M. Allam, et. al., "High-Speed Dynamic Logic Styles for Scaled-Down CMOS and MTCMOS Technologies" in Proc. of ISLPED, pp. 155-160, Aug. 2000