Effects of Elevated Temperature on Tunable Near-Zero Threshold CMOS

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ABSTRACT

This paper explores functionality, performance, and energy efficiency of an 80,000 transistor, 0.35μm, back-bias tunable, near-zero V_{th}, 32 x 32-bit multiplier operating at 100°C. Compared to operation at 28°C, performance at V_{dd}=2.0 V degrades 14 percent from 188MHz to 162MHz. At lower supply voltages, back bias is adjusted to minimize power dissipation as a function of operating frequency similarly to what we reported last year at 28°C. Comparing the operating points, the same performance at 100°C requires about 1.5 times the power measured at 28°C. It also requires about 1.2 V additional back bias and about a 20 percent increase in V_{dd}. The fraction of total power dissipated as leakage increases by about 1.5 times.

1. INTRODUCTION

An increasing number of applications, especially portable ones, are becoming limited by power, rather than performance. Reducing supply voltage [1, 2] or signal swing [3] have been shown effective in reducing power. However, to maintain performance with lower supply voltage, the transistor threshold voltage (V_{th}) also needs to be lowered [4], resulting in increased leakage power.

We have demonstrated [5] that circuits fabricated in near-zero threshold CMOS technology, combined with variable threshold CMOS (VTCMOS) techniques [6, 7, 8, 9] and operating at room temperature can achieve significant energy savings as compared to equivalent circuits fabricated in standard CMOS technology. It was also shown that tunable near-zero threshold CMOS technology offers performance advantages over standard CMOS. Unlike standard CMOS where leakage power is usually a negligible portion of the total power, we have shown that the leakage power should be a significant portion of the total power if one is to achieve minimum energy per operation.

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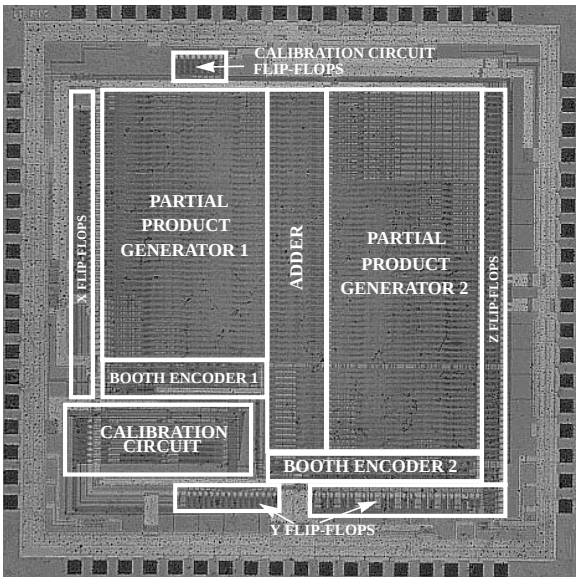

Figure 1: Chip micrograph

This paper explores the effects of elevated temperature on the functionality, speed and energy efficiency of circuits fabricated in near-zero threshold CMOS. It demonstrates that even at increased ambient temperature, back gate bias can be used to optimize the ratio of leakage and switching power and therefore achieve minimum energy per operation.

2. CIRCUITS AND TECHNOLOGY

A 32 x 32-bit signed integer multiplier [10] designed using dynamic, low-swing differential circuit techniques has been used as a test vehicle to measure the effects of elevated ambient temperature on functionality, speed and energy efficiency of circuits fabricated in near-zero threshold CMOS technology. The multiplier uses 4-bit Booth encoding and tree reduction by a 4-2 adder. It was fabricated in a 0.35μm near-zero threshold process. It occupies 3.1 x 3.1 mm area and contains about 80,000 transistors (Figure 1). The multiplier was tested at ambient temperatures of 28±2°C and 100±2°C measured while chip was powered-off. When the chip was operating, we observed up to an additional 6°C in-

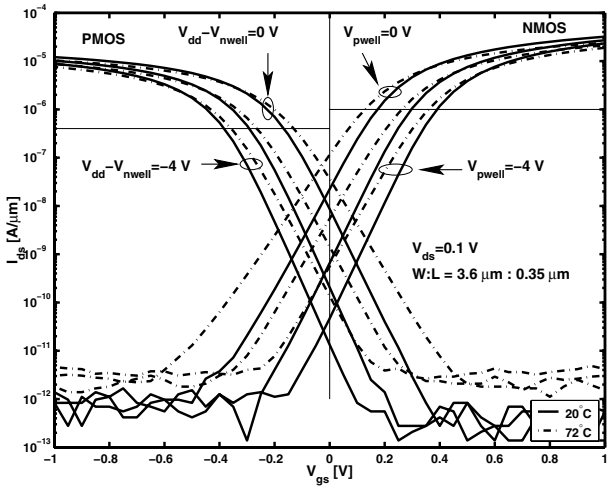

Figure 2: 3.6 μm : 0.35 μm NMOS and PMOS transistor I-V curves at 20°C and 72°C showing large threshold tunability. The curves are plotted for V_{dd}-V_{nwell}=V_{pwell}={0,-2,-4} V

crease in the die package temperature caused by chip power dissipation.

Figure 2 shows I_{ds} vs. V_{gs} transistor characteristics of a 3.6 μm : 0.35 μm PMOS and NMOS device for back-bias (V_{dd}-V_{nwell}, V_{pwell}) voltages ranging from 0 to −4 V at 20°C and 72°C. It demonstrates a wide range of threshold tunability which was used to balance static and dynamic power over frequency, circuit activity, effective logic depth and temperature. Degradation of drive current and subthreshold slope is observed at elevated temperature.

3. RESULTS

Figure 3 shows a Shmoo plot of the multiplier at 28°C. At 28°C the zone of correct operation includes both filled and unfilled circles. For supply voltages of 0.8 V and above, the multiplier is fully functional regardless of the values of the back-bias voltages. At lower supply voltages, a balance between the two biases is required to maintain minimum values of $I_{onNMOS}/I_{offPMOS}$ = 100 and $I_{onPMOS}/I_{offNMOS}$ = 120 to ensure proper circuit operation[5]. In addition, since the NMOS transistors have lower built-in (V_{pwell}=0 V) threshold voltage than the PMOS transistors, the zone of valid operation at low supply voltages is offset with respect to the diagonal. The multiplier was found to be functional down to V_{dd}=0.16 V.

Figure 3 also shows a Shmoo plot of the near-zero V_{th} CMOS multiplier at 100°C. At 100°C the zone of correct operation is indicated by filled circles only. In general, this behavior is similar to the behavior shown at 28°C. As the supply voltage is decreased, a balance between two biases has to be maintained to obtain correct operation. However, while at V_{dd}=0.2 V and 28°C we found the zone of valid operation to span about 0.8 V in both (V_{dd}-V_{nwell}) and V_{pwell}, at 100°C we found only a single valid combination of (V_{dd}-V_{nwell}) and V_{pwell} which produced correct operation. Since increased temperature lowers the threshold voltage and therefore increases I_{off}, only at that particular location in (V_{dd}=0.2 V, -4V≤(V_{dd}-V_{nwell})≤0V, -4V≤V_{pwell}≤0V)

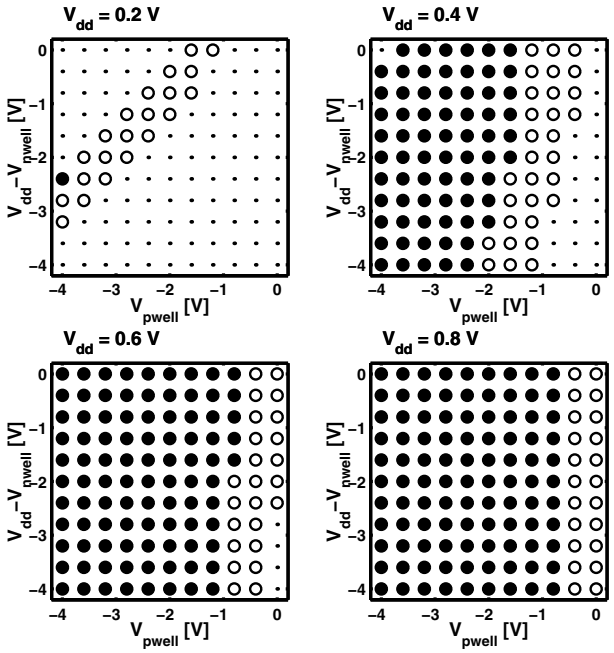

Figure 3: Multiplier Shmoo plot. Filled circles indicate correct operation both at 28°C and 100°C, while unfilled circles indicate correct operation at 28°C only

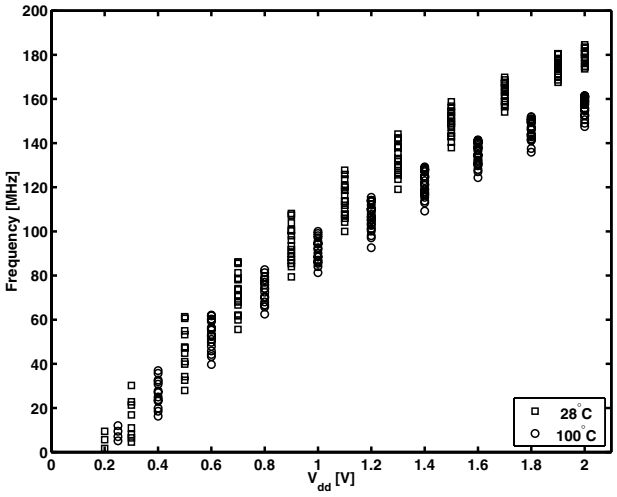

Figure 4: Multiplier frequency vs. supply voltage at 28°C and 100°C

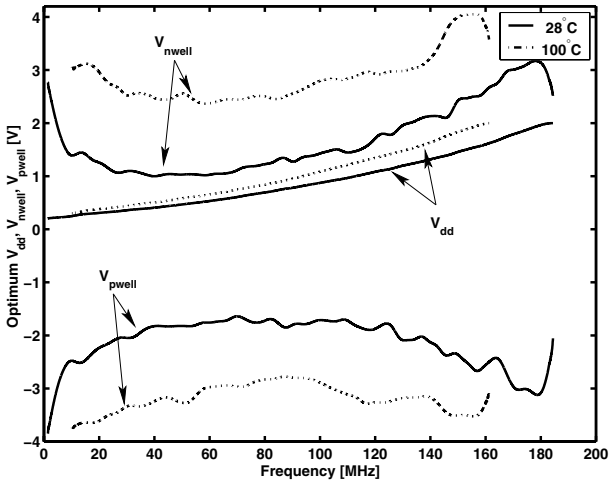

Figure 5: Optimum supply and well voltages vs. frequency at 28°C and 100°C

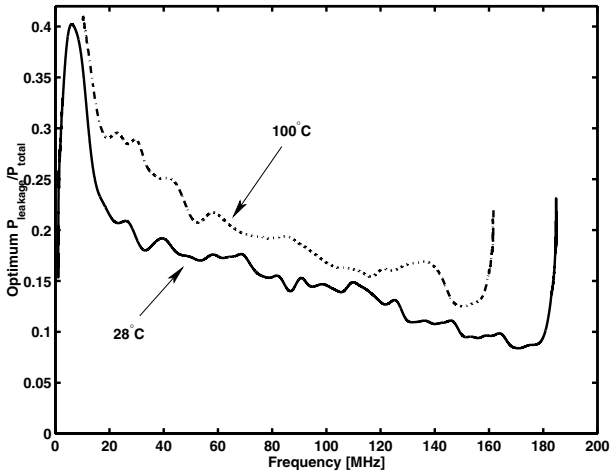

Figure 6: Optimum ratio of leakage power to total power at 28°C and 100°C

space we are able to achieve the minimum required values of $I_{onNMOS}/I_{offPMOS}$ and $I_{onPMOS}/I_{offNMOS}$.

Figure 4 shows multiplier performance vs. supply voltage for both temperatures. The range of points at each value of V_{dd} corresponds to various combinations of $(V_{dd}-V_{nwell})$ and V_{pwell} ranging from (0,0) to (−4,−4). At 28°C the multiplier runs at 188 MHz at V_{dd}=2.0 V, 136 MHz at V_{dd}=1.2 V and at 40 MHz at V_{dd}=0.4 V. At 100°C the multiplier runs at 162 MHz at V_{dd}=2.0 V, 115 MHz at V_{dd}=1.2 V and at 37 MHz at V_{dd}=0.4 V. The performance degradation is about 15 percent at the higher supply voltages due to decreased carrier mobility. At lower voltages the performance degradation is less than 10 percent. The smaller speed penalty at lower voltages can be attributed to improvements in performance resulting from temperature induced threshold lowering.

In low threshold CMOS, the key to achieve minimum power at the required performance is to choose the optimum ratio of leakage power to total power. For example, for the multiplier to run at 40 MHz at 28°C, one can choose a supply voltage ranging from 0.37 to 0.6 V. Although a lower supply voltage may seem advantageous, it requires very low thresholds which in turn makes leakage power too large.

Figure 5 shows the supply and well voltages which result in minimum total power at the given frequency for both ambient temperatures. We observe that to run at any given frequency at 100°C we need to apply higher supply and well voltages than to run at 28°C at that same frequency. The optimum supply voltage is on average 23 percent higher at 100°C than at 28°C. The majority of that increase is due to the performance degradation discussed earlier. The optimum $|(V_{dd}\text{-}V_{nwell})|$ voltage at 100°C is on average 1.10 V higher than at 28°C, while the optimum $|V_{pwell}|$ voltage is 1.25 V higher at 100°C than at 28°C.

As frequency increases over about 100 MHz, we observe a gradual increase in absolute values of the optimum well voltages, indicating a need for higher thresholds. This increase compensates for decreased thresholds resulting from drain-induced barrier lowering, which is more pronounced at higher supply voltages. At the highest achievable frequencies for each ambient temperature we observe sharp decreases in the absolute values of the well voltages, indicating a need for lower thresholds. At the highest frequencies it would be more efficient to run at higher supply and threshold voltages. However, since we limited our supply voltage to 2 V, the only way to achieve the highest frequencies is to run at maximum supply voltage and lowest thresholds.

Figure 6 gives the optimum ratio of leakage power to total power vs. frequency for both temperatures. Both curves show very similar tendencies, with the optimum ratio decreasing with frequency. This variation is caused by different rates of change of leakage and active power as a function of the available ranges of supply and threshold voltage needed to achieve a desired frequency. While operating at 100°C, the chip tolerates a leakage ratio about 3 to 5 percent higher than at 28°C. Although one could apply more back bias and decrease the leakage power, the penalty in increased switching power would be larger. Abrupt increases in the optimum ratio at the highest frequencies for both temperatures can be attributed to the limited supply voltage range as explained in the previous paragraph.

Figure 7 shows minimum achievable energy per operation vs. frequency for both temperatures (left y-axis). It also gives the ratio of these two energies vs. frequency (right y-axis). Over a wide frequency range, the same performance at 100°C requires about 1.5 times the power at 28°C.

(Energy x Time) is often considered as metric of choice for low-power applications [11]. In Figure 8, it is plotted vs. supply voltage for the two temperatures. The most optimum (Energy x Time) point for the multiplier operating at 28°C occurs at V_{dd}=0.36±0.01 V, $V_{dd}-V_{nwell}$=−0.8±0.2 V and V_{pwell}=−2±0.2 V, and is 1.6 times smaller than the lowest (Energy x Time) value attainable at 100°C at V_{dd}=0.50±0.01 V, $V_{dd}-V_{nwell}$=−2±0.2 V and V_{pwell}=−3±0.2 V.

4. CONCLUSIONS

We have demonstrated that the tuning techniques we previously applied to near-zero threshold CMOS at room temperature also work well at 100°C. We can still minimize energy at a target operating frequency by adjusting back bias. To achieve the same performance across a wide fre-

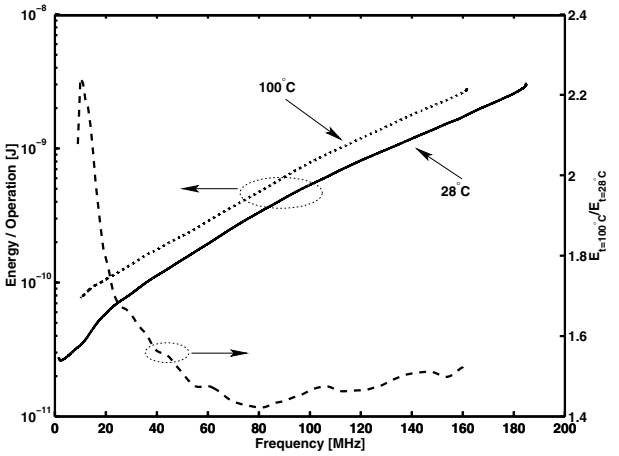

Figure 7: Minimum energy per operation vs. frequency at 28°C and 100°C (left y-axis) and the ratio of two energies (right y-axis)

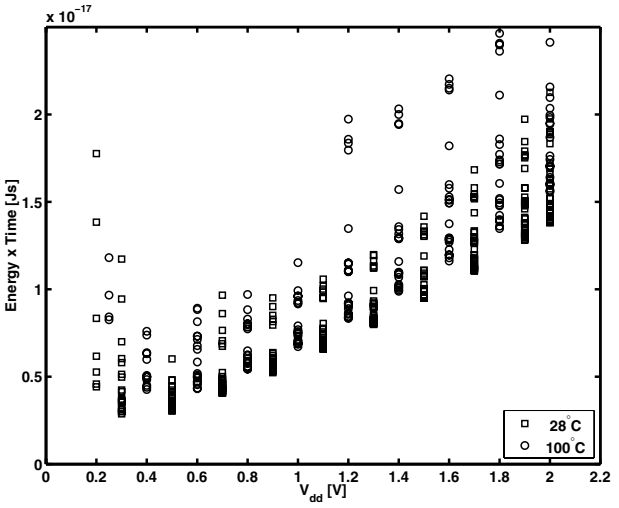

Figure 8: (Energy x Time) vs. supply voltage at 28°C and 100°C

quency range, the back bias needs to increase about 1.2 V, and the supply voltage needs to increase about 20 percent, increasing the power dissipation by about 1.5 times going from 28°C to 100°C.

5. ACKNOWLEDGMENTS

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