A CMOS VCO Architecture Suitable for Sub-1 Volt High-Frequency (8.7-10 GHz) RF Applications

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ABSTRACT

This paper proposes an LC-based oscillator structure which enables operation from a supply voltage as low as 0.85V, while being suitable for high-frequency RF applications. Two VCO prototypes were fabricated in a standard 0.18 µm CMOS process. The 8.7 GHz VCO operates from a supply voltage of 0.85 V, consumes 6 mW, and exhibits -100 dBc/Hz phase noise at 600 kHz offset. The 10 GHz prototype operates from a supply voltage of 1 V, consumes 9 mW, and has -98 dBc/Hz phase noise at 600 kHz offset. A tuning range of 400-450 MHz is achieved without using varactors.

1. INTRODUCTION

A key and critical building block in both wireless and optical communications transceivers is the voltage controlled oscillator (VCO). The continuous increase in the operating frequencies of integrated circuits, driven by the need for wider bandwidths and higher data rates, and the quest for system-on-chip solutions, resulted in a remarkable growth of interest in fully-integrated LC-based CMOS VCO's in recent years (e.g. [1]-[10]). Oscillating frequencies as high as 12.5 GHz have been achieved using standard digital CMOS processes, e.g. [1], [5], [10]. The structure of those VCO's employed stacked PMOS and NMOS transistors sharing the same DC current, and therefore requiring relatively high supply voltages (2.5-3.5V). Driven by the reduction of the power consumption of digital circuits and the scaling of modern technologies, the supply voltages of integrated circuits continue to decrease towards sub-1V. New circuit architectures are needed, especially for analog signal processors, to cope with this trend [11].

The VCO topology proposed in this paper considerably reduces the supply voltage requirement, and consequently the power consumption. This is done by altering the structure of the conventional "complementary differential LC circuit" shown in Fig. 2(a) [5]-[6]. In addition to maintaining the features of the original topology (discussed in Section 2), the proposed architecture provides an alternative to overcome the limited tuning range of back-gate tuning (Section 3). Detailed circuitry and design guidelines for the proposed topology are presented in Section 4.

Two VCO prototypes were implemented in a standard 0.18 µm CMOS process. They operate using 0.85 and 1-Volt power supplies, which is approximately *one third* the supply voltage needed by the original topology (labelled **k** and **l** in Fig. 1). This is achieved while satisfying other requirements such as low phase noise, low power consumption (Fig. 1), and a reasonable tuning range. Measured results are reported and discussed in Section 5.

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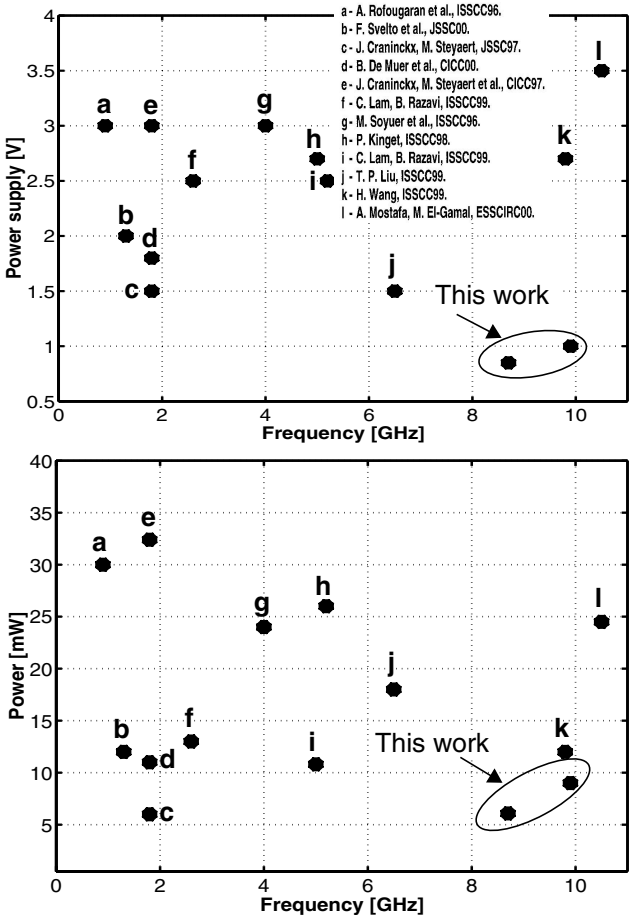

Fig. 1: Comparison of supply voltage and power consumption versus frequency to state-of-the-art VCO's.

2. THE COMPLEMENTARY DIFFERENTIAL LC-STRUCTURE

The complementary differential back-gate tuned VCO in Fig. 2(a) has been shown to allow very high frequencies of oscillation (9.8 - 12.5 GHz) [5], [10]. It uses NMOS and PMOS cross-coupled amplifiers along with a differential inductor *L*. The resonant tank is formed by the inductor and the parasitic capacitances of both amplifiers. Frequency tuning can be performed by controlling the PMOS transistors' back-gate voltages. This configuration has several desirable features:

1) The differential excitation of integrated inductors yields

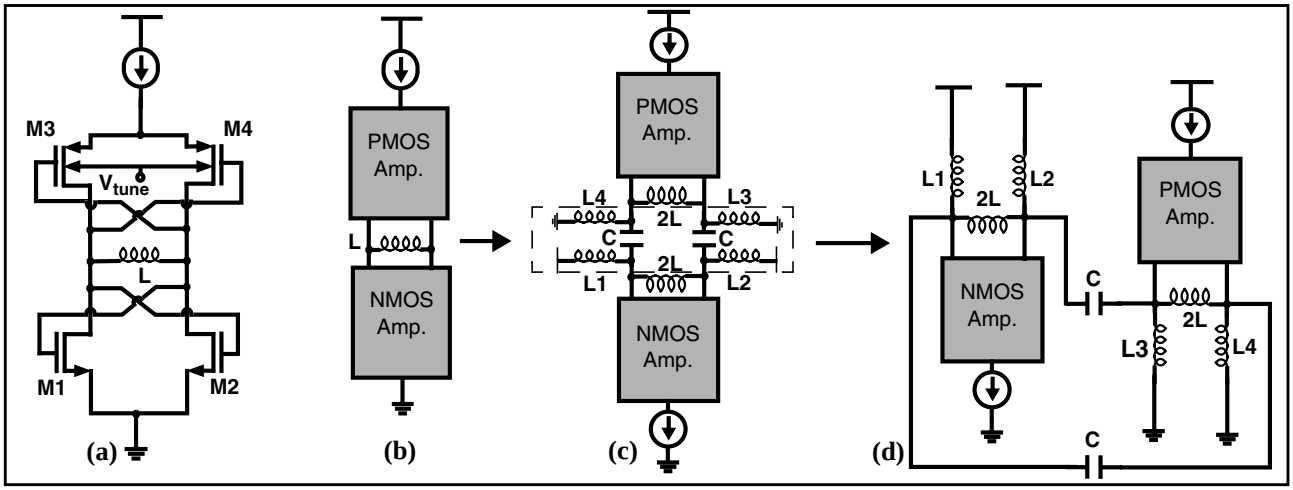

Fig. 2: (a) Complementary differential LC VCO structure [5]-[6]. (b)-(d) Progression towards a low-voltage topology.

higher *effective* quality factor [12]. This results in a decrease in the VCO's phase noise.

2) The PMOS devices are used for frequency tuning by controlling their back-gate voltages, thus

   eliminating the need for varactors, which tend to degrade the tank quality factor at high frequencies.

3) Dispensing of the varactors allows for higher frequency of oscillation.

4) The tank resonator is formed in a loop configuration, i.e. none of its elements is referenced to ground (refer to Section 4.1 and Fig. 4). This makes the frequency of oscillation less sensitive to transistors' and inductor's parasitics to the substrate.

The main drawbacks of the topology in Fig. 2(a) are the relatively high voltage supply required, and the limited tuning range provided by back-gate tuning.

3. PROPOSED CIRCUIT ARCHITECTURE

The progression of the circuit structure towards a low-voltage topology is shown in Fig. 2. Capacitors are inserted between the PMOS and NMOS sections to decouple their DC bias, without affecting the AC interaction between the two tanks. Inductors *L1-L2* are then added to ensure a DC path from the power supply to the NMOS tank, while presenting a high impedance to the AC signals. Similarly, inductors *L3-L4* secure a DC path for the PMOS tank to ground.

It is clear that the resulting topology significantly reduces the voltage supply required, while maintaining the characteristics of the original circuit. A second advantage is gained by decoupling the DC biasing of the two tanks: Tuning can now be done either using the back-gate voltage of the PMOS tank, or via its bias current. Combining both tuning mechanisms results in a wider tuning range (Fig 8).

4. CIRCUITRY AND DESIGN GUIDELINES

Fig. 3 shows the complete transistor-level VCO circuit. In the following sub-sections, we briefly highlight the main design issues related to the proposed structure.

4.1 The LC Tank Resonator

Figure 4 shows the AC equivalent circuit of the LC-tanks of the VCO in Fig. 3. It is composed of two differential inductors *2L*, in parallel with a total capacitance composed of the drain-gate capacitances C_{dg} and gate-source capacitances C_{gs} of *M1-M4*. All the capacitances related to *M1-M2* form the fixed component of the tank capacitance, whereas those of *M3-M4* form the variable part. The design requirements of the DC-blocking capacitors *C*, and the AC-blocking inductors *L1-L4*, are discussed in subsequent sections. In the high-frequency equivalent circuit shown in Fig. 4(b), the coupling capacitors are treated as short circuits, and *L1-L4* as open circuits. The oscillator frequency is given by $f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{\text{tank}} \cdot C_{\text{tank}}}}$, where

$$C_{\text{tank}} = C_{dgM1} + C_{dgM2} + \frac{\langle C_{gsM1} + C_{gsM2} \rangle}{C_{gsM1} \cdot C_{gsM2}} + C_{dgM3} + C_{dgM4} + \frac{\langle C_{gsM3} + C_{gsM4} \rangle}{C_{gsM3} \cdot C_{gsM4}}, \quad (1)$$

and $L_{\text{tank}} = 2L \parallel 2L = L$.

4.2 The Coupling Capacitors

The sizes of capacitors *C* need to be chosen to ensure they present a low impedance path to the RF signal between the PMOS and NMOS tanks, at the frequency of oscillation. For this, the following condition needs to be satisfied

$$2C \gg C_{\text{tank}}. \quad (2)$$

We used two 2.5 pF high quality metal-insulator-metal (MIM) capacitors, which represent approximately 7-8 Ω of resistance at f_o.

4.3 The AC-Blocking Inductors

The role of *L1-L4* is to prevent the tank's energy from leaking to the voltage supplies. They should act as AC-blocking impedances. The impedance of each one of those inductors at f_o, Z_{Lblock}, needs to be significantly larger than the tank impedance Z_{tank}. It can be shown that this condition is ensured when the following relations are satisfied

$$\frac{Z_{Lblock}}{2} \gg Z_{L_{\text{tank}}} \parallel Z_{C_{\text{tank}}}, \quad (3)$$

$$_{block} \gg \frac{2 \cdot L_{\text{tank}}}{1 + (4.\pi^2 \cdot f_o^2 \cdot L_{\text{tank}} \cdot C_{\text{tank}})}. \quad (4)$$

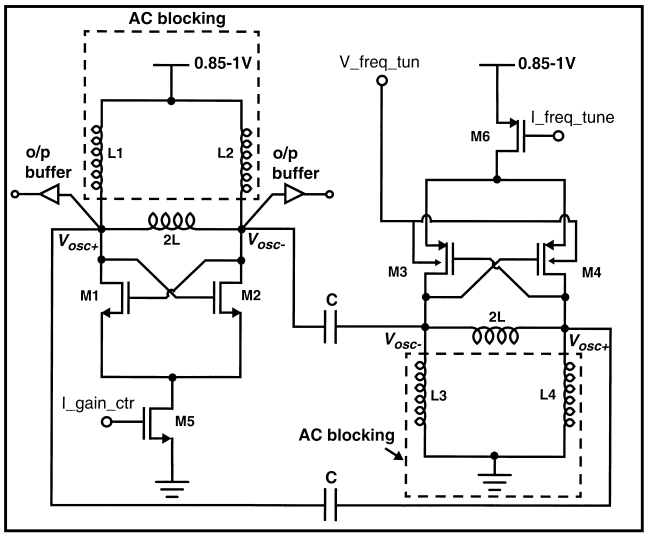

Fig. 3: Circuit of the proposed VCO using capacitively coupled NMOS-PMOS LC tanks. The output buffers are on-chip PMOS transistors with 50 Ω resistor loads.

In our prototypes, each one of the blocking inductors is made up of a combination of an integrated spiral inductor in series with the bonding inductance of the package, with a total of approximately 3.5 nH.

5. EXPERIMENTAL RESULTS

A micrograph of the 8.7 GHz chip is shown in Fig. 5. Symmetry is conserved throughout the entire layout. All control nodes are bonded for packaging, while ground-signal-ground pads were used for on-chip probing the RF output. The tank's coupling capacitors are built using the three top metal layers only, in order to avoid signal leakage to the substrate. Line widths are set according to RF design guidelines, keeping DC lines thin and AC connections wide and as short as possible.

The measured single-ended output spectrums for the 8.7 and 10 GHz circuits are shown in Figs. 6 and 7, and were used to directly estimate the phase noise. The latter are -86dBc/Hz and -82dBc/Hz at a 100 KHz offset for the 8.7 and 10 GHz VCO's respectively. Note that the average power of the signal is underestimated due to the narrow span and limited resolution bandwidth of the spectrum analyzer. In estimating the phase noise, the signal power was measured using a wider span [2].

Two tuning mechanisms can be used to vary the VCOs' frequencies. Fig. 8 (a) shows the frequency tuning using the back-gate voltages of the PMOS tank at a constant bias current of 2.36 mA. Fig. 8 (b) shows frequency tuning using the bias current of the PMOS tank at a constant back-gate voltage of 0.85 V. The two diamond points in the top figure show the minimum and maximum achievable frequencies, when both tuning approaches are combined. A maximum tuning range of 400 MHz is measured for the 8.7 GHz prototype, and 450 MHz for the 10 GHz.

One added advantage of the proposed topology is that the output amplitude is not very sensitive to the PMOS tank bias current since the transconductance is mainly provided by the NMOS tank, while relatively lower current is used in the PMOS tank. Fig. 9 shows the measured output power of the 8.7 GHz VCO as both the back-gate voltage and bias current of the PMOS transistors are varied. The measurements indicate that as the PMOS tank bias current varies from 0 mA to 4mA, the output power changes only

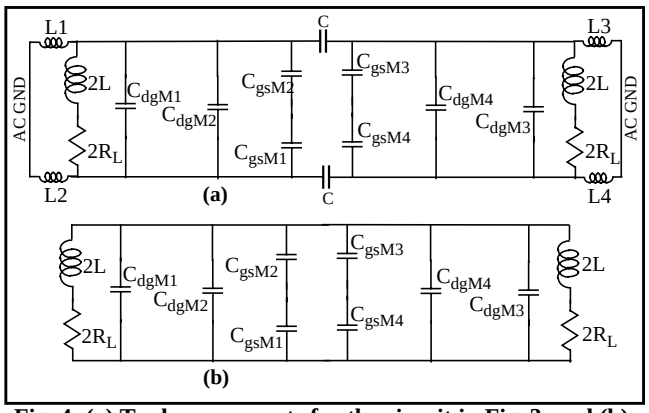

Fig. 4: (a) Tank components for the circuit in Fig. 3, and (b) high frequency equivalent circuit.

by about 3.5 dBm, which can be a worthy trade-off for the increased tuning range. Table 1 summarizes the characteristics and performance of the presented prototypes.

6. CONCLUSION

A CMOS VCO architecture suitable for high-frequency, low-voltage, and low-power applications was proposed. It maintains the advantages of the original complementary differential LC structure, while significantly reducing the supply voltage. Two prototypes were built for proof of concept. As shown in Fig. 1, they require the lowest voltage supply (0.85-1V) and consume the lowest power (6-9 mW) compared to other oscillators operating in the 8-10 GHz frequency range.

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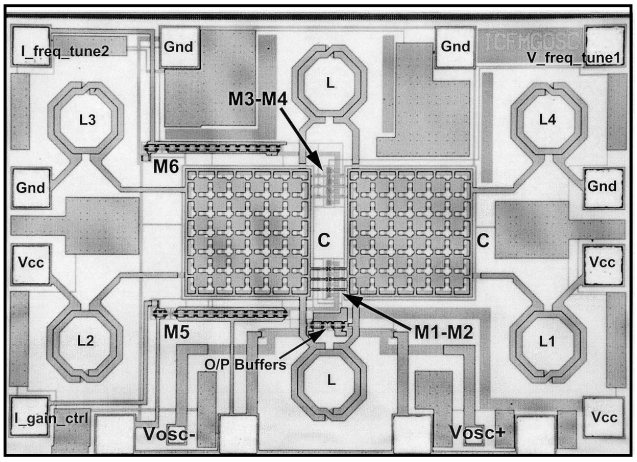

Fig. 5: Microphotograph of the 8.7 GHz VCO.

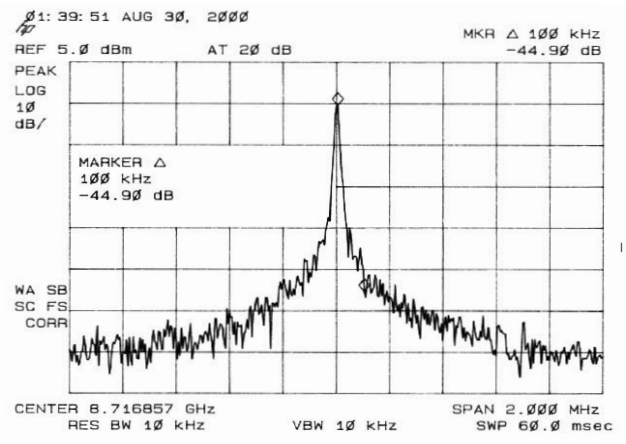

Fig. 6: Measured single-ended output of the 8.7 GHz VCO.

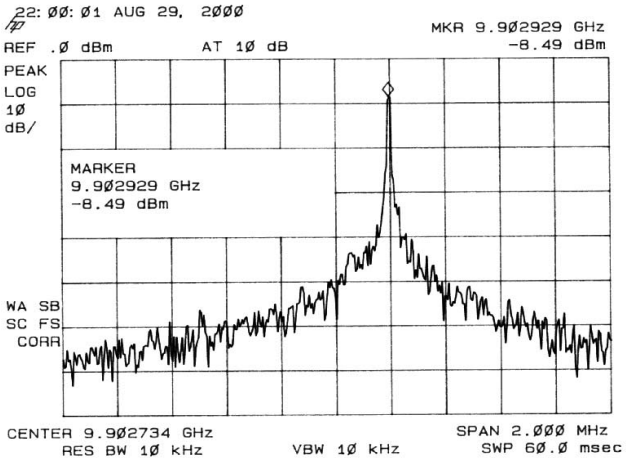

Fig. 7: Measured single-ended output of the 10 GHz VCO.

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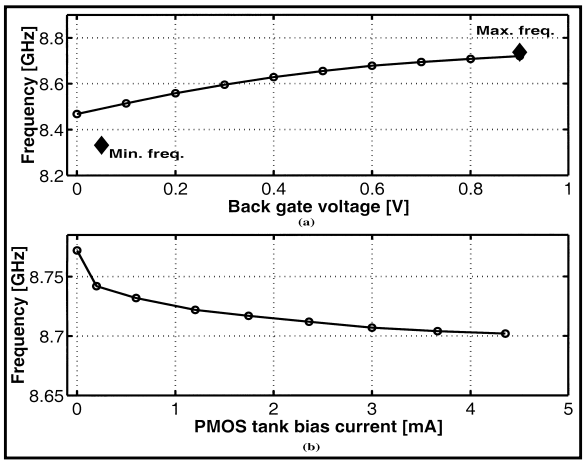

Fig. 8: Frequency tuning versus (a) back-gate voltage, and (b) PMOS tank bias current. The two diamond points on the top figure show the minimum and maximum achievable frequencies, when both tuning schemes are combined.

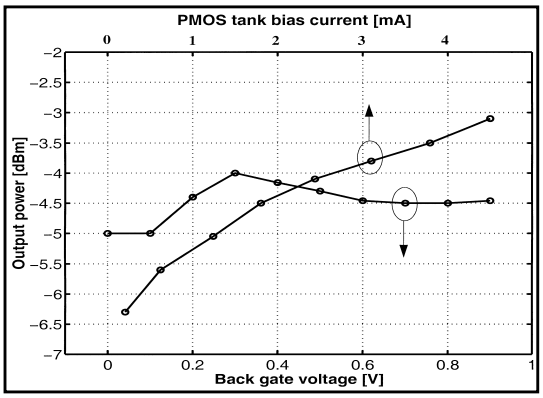

Fig. 9: Output power variation of the 8.7 GHz VCO as function of both the back-gate voltage and bias current of the PMOS tank.

Table 1. Summary of the process characteristics, and performances of the two VCO's.

	Prototype 1 [8.7 GHz]	Prototype 2 [10 GHz]
Technology	0.18 μm, 6 metal standard CMOS	0.18 μm, 6 metal standard CMOS
Substrate resistivity	10 Ω/cm	10 Ω/cm
Thickness of top metal	0.99 μm	0.99 μm
Differential inductor	1 nH	0.85 nH
Estimated quality factor of inductor at f_o	4	5
Size of M1-M2	100 μm	100 μm
Size of M3-M4	100 μm	50 μm
Size of PMOS buffer	50 μm	50 μm
Area	1.5 mm x 1.1 mm	1.5 mm x 1.1 mm
Supply voltage	0.85 V	1V
Supply current	7.1 mA	9 mA
Power consumption	6.0 mW	9 mW
Phase noise @ 100 kHz offset Phase noise @ 600 kHz offset Phase noise @ 1 MHz offset	-86 dBc/Hz -100 dBc/Hz -103 dBc/Hz	-82 dBc/Hz -98 dBc/Hz -101 dBc/Hz
Tuning range	400 MHz	450 MHz
Tuning sensitivity	470.6 MHz/V	450 MHz/V