High Density Capacitance Structures in Submicron CMOS for Low Power RF Applications

Tirdad Sowlati
Philips Research
345 Scarborough Road
Briarcliff Manor, NY 10510 USA.
(914)-945-6044
tirdad.sowlati@philips.com

Vickram Vathulya
Philips Research
345 Scarborough Road
Briarcliff Manor, NY 10510 USA.
(914)-945-6199
vickram.vathulya@philips.com

Domine Leenaerts
Philips Research
Prof. Hostlaan4, 5656AA
Eindhoven, Netherlands
31-40-2744723
domine.leenaerts@philips.com

ABSTRACT

This paper presents four novel interconnect based capacitors with 2 to 3 times the capacitance density of a conventional metal sandwich capacitor and with self-resonant frequencies above 20 GHz, suitable for low power RF applications. Unlike the conventional capacitor, the capacitance density of these structures increases with the scaling of the technology. The structures have been fabricated in both 0.25 µm and 0.18 µm CMOS technologies, measured and an equivalent circuit presented.

Categories and Subject Descriptors

1.3. Analog, MEMS and Mixed Signal Electronics

General Terms

Measurement, Documentation, Experimentation.

Keywords

CMOS, interconnect, RF passives, Bluetooth, HiPerLAN.

1. INTRODUCTION

The motivation for designing RF/analog circuits in digital CMOS is the development of a single chip solution for wireless applications in digital CMOS technologies to reduce power consumption, size and cost. Various transceiver blocks have already been demonstrated in digital submicron CMOS at frequencies in the range of 1- 5 GHz [1-5]. Based on the technical specifications for the available communication bands, we can identify Bluetooth (2.4 GHz) and HiperLAN (5.2 GHz) standards as excellent candidates for RF CMOS single chip radio designs.

Along with active circuits, there is also a push towards integrating high quality passives onto the chip thereby reducing the discrete component count and also avoiding power loss associated with going off-chip. On-chip inductors with high quality factors and fractal capacitors to obtain higher capacitance densities have also been proposed [6-7].

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The low capacitance density of the standard metal sandwich capacitor in digital CMOS results in large chip area consumed by capacitors required in RF/Analog CMOS. By shrinking CMOS technologies, we can achieve higher f_T and f_{MAX} values. However, the metal sandwich capacitors do not scale with this shrink as the dielectric thickness is not scaled. Gate oxide based MOS capacitors can provide higher capacitance densities but are non-linear and voltage dependent. Moreover, their oxides are susceptible to breakdown under large voltage swings encountered in power amplifier designs. Linear and high density capacitors are also required in low power design. As an example, Direct conversion architectures with AC coupling are used to achieve low power consumption [8].

In this work, we present four novel interconnect based capacitance structures, using an optimal combination of fringe, cross-over and metal-metal capacitances. These capacitors have the added advantage of being scalable with "technology shrinks". We will also show that substrate shields do not influence the capacitance density, and that higher Q factors can be obtained.

2. STRUCTURAL DESIGN

In this section, we describe the design of the proposed capacitance structures along with the standard capacitor assuming five metallization layers. Top and side view diagrams in some cases and perspective views in other cases are used for clarity. In all the figures, the grey and black colors indicate the two nodes of the capacitors.

2.1. Metal-Sandwich Capacitor

The conventional capacitor is a multi-plate parallel plate capacitor with alternate plates connected to the same node as shown in Fig.1.

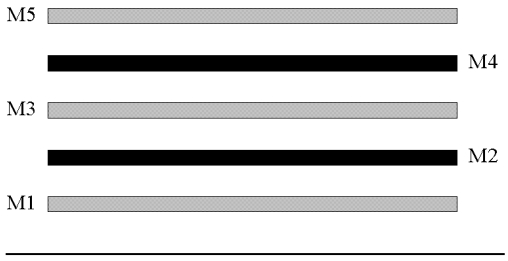

Figure 1: Metal Sandwich Capacitor sideview

Metal layers 1, 3 and 5 are connected together to form one node of the capacitor and layers 2 and 4 are connected to form the other node. The capacitance density of this structure does not scale with shrinking of the technology. We have proposed the following scalable capacitor structures.

2.2. Pillar Capacitor

In the pillar structure, isolated metal pillar columns connected by vias are created with metal levels 2, 3 and 4. These columns are placed at minimum allowed spacings from each other and connected in the pattern shown in a perspective view in Fig.2 to either a large Metal 5 sheet forming one node (A) or Metal 1 sheet forming the other node (B). The pattern is based on surrounding each pillar connected to node A with four pillars all connected to the node B and maximize the periphery for a given area.

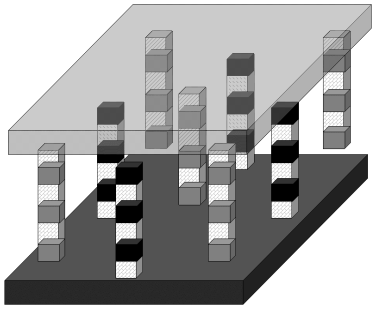

Figure 2: Pillar Capacitor

2.3. Pillar Stripe Capacitor

In another variation of the pillar structure (Fig.3), instead of using one large plate for the top and bottom metals, we use metal stripes along each column to utilize cross-over capacitance in the top and bottom plates and minimize parasitic substrate capacitance. In this way, we also increase the periphery to area ratio in Metal 1. However, the unit pillar section can only consist of Metals 2 and 3. Metals 1 and 4 will be used for the striping as the minimum dimension requirement of Metal 5 is higher than the other metals.

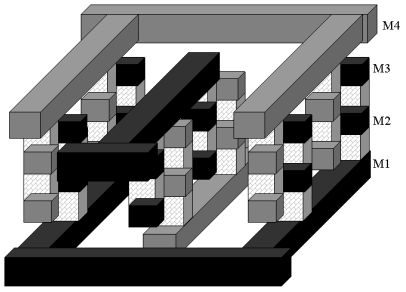

Figure 3: Pillar Stripe Capacitor

2.4. Ring Capacitor

In the ring capacitor (Fig. 4), concentric rectangular rings formed using Metals 1-4 are formed at minimum allowed distance apart. Metal 5 is then used to connect alternate rings to form the 2 nodes of this capacitor. At the point of contact by Metal 5, the 4 metal levels of each ring are connected by means of vias. By using vias to connect the 4 metal levels in each ring all around the ring instead of only at the point where Metal 5 contacts, we can increase the capacitance density ideally by about 20%. This will be called the **Ringvia capacitor.** Rather than having enclosed rings, we can have alternating stripes of metal to derive the IM capacitor shown in Fig. 5.

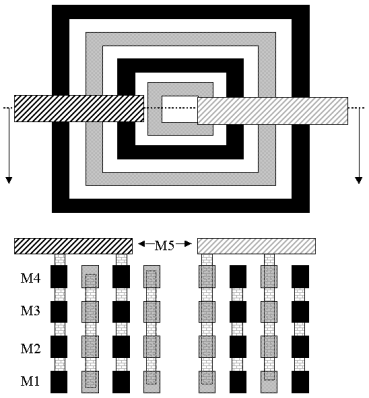

Figure 4: Ring capacitor top /side view

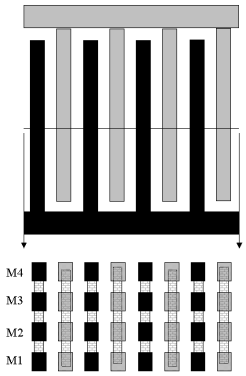

Figure 5: IM capacitor top/side view

2.5. Horseshoe Capacitor

The final structure is the horseshoe structure whose top and side views are shown in Fig. 6. This structure uses a combination of cross-over and metal-to-metal capacitances. By converting the horseshoe structures to stripes, we can derive the Inter-Metal Shuffled capacitor (IMS) shown in Fig. 7.

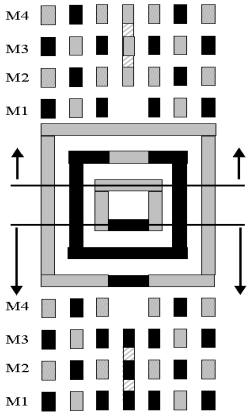

Figure 6: Horseshoe capacitor top and side views

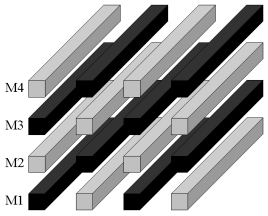

Figure 7: IMS Capacitor

3. MEASUREMENTS

The capacitor chip design which includes de-embedding structures to eliminate the effect of the measurement pads can be tested either as a full 2-port or as a 1-port directly across the capacitors. One chip was fabricated in a 5-level metal, 0.25µm digital CMOS technology developed at the Philips Semiconductors MOS4YOU facility in Nijmegen. The other chip was fabricated in a 5-level metal 0.18µm digital CMOS technology of the same foundry. Here we tested the effects of shielding on an IMS structure along with the effect of scaling.

Low frequency capacitance values measured with a Boonton C-V meter have been used in extracting an RF equivalent circuit for these capacitors to be used in future RF CMOS circuit designs. The difference between measured and extracted capacitance values is attributed to the fact that the process parameters used by the Cadence tool to extract the fringe and cross-over capacitance are not accurate and should be modified.

Table 1: Capacitance densities in 0.25 µm CMOS technology

Capacitor	Extracted (fF/µm^2)	Measured (fF/µm^2)
Sandwich	0.15	0.18
IMS	0.42	0.33
Horseshoe	0.53	0.38
IM	0.34	0.33
Ringvia	0.46	0.40
Pstripe	0.50	0.44

Table 2: Capacitance densities in 0.18 µm CMOS technology

Capacitor	Extracted (fF/µm^2)	Measured (fF/µm^2)
Sandwich	0.22	0.22
IMS	0.59	0.50
Horseshoe	0.69	0.52
IM	0.55	0.55
Ringvia	0.71	0.63
Pstripe	0.69	0.66

The data in Tables 1 and 2 confirms that these novel structures scale with technology and give increased capacitance (increase of 60% going from 0.25 µm to 0.18 µm CMOS technology). The increased capacitance density with scaling is due to narrower interconnect widths and reduced spacing between interconnects for minimum design rules. Single port S-parameter measurements undertaken on the capacitance structures using an HP 8719ES VNA along with air-coplanar Signal-Ground probes from Cascade Microtech indicate that the self-resonance of these structures is higher than our measurement range (10 GHz) and thus are viable for Bluetooth and HiPerLAN applications.

The IMS structure of Fig. 7 has been modified to add a metal 1 shield beneath the structure. Metals 2-5 have been used to realize the capacitance. The results in Table 3 show that the capacitance density is not affected. For the shielded versions, a slightly higher Q is obtained, due to reduced series losses towards the substrate. However, the resonance frequency will drop due to higher parasitic capacitance; the distance from capacitor to shield is smaller than to the substrate. Shielding can be used to reduce the effects of substrate noise on the components. The experiment on shielding was carried out on high resistivity (7 Ohm-cm) substrates, while the remaining experiments have been done on low resistivity (0.01 Ohm-cm) CMOS substrates.

4. CIRCUIT MODELING

We have used the HP Advanced Design system in order to optimize our equivalent circuit representations for all the capacitor structures. The RF signature of the measurement pads have been accounted for and de-embedded from the measurements to focus on the actual structures.

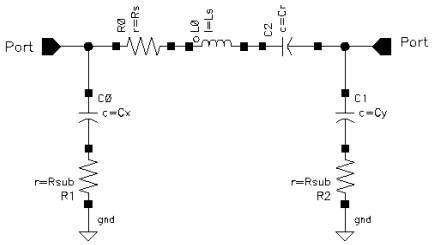

Figure 8: RF Equivalent circuit for capacitor structures

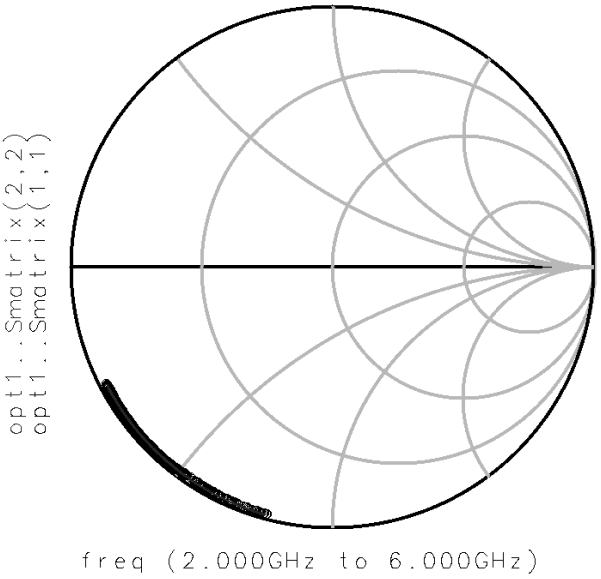

Figure 9: S11 simulated and measured results for the Ringvia capacitor

Shown in Fig.8 is the equivalent circuit representation adopted for these structures. Each capacitor (C_r) is viewed as having a

parasitic resistive (R_s) and inductive (L_s) component in series which will indicate the resonant of these structures.

Moreover, each node of the capacitor has a parasitic capacitance to the substrate (C_x and C_y respectively) in series with a substrate resistance (R_{sub}). The above parameters were optimized with the simulator for each of the structures and the results have been summarized along with the resonant frequencies (ω_o) and Q-factors in Table 4. A very good fit is achieved between measured and modeled S11 values within our frequency range of interest (for Bluetooth and HiPerLAN) as seen in Fig. 9 for one particular structure.

5. CONCLUSIONS

We have presented four novel interconnect based capacitance structures along with their equivalent circuit models, suitable for low power RF applications. Compared to the conventional sandwich capacitor structure, these capacitors provide capacitance densities more than double in 0.25 μm and triple in 0.18 μm CMOS. Their achievable capacitance density increases with scaling of the technology.

ACKNOWLEDGEMENTS

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Table 3: Performances of IMS structures in 0.18 μm high resistivity CMOS technology

Name	Measured C (pF)	Capacitance density ($fF/\mu m^2$)	Resonance Freq, ω_o (GHz)	Measured Q @ 2GHz
IMS_1 with shield	7.5	0.5	10	90
IMS_2 with shield	0.5	0.5	15	100
IMS without shield	1.5	0.5	12	75

Table 4: Extracted equivalent circuit parameters in 0.25 μm CMOS technology

Capacitor	Cr (pF)	Ls (pH)	Rs (Ohms)	Cx=Cy (pF)	Rsub (Ohms)	ω_o (GHz)	*Q @ 2GHz*
Sandwich	2.40	28.0	0.4	0.34	0.20	19.4	82
Pstripe	1.85	16.0	1.4	0.33	0.70	29.3	31
Ringvia	1.86	19.5	0.9	0.33	0.70	26.4	48
IM	2.00	24.0	0.5	0.37	0.60	23.0	80
Horseshoe	1.62	13.5	1.0	0.38	0.75	34.0	49
IMS	1.57	10.0	0.7	0.30	0.70	40.0	72