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Enhanced Multi-Threshold (MTCMOS) Circuits Using Variable Well Bias

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Abstract

Advanced CMOS technology can enable high levels of performance with reduced active power at the expense of increased standby leakage. MTCMOS has previously been described as a method of reducing leakage in standby modes, by addition of a power supply interrupt switch. Enhancements using variable well bias and layout techniques are described and demonstrate increased performance and reduced leakage over conventional MTCMOS circuits.

Keywords

MTCMOS, multi-threshold, variable well bias, leakage control, low power digital circuit design.

1.0 Introduction

Deep sub-micron CMOS technology has enabled increasing amounts of function to be integrated on a single chip to a point where complete systems on a chip are now possible. Excess integration capacity on the silicon die will allow multiple application specific options, with different modes of operation, to be integrated onto a single chip. It is desirable from a system control point of view, for these functions and modes to be selectively enabled by the system software for interfacing with various protocols or performing different tasks defined by the application. This can reduce manufacturing costs by allowing a single part to address multiple applications and markets.

Advanced CMOS technology can also allow very low power operation of battery powered handheld devices by scaling down the supply and device threshold voltages (Vt) to a level which just maintains acceptable performance for a given application [1]. This method achieves low active power, but comes at a cost of increased standby power resulting from increased device leakage from the use of low threshold devices.

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Multi-threshold CMOS (MTCMOS) [2] has been described as a method to reduce standby leakage current in the circuit, with the use of a high threshold MOS device to de-couple the logic from the supply or ground during long idle periods, or sleep states. Figure 1 shows an example of an MTCMOS circuit, where the logic block is constructed using low threshold devices and the either the power supply can be gated by a high threshold header switch, or the ground terminal is gated by a high threshold footer switch.

During active operation of the MTCMOS circuit described by Figure 1, the power interrupt switch is turned on by the SLEEPN (or SLEEP) signal and current dissipated by the logic is drawn through the interrupt switch which causes a reduction in drive voltage seen by the logic, reducing logic performance. To compensate for the reduction in logic performance: larger power supply voltages can be used to at the expense of increased active power for similar performance, larger device widths for the power interrupt switch can be used to minimize performance impact, at the expense of increased area and power for entering and existing sleep mode, and/or adjustments in device implants to allow moderately high threshold values is another technique that can be used to increase performance at the expense of increased device leakage during idle mode.

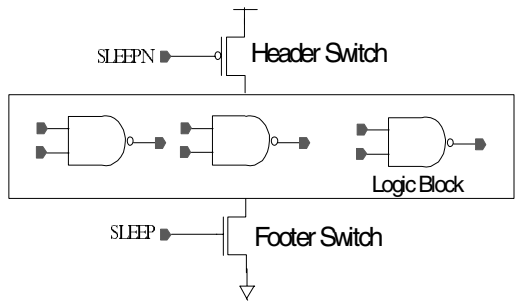

Figure 1 MTCMOS Logic.

This paper examines various options to reduce frequency loss due to the insertion of a power supply interrupt switch by means of layout placement, gate drive and application of device body bias in an ASIC environment.

2.0 Test Circuit

As a way to explore various options for implementing power interrupt switches, a leakage model was constructed to mimic the worst case active power and leakage associated with the logic of a synthesized embedded processor. A leakage model was constructed, using 90% of all the standard cell gates used in a synthesized embedded processor at 1/50th in count. Latches were omitted from the leakage model to simplify the experiment and to isolate affects on logic performance. The distribution of the gate usage is shown in Figure 2. These gates were arranged in eight delay chains which span from 2ns to 4ns in delay (under nominal conditions and supply voltage) to resemble various critical paths in the processor. The logic gates were placed and routed in a 0.18um triple well CMOS technology using low threshold devices with isolated n-wells and p-wells. The threshold voltages defined in this experimental technology were approximately +0.25 and -0.25 V for the low Vt NFET and PFET devices respectively, and +0.7V and -0.65V for the high Vt NFET and PFET devices respectively.

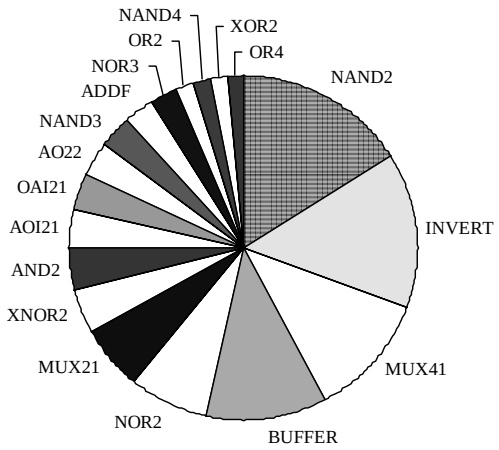

Figure 2 Embedded processor model book usage.

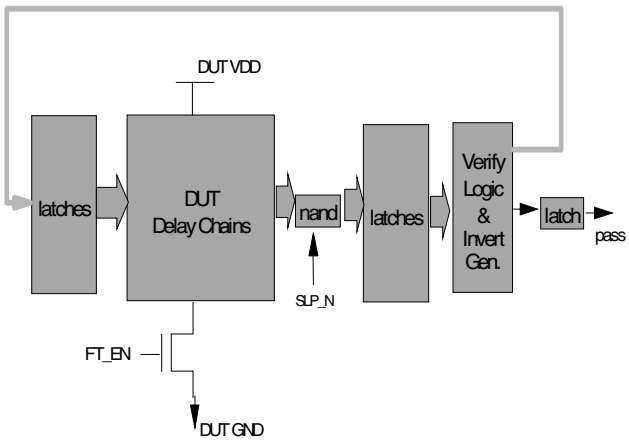

Figure 3 Block diagram of experimental macro.

Figure 3 shows the entire test circuit which includes leakage model (DUT; device under test), a bank of latches to launch data into the DUT, and a bank of latches to capture the outputs of the DUT, along with logic to indicate that all signals propagated within a single cycle. The power/ground supplies and bodies of the latches and support circuits and I/O were isolated from the DUT and placed in separate wells.

3.0 Floorplan

Two layout styles were examined for inserting the power supply interrupt devices, an integrated method and an external ring. Figure 4 shows the integrated method, which places a footer within each standard cell row at the intersection of the M1 virtual ground (VGND) and the global M2 real ground (GND). This method allows sharing current from the logic gates through footer switches within each row. Sizing the footer by parallel placement of footer books can be based on the power density limits specified by the application. Since the footer is placed in each row along side the standard cells, a single common p-well is used for all NFETs within each row, including footers. The same methodology could be extended to PFET header switches, were stripes of n-wells isolate each row of pfets in the gates. A drawback of this method is that density limitations would make it desirable to share the well between the footer device and the switched logic p-wells, adding additional reverse bias to the switched logic during active mode from the voltage drop across the footer device.

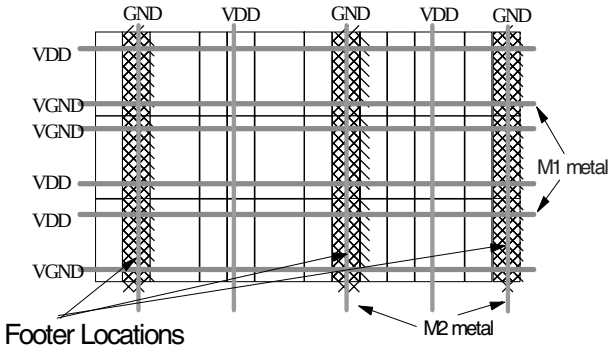

Figure 4 Integrated footer layout.

Figure 5 shows an alternate approach using an external ring for inserting power supply interrupt devices. Here the power distribution grid is interrupted at the M2 and M3 by two rings, the inner ring supplying virtual ground (VGND) and the outer ring connecting to the real ground (GND). The area between the rings can be used for the footer switch. The external ring approach has the benefits of easily allowing the power interrupt switch to be placed in a separate well from the internal logic, enabling separate body connections for the power interrupt switch and the switched logic. This will eliminate increased reverse body bias on the switched logic NFETs, at the expense of complicating p-well contact routing and routing real GND to internal non-switched logic. Another benefit of the external ring approach is that preexisting fixed layout cores can more easily be converted to use a power interrupt switch.

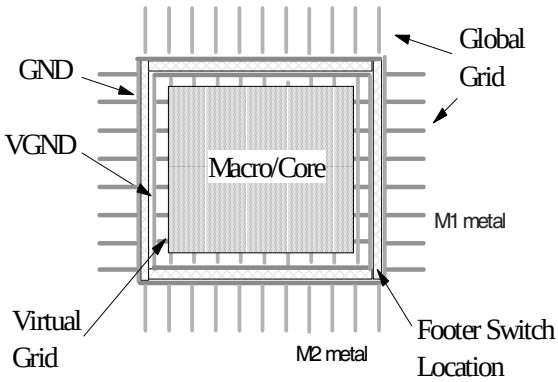

Figure 5 External ring footer layout.

4.0 Simulated Results

Transistor level circuit simulation was used to estimate the leakage of the test circuit along with the size requirements of the header and footer switches. Figure 6 shows the normalized delay increase of the test circuit as a function of footer size as a percentage of total device width in the test circuit for a low Vt footer and a high Vt footer. The simulation was made at 0.9V VDD at 85C. For both low Vt and high Vt footer cases, the delay logic was made using only low Vt devices.

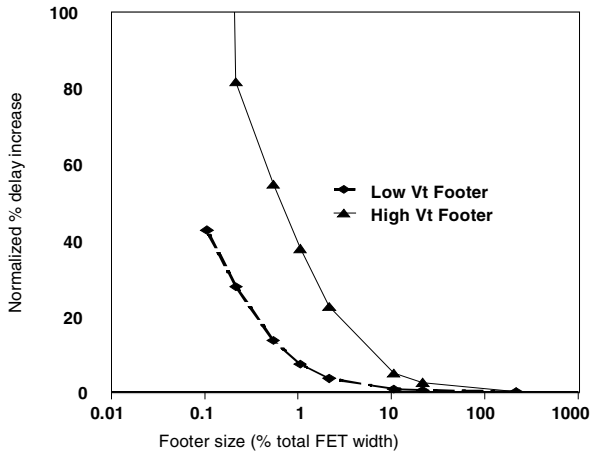

Figure 6 Simulated normalized delay as a function of footer size.

Figure 7 shows leakage of the test circuit as a function of footer device width in terms of percentage of total FET width in the test circuit for 0.9V VDD at 85C. A curve for no footer shows a constant leakage which would result from the circuit without a footer, another curve shows the leakage with a low Vt footer, while the final curve shows the leakage resulting from a high Vt footer. Together, Figure 6 and Figure 7 show the performance and leakage trade-offs possible from choice of footer size threshold voltage.

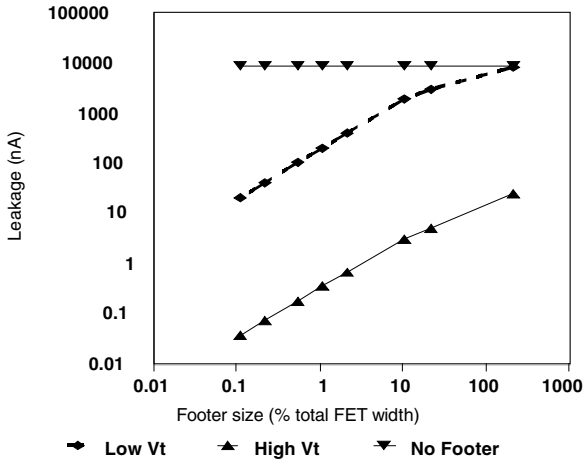

Figure 7 Simulated leakage as a function of footer size.

5.0 Measured Results

Various test circuits were constructed and fabricated to examine integrated and external ring floorplan arrangementsfor power interrupt devices. These test structures also allowed options for separately biasing the bodies of the power interrupt switches with respect to the switched logic. All test measurements were done at room temperature with a 0.9V power supply (unless where noted differently). Floorplan experiments were done using footer devices to interrupt the GND terminal. All gates in the load DUT circuit were constructed with low Vt FETs. Both the integrated and external ring footers used the same effective device width, at 2% of the total NFET and PFET width of the leakage model. Experiments incorporating a header device (VDD interrupt) used a PFET sized at 3.5% of the total NFET and PFET width. These sizings were chosen to minimize frequency impact and for equal footprint of NFET footers and PFET headers created by parallel intantiation of standard cell books.

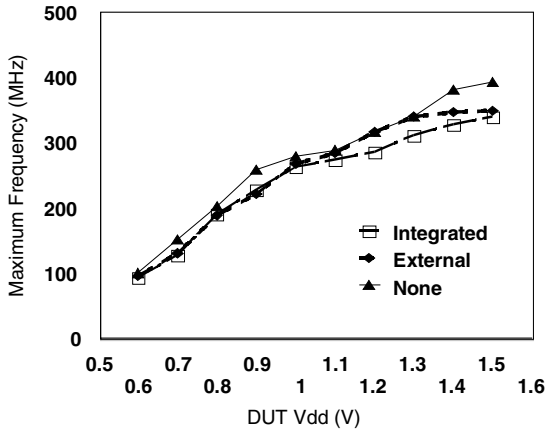

Figure 8 Low Vt footer measured performance.

Figure 8 shows the maximum frequency where the all delay paths completed within a single cycle using a low threshold NFET devices as a ground interrupt device (footer) with an integrated layout method, an external ring method and no footer (none), as a function of DUT supply voltage.

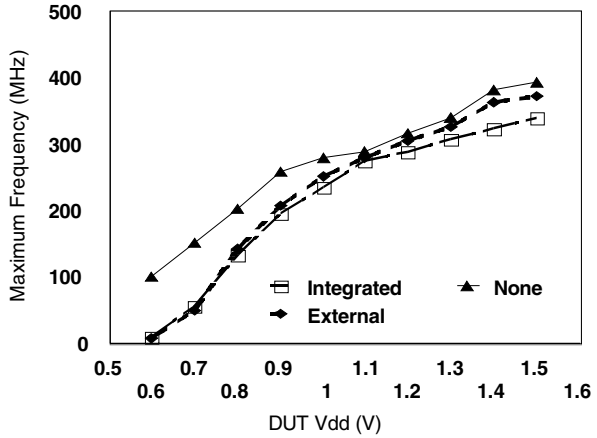

Figure 9 High Vt footer measured performance.

Figure 9 shows measured results for the same circuits, except using high threshold footer devices. The performance penalty for using a footer device can be seen clearly from the difference in performance between the figures. These figures also show a slight decrease in performance penalty using the external footer as opposed to the integrated footer. This can be attributed to decreased reverse body affect from using external footer since it was placed in an isolated p-well from the switched logic NFETs. Also, the virtual ground is more fully connected using the external footer as opposed to the integrated footer, since the external ring footer has M1, M2 and M3 connections for VGND, allowing more sharing paths between the switched logic and footer devices.

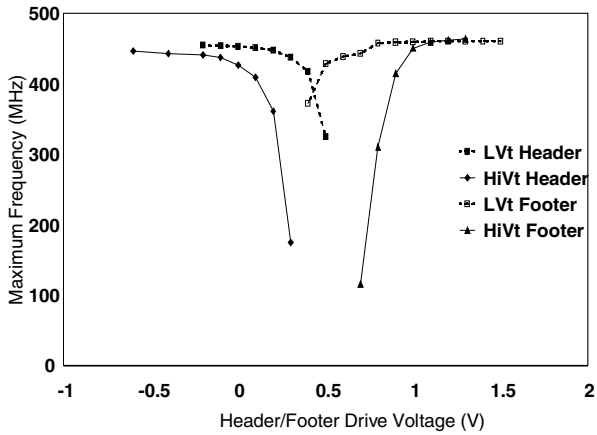

Figure 10 Header/Footer overdrive response.

Figure 10 shows the maximum attainable performance as a function of supply voltage for both high Vt headers and footers for different values of header/footer drive voltages. This method of overdriving the header or footer switch with a large gate drive is described in [3] as a way of reducing the performance penalty of MTCMOS. These measurements were done with VDD and all PFET n-well voltages at 0.9V. As can be seen from Figure 10, additional header or footer overdrive voltages can restore performance lost from using a high Vt device for the power supply interrupt.

Figure 11 shows the effects of n-well bias on a test macro incorporating an external ring connected high Vt header. The test was run with a 0.9V supply voltage. The plot also shows the performance improvement from forward bias of the header n-well. As can be seen from the plot, approximately an additional 5% performance increase can be accomplished by forward biasing the header n-well with respect to the switched logic n-well. The forward bias effect is limited by increase in leakage current as the well diode begins to conduct in forward bias mode.

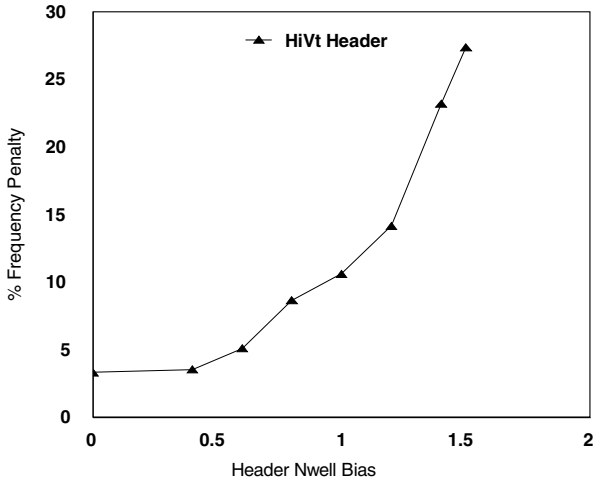

Figure 11 High Vt Header n-well bias effects on leakage and performance.

Figure 12 shows measured standby leakage of the test macro with the high Vt header along side a macro utilizing a low Vt header switch. The nominal n-well body voltage and DUT VDD for the switched logic is set at 0.9V. Figure 12 shows that comparable leakage performance can be achieved using a low Vt device with reverse body bias as with a very high Vt device without body bias. A low Vt PFET header can allow better performance and lower active power over a high Vt header device, and by applying a large reverse body bias to the header during standby state, similar leakage characteristics can be achieved. The header made using the high Vt device shows that the leakage can be reduced by almost 100x by reverse body bias, being limited by GIDL (gate induced drain leakage) [4] effects resulting from large reverse bias voltage.

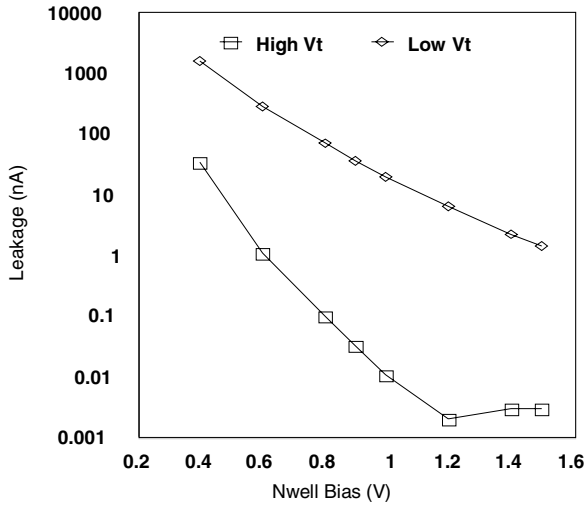

Figure 12 Leakage as a function of n-well body bias for Low Vt and Hi Vt header devices.

Figure 13 shows the measured standby leakage of the test macro utilizing a low Vt footer and a high Vt footer with variable pwell bias. The test was also done at room temperature and 0.9V VDD. During nominal pwell bias at 0V, the high Vt footer offers approximately 1000x reduction in leakage, while under reverse bias of the footer switch, the leakage advantage from the increased Vt is diminished by the increased GIDL seen in the high Vt nfet device. Figure 13 shows that the GIDL effect on the leakage is more severe in the high Vt NFET then the high Vt PFET. The figure also shows a low Vt footer device at -1V pwell bias can achieve lower leakage then a high Vt footer at the same well bias.

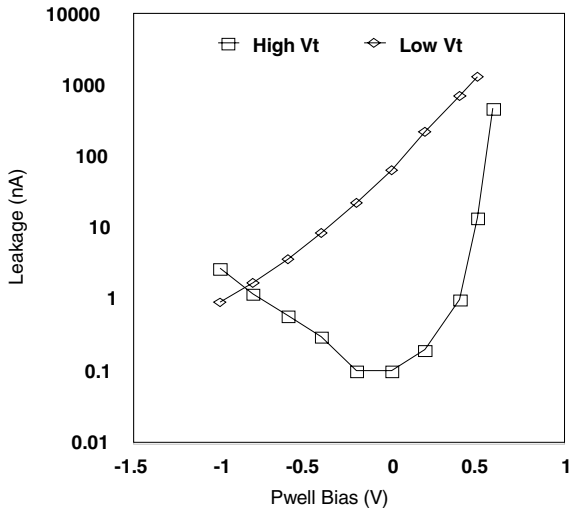

Figure 13 Leakage as a function of p-well body bias for Low Vt and Hi Vt footer devices.

6.0 Conclusion

Two methods for constructing power supply interrupt switches for leakage control were described. Measured results suggest that the externally connected ring floorplan with the power supply interrupt switch placed within an isolated well, can offer slightly improved performance over an integrated layout. The isolated well can also allow a separate well bias for the power supply interrupt switch, allowing variable threshold operation of the header or footer switch by the use of well bias. Measured results on fabricated wafers show that variable well bias can serve as an effective method to reduce performance degradation associated with MTCMOS and enhance leakage control during standby mode. Use of a reverse bias on the power supply interrupt switch, constructed with a low Vt device, during sleep mode can allow substantial leakage reduction without the expense of adding a high threshold device. Likewise, adding a forward bias to the power supply interrupt switch during active mode of operation will reduce the performance penalty associated with MTCMOS. The application of boosted gate drive was also shown as a an method for increasing performance in MTCMOS.

7.0 References

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