A 60dB, 246MHz CMOS Variable Gain Amplifier for Subsampling GSM Receivers

Mohamed A.I. Mostafa
Texas A&M University
Electrical Engineering Dept.
College Station, TX 77843
(979) 845-5900
moh_mostafa@ieee.org

Sherif H.K. Embabi
Texas Instruments Inc., Wireless
Communications Business Unit
Dallas, TX 75243, USA
(214) 480-2633
s-embabi1@ti.com

Mostafa A.I. Elmala
Texas A&M University
Electrical Engineering Dept.
College Station, TX 77843
(979) 845-5900
Mostafa@ee.tamu.edu

ABSTRACT
This VGA is designed for a GSM subsampling receiver. It operates at an IF frequency of 246MHz. The VGA provides a 60dB digitally controlled gain range in 2dB steps. The VGA is implemented in a 0.35µm CMOS process. The current is 9mA@3V. The overall gain accuracy is less than 0.3dB. The noise figure at maximum gain is 8.7dB. The IIP3 is –4dBm at minimum gain.

Categories and Subject Descriptors
1.3 [**Analog, MEMS and Mixed Signal Electronics**]: RF circuits, Wireless systems, and mixed-signal circuits.

General Terms
Performance, Design, Experimentation, Standardization.

Keywords
VGA, CMOS, subsampling, GSM, IF, receiver.

1. INTRODUCTION
Variable gain amplifier (VGA) circuits are employed in many applications in order to maximize the dynamic range of the overall system. VGA circuits are often employed in imaging circuits [1], hearing aids [2], disk drives [3], and in virtually all wireless communication systems [4]. The automatic gain control (AGC) loop is needed in wireless systems since the received signal power of all communication systems has a wide dynamic range. In order to keep the communication systems working under these conditions, a VGA is typically employed in a feedback loop to realize the AGC circuit, whose output signal has a fixed magnitude for different input signal strengths..

2. SYSTEM SPECIFICATIONS
The power and noise figure (NF) budgets for the 1.8GHz GSM subsampling receiver is shown in Fig. 1. The specifications of the VGA were derived based on the shown gain and noise figure distribution. The major challenge posed by subsampling is noise folding. This folded noise is typically dominated by that of the VGA, assuming that a high-Q IF BPF precedes the VGA. This puts severe constraint on the VGA noise figure. Assuming that the gain and NF of the RF front-end are 17dB and 6dB, respectively, thus the maximum gain of the VGA must be 45dB and the NF_{max_gain} not to exceed 15dB. To relax the image rejection requirements, an IF of 246MHz was chosen. To relax the linearity constraint of the sample and hold and to reduce the ADC dynamic range, a 60dB gain range was chosen for the VGA. Similar specifications have been realized using a BiCMOS technology consuming 12mA @3.6V [5]. This paper reports on a VGA implementation in a digital CMOS process, which meets all the above requirements.

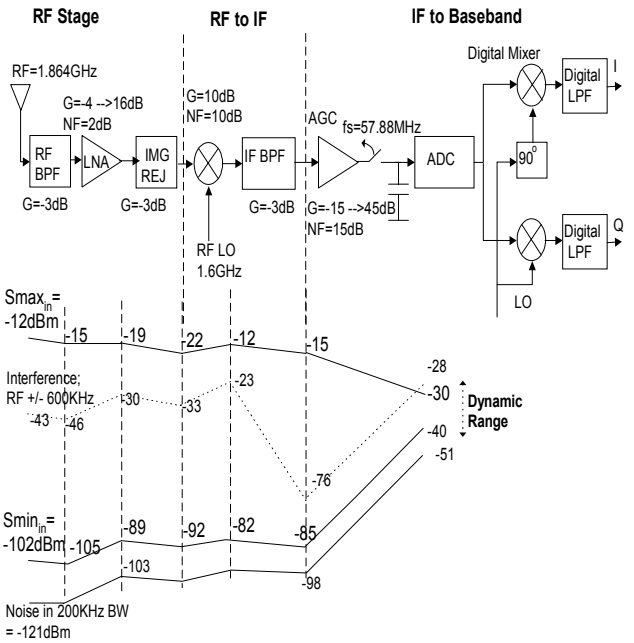

Fig. 1. Power and NF budget of the receiver.

3. CIRCUIT IMPLEMENTATION
The VGA is designed as a three-stage cascaded amplifier to achieve large dynamic range and large bandwidth. Each stage has –5dB to 15dB gain range as shown in Fig. 2. The structure of each stage is optimized for both noise and linearity. This gain

ISLPED'01, August 6-7, 2001, Huntington Beach, California, USA.

distribution is chosen mainly to enhance the total noise figure of the VGA. The noise factor of 3 stages VGA is given by:

$$f_{Tot} = f_1 + \frac{f_2 - 1}{G_1} + \frac{f_3 - 1}{G_1 G_2}, \quad (1)$$

where f_i, and G_i are the noise factor and the gain of stage i, respectively. It is clear from this equation that a large gain in the first stage will reduce the noise figure of the whole VGA.

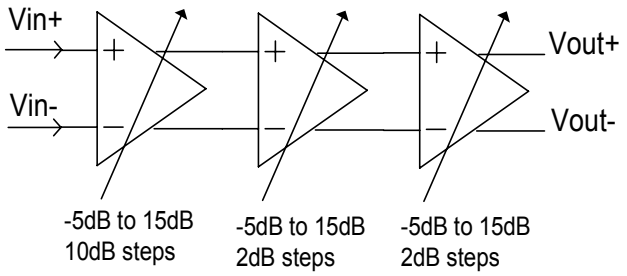

Fig. 2. VGA three-stage amplifier structure.

In addition, while changing the gain, the strategy is to keep the first stage gain always maximum all over the higher 40dB gain range of the total 60dB dynamic range. Only when the signal is large enough that the noise figure of the VGA would not be critical to the performance of the receiver, the gain of the first stage could be changed to a lower value. Moreover, for very large signal, the attenuation in the first stage will enhance the linearity of the VGA and will increase the total IP3.

3.1 DEGENERATION STRUCTURE

In order to get high precision gain steps and good linearity, fully differential degeneration VGA structure was employed. The basic degeneration differential amplifier is shown in Fig. 3. The differential input voltage signal is converted to a differential current through the transconductance of the degenerated differential pair, which is given by:

$$gm_{diff} = \frac{gm_1}{1 + gm_1 * \frac{R_d}{2}} \quad (2)$$

Therefore, the gain of this stage is:

$$Gain = \frac{R_L}{\frac{R_d}{2} + \frac{1}{gm_1}} \quad (3)$$

By changing the ratio of the load and degeneration resistors, this circuit can provide both amplification and attenuation. However, to achieve high precision, it is desirable for the gain to be only a function of the ratio of resistor values. Therefore, the gm boosting circuit, shown in Fig. 4 [6], was used to minimize the contribution of gm to the gain. The gm will be boosted by the gain of the feedback circuit and can be written as:

$$gm_{eff} = gm_2(1 + gm_3 R_{oA}) \quad (4)$$

where R_{oA} is the output impedance at node A.

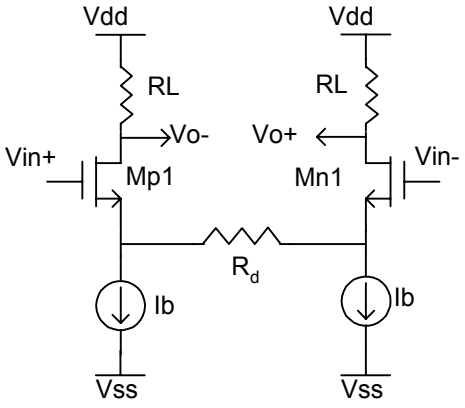

Fig. 3. Basic degeneration differential pair.

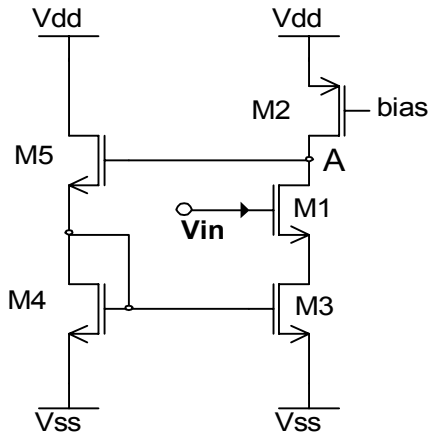

Fig. 4. gm boosting circuit.

3.2 FIRST STAGE OF THE VGA

The first stage is implemented as a low noise, pseudo-differential common gate structure to reduce the total noise figure of the VGA and is shown in Fig. 5. It utilizes a gm boosting circuit as the one shown in Fig. 4, to reduce the input impedance to near 50 Ω. Thus, it does not need any input matching network. The main gm boosting circuit consists of transistors Mn_{b1} (Mp_{b1}) through Mn_5 (Mp_5), with the gm of transistor Mn_2 (Mp_2) being the one to be boosted. The gain is digitally controlled using a bank of transistors (Mn_{b1} to Mn_{bk}, and Mp_{b1} to Mp_{bk}) which is controlled by switches B_1 to B_k. The gain of the first stage is given by;

$$Gain_1 = 2gm_{n2}Ro_1, \quad (5)$$

where Ro_1 is the output impedance at node o_1.

Since the NF of the first stage is critical, two cross-coupled capacitors C1 and C2 are connected as shown in Fig. 5. [7]. This was found to greatly enhance the noise figure of the common gate structure. The cross coupling capacitors cause the noise of both Mp_2 and Mn_2 to appear as a common mode noise current at the drain node of both transistors. Thus in the differential mode their noise will be significantly reduced, which in turn reduces the noise figure of the common gate structure.

Finally, the outputs of the first stage are buffered using two source follower amplifiers, which are made of the same gm boosting circuit shown in Fig. 4. The enhanced gm source follower achieves a bandwidth of 300 MHz for a 5pF load.

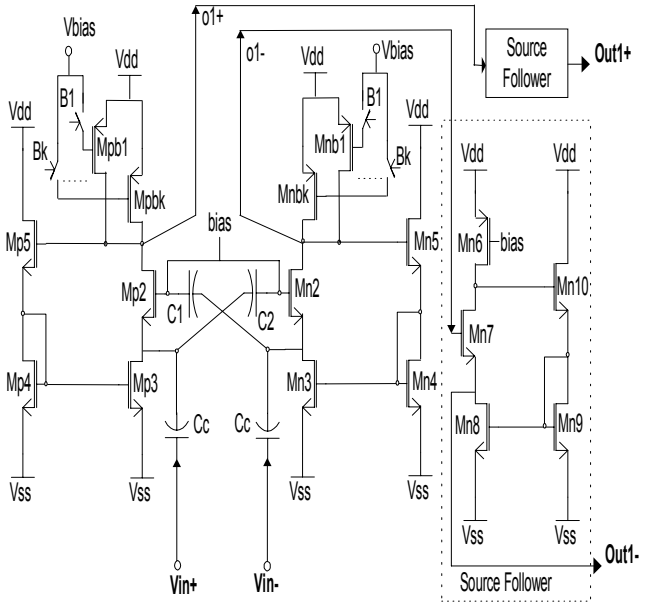

Fig. 5. First stage of the VGA.

3.3 SECOND AND THIRD STAGES OF THE VGA

The last two stages are identical. Their schematic is shown in Fig. 6. They use degenerated differential pair with gm boosting circuit as the one shown in Fig. 4. The output current of the gm boosting circuit is mirrored from Mn_{14} (Mp_{14}) to Mn_{16} (Mp_{16}) and is converted to voltage through the load resistor RL. A degeneration resistor (R_d) is connected between the two sources of Mp_{12} and Mn_{12} of the differential pairs.

To change the gain, it is more desirable to change the degeneration resistor, R_d, to maintain a constant bandwidth throughout all the gain stages. However, in previous work, changing the degeneration resistors limited the gain dynamic range to 12dB [6]. Moreover, if used with a higher dynamic range VGA, it can cause stability problem [8]. Another method to change the gain is to change the current mirror ratio to the output, however, this was found to dramatically degrade the bandwidth of the VGA due to the large capacitance from the array of the current mirrors.

In order to obtain a large dynamic range, large bandwidth, good stability, and high precision gain for the VGA, a degeneration resistor, RL_d, is used between the output nodes as shown in Fig. 6. This does not affect the stability of the VGA nor its minimum bandwidth (which will be only limited by the main load resistor). Moreover, it can be used to achieve larger gain range and relax the design of the common mode feedback circuit. Although, the resistor array architecture is the most commonly used approach for gain control, the use of a switch in series with a resistor will limit the accuracy of the VGA due to the error caused by the finite resistance of the MOS switch. A large width MOS switch can be used, however, the large parasitic capacitance of the switch will limit the bandwidth. Hence, to overcome this trade off, the whole output branch, which includes the cascode transistors (Mn_{17}, and Mp_{17}, (or Mn_{18} & Mp_{18})), the load resistors, and the degeneration resistor, is selected through the cascode transistors (which act as switches), as shown in Fig. 6. Moreover, the switch can now have minimum width. This technique provided satisfactory results in terms of both accuracy and bandwidth.

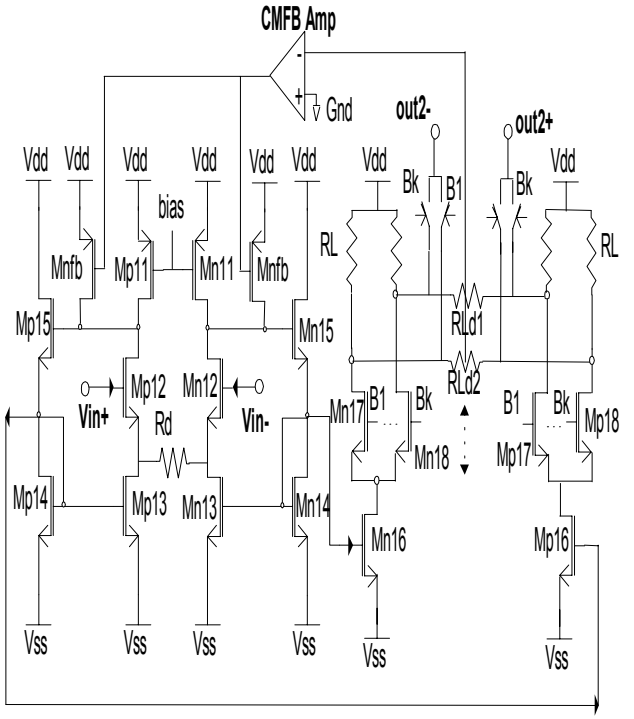

Fig. 6. Stage two (or three) of the VGA.

The gain is accurately set by the ratio of the parallel combination of the load resistor and the output degeneration resistor ($RL//RL_{di}$) to the degeneration resistor ($Rd+1/gm_{12}$) of the input stage. The gm boosting circuit is employed to minimize the dependency of the gain on the transconductance of Mn_{12} and Mp_{12} (gm_{n12} and gm_{p12}). The gain is given by:

$$\text{Gain}_2 = N \frac{RL \,//\, \frac{RL_d}{2}}{\frac{R_d}{2}} \qquad (6)$$

where N is the current mirror gain from Mp_{14} (Mn14) to Mp_{16} (Mn16).

It is worth noting that using the degeneration resistance between the output nodes for gain selection does not affect the operation of the common mode feed back circuit, as it does not change the biasing of the circuit because the load resistor does not changes. This also enables stage 2 and 3 of the VGA to be directly coupled without coupling capacitor nor DC biasing circuit, saving needed current and bandwidth.

Finally, The output of the third VGA stage is buffered by a source follower similar to the one used in the first stage for good isolation and bandwidth enhancement. Moreover it enables the output to be tested off-chip without the need for a matching circuit since the gm boosting circuit can be adjusted to give 50Ω

output impedance. Thus reducing the number of off-chip components.

3.4 COMMON MODE FEEDBACK

The RL_d, is made up of two series resistors each equal $\frac{RL_d}{2}$. The point where the two resistors are connected is used to sense the CMFB voltage. This voltage is fed back through a differential OPAMP as shown in Fig. 6. It is compared to the ground signal, which is the middle voltage between the two supplies to give maximum output swing. The output of the feedback OPAMP is used to adjust the biasing current through the two transistors, Mn_{fb}, and Mp_{fb}. The feedback OPAMP is a conventional two-stage amplifier with 40dB gain and 70^0 phase margin and is shown in Fig. 7.

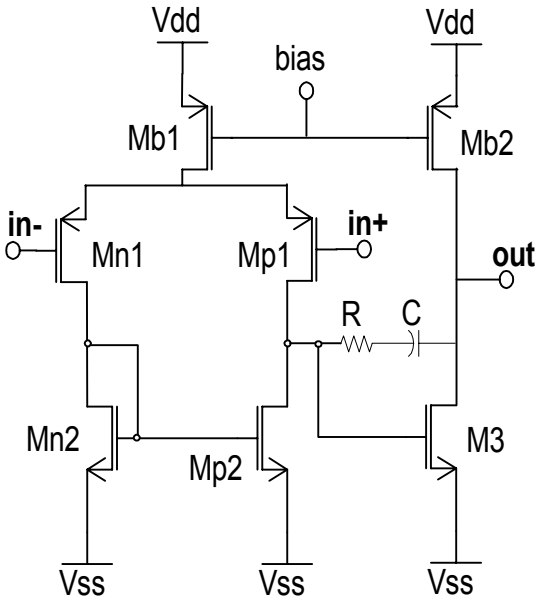

Fig. 7. Common mode feedback OPAMP.

4. MEASUREMENTS RESULTS

The proposed VGA was fabricated in TSMC's 0.35µm CMOS process occupying 0.64mm^2. A chip micrograph is shown in Fig. 8. A gain range from –15dB to 45dB was measured in 2dB steps. The accuracy in the gain steps was 0.3dB. The VGA operates at 246MHz with gain variation of ±0.2dB over a 10MHz band.

The noise figure is measured to be 8.7 dB at the maximum gain of 45dB, and 30dB at the minimum gain of –15dB. Such low NF was achieved at a high frequency in a digital 0.35µm CMOS process. It is very interesting to notice that the noise figure changes only by 22dB as the gain varies by 60dB. This will satisfy noise specification for any signal above the sensitivity of the GSM (-102dBm). Fig. 9 shows both the maximum gain and 2dB step below and their corresponding noise figures, while Fig. 10 shows maximum and minimum gains and their corresponding noise figures.

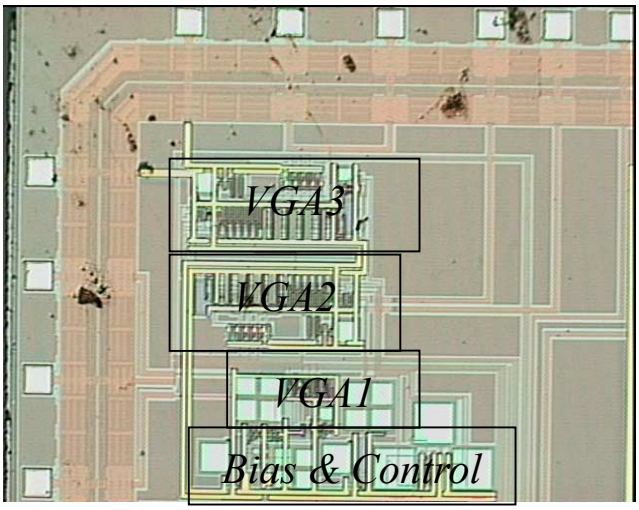

Fig. 8. Chip micrograph.

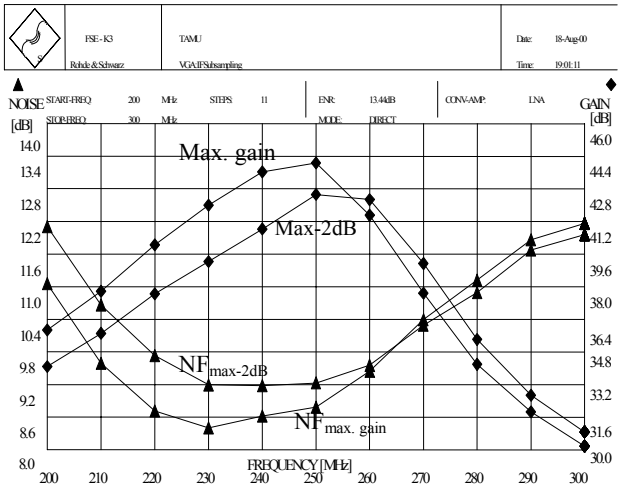

Fig. 9. VGA maximum gain & NF and 2dB below.

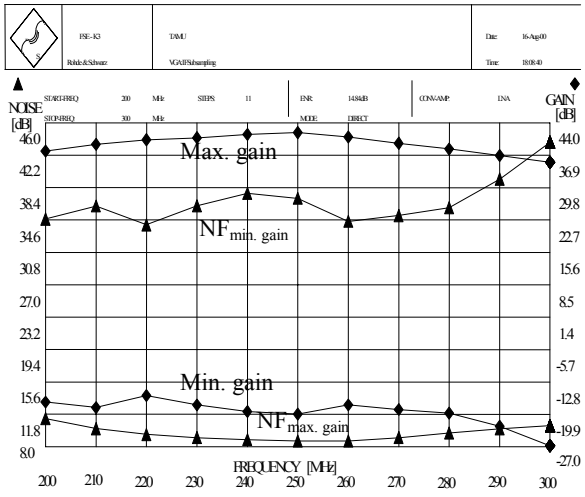

Fig. 10. VGA maximum and minimum gains & NF.

A two-tone test was used to measure the IP3 of the VGA. The measurement result for the minimum gain is shown in Fig. 11. An IIP3 of –4dBm was measured for the minimum gain as shown in Fig. 12, and a -1dBm OIP3 for the maximum gain.

As the maximum signal power at the output of the VGA is required to be around –25dBm, the measured IP3 for the VGA satisfies the specification with enough safe margin.

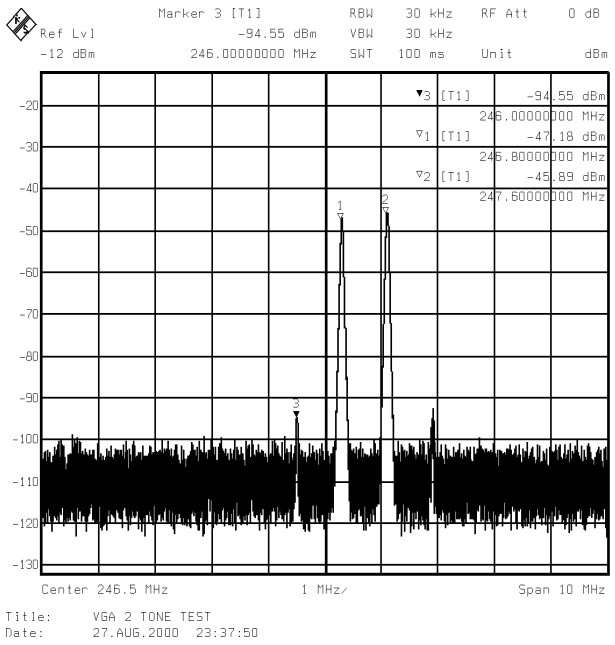

Fig. 11. Two-tone test for the VGA at minimum gain.

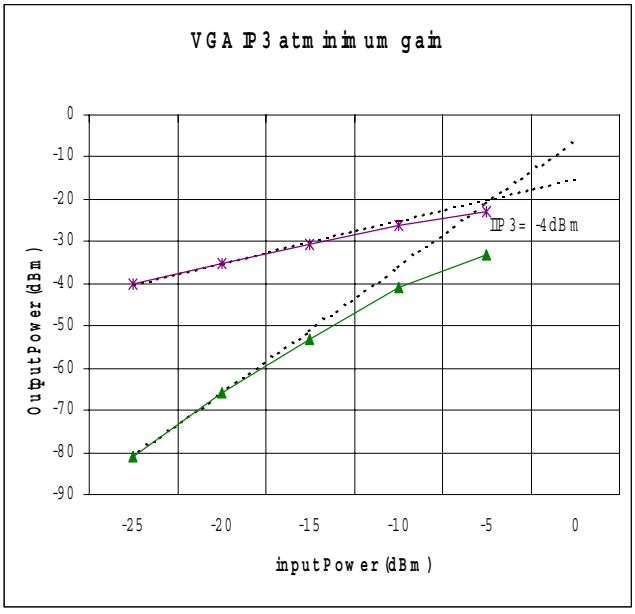

Fig. 12. IP3 curve for the VGA at minimum gain.

A group delay of 1.5ns was measured over a 5MHz band centered at 246MHz as shown in the network analyzer result of Fig. 13. This implies that the proposed VGA may be usable for 3G applications where the channel bandwidth is around 5MHz.

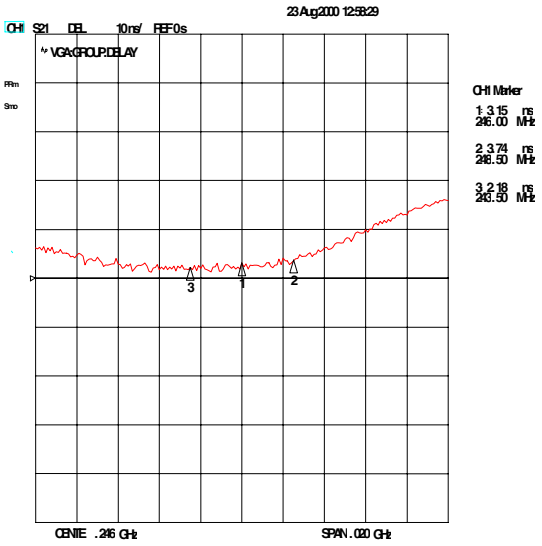

Fig. 13. Group delay at 5MHz span around 246MHz.

To show the advantage of choosing a common gate structure for the first stage of the VGA to eliminate the need for an input matching network, S11 measurement is shown in Fig. 14. It is clear that at the IF frequency of 246 MHz, the input impedance is very close to 50Ω without any matching circuit.

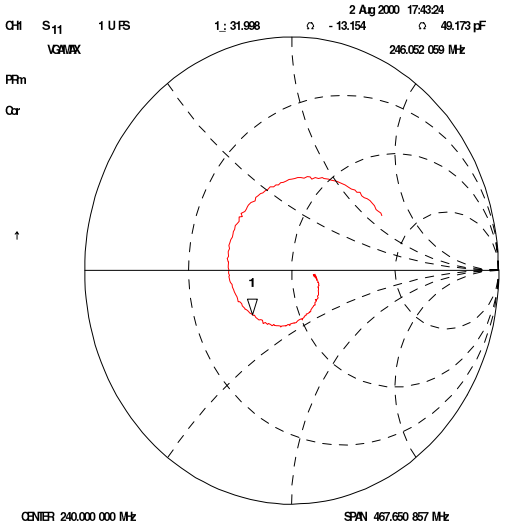

Fig. 14. S11 measurement for input matching check.

Table 1 shows the required specifications and the corresponding measurement results.

Table 1. Specifications vs. measurements.

	Specifications	Measurements
Freq. of operation	246MHz	246MHz
Dynamic range	-15dB to 45dB	-15dB to 45dB
Noise figure	<15dB	8.7dB
Gain step	2dB	2dB
Gain accuracy	<0.4dB	0.3dB
OIP3 @max. gain	>-7dBm	-1dBm
IIP3 @min. gain	>-6dBm	-4dBm
Current	small	9mA
Group delay	<5ns [5MHz]	1.5ns [5MHz]
Matching	50Ω	32Ω

5. CONCLUSION

A low noise VGA that is designed for a GSM subsampling receiver was presented. The VGA was implemented in a digital 0.35µm CMOS process and it operates at an IF of 246MHz with 60dB dynamic range. The noise figure at maximum gain of 45dB is 8.7dB. The current is 9mA@3V. The overall gain accuracy is less than 0.3dB. The IIP3 at minimum gain is –4dBm and the OIP3 is –1dBm at maximum gain. The performance of the proposed VGA puts it as a strong candidate for 3G applications.

6. REFERENCES

[1] A. Motamed, C. Hwang, and M. Ismail, "A low-voltage low-power wide-range CMOS variable gain amplifier," IEEE Trans. Circuits Syst. II, vol. 45, no. 7, pp. 800-811, July 1998.

[2] J. Duque-Carrillo, et al., "VERDI: an acoustically programmable and adjustable CMOS mixed-mode signal processor for hearing aid applications," IEEE J. Solid-State Circuits, vol. 31, pp. 634-645, May 1996.

[3] R. Harjani, "A low-power CMOS VGA for 50 Mb/s disk drive read channels," IEEE Trans. Circuits Syst. II, vol. 42, pp. 370-376, June 1995.

[4] M. Mostafa, H. Elwan, A. Bellaour, B. Kramer, S. Embabi, "A 110 MHz 70 dB CMOS variable gain amplifier," IEEE Int. Symp. on Circuits and Syst., vol. 2, pp. 628-631, May 1999.

[5] G.S. Sahota, and C.J. Persico, "High dynamic range variable-gain amplifier for CDMA wireless applications," ISSCC Dig. Tech. Papers, pp. 374-375, Feb. 1997.

[6] J. Rijns, "CMOS low distortion high-frequency variable gain amplifier," IEEE JSSC, vol. 31, no. 7, July 1996.

[7] W. Zhou, S. Embabi, J. Gyvez, and E. Sanchez-Sinencio, "Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixers," ESSCIRC Dig. Tech. Papers, pp. 116-119, Sept. 2000.

[8] E. Ibaragi, A. Hyogo, and K. Sekine, "A design technique of the CMOS circuit with a very low impedance terminal for stability," IEEJ, 2nd Analog VLSI Workshop Proc., pp. 51-56, June 1998.