A 1 V, 1.9 GHz Mixer Using a Lateral Bipolar Transistor in CMOS

Song Ye
University of Toronto
10 King's College Road
Toronto, Ontario, M5S 3G4, Canada
1-819-776-2848
yesong@vrg.utoronto.ca

Koji Yano
Yamanashi University
Takeda-4, Kofu
Yamanashi 400-8511, Japan
81-55-220-8474
yano@esd.yamanashi.ac.jp

C. Andre. T. Salama
University of Toronto
10 King's College Road
Toronto, Ontario, M5S 3G4, Canada
1-416-978-8658
salama@vrg.utoronto.ca

ABSTRACT

This paper describes a low power mixer implemented in a standard 0.25 um CMOS process. The mixer uses lateral bipolar transistors in CMOS to form the core of the circuit. No additional processing steps are needed to obtain the BJT when the MOSFET is properly designed. The mixer exhibits 6.5 dB gain, operating at 1.9 GHz from a 1 V supply and a power dissipation of 1.3 mW. Such a mixer is a likely candidate for low power portable wireless applications.

Categories and Subject Descriptors

1.3 [**Analog, MEMS and Mixed Signal Electronics**]: RF circuits, Wireless systems, MEMS circuits, AD/DA Converters, Mixed-signal circuits, DC-DC conversion.

General Terms

Measurement, Design, Experimentation.

Keywords

RF, CMOS, mixer, lateral bipolar transistor, low power.

1. INTRODUCTION

Presently, the dominant technology for commercial RF front ends is advanced bipolar junction transistor (BJT) [1]. However, the demand for low cost implementations is driving the integration of RF building blocks into a digital CMOS process. Unfortunately, the performance of CMOS RF building blocks is limited by the low transconductance and low cutoff frequency of the MOSFET.

BiCMOS offers a combination of both bipolar and CMOS devices, however BiCMOS requires additional mask layers and increased process complexity, which translate into lower yield and higher costs as compared to standard CMOS process.

Circuit designers have come to realize that bipolar transistors inherent in submicron CMOS devices can be used to enhance circuit performance because of their high transconductance and cutoff frequency [2-7]. Since this approach requires no modification of the process, it is a cheap, widely applicable and relatively simple alternative. An amplifier using this approach has been reported [6]. A mixer using a BiCMOS gate-controlled lateral PNP transistor has also been proposed [7], however, it was limited to relatively low frequency (400 MHz). The lateral bipolar transistor is also referred as CLBT (compatible lateral bipolar transistor) [5].

This paper describes a 1.9 GHz mixer implementation using a lateral BJT inherent in a 0.25 um bulk CMOS technology and illustrates the applicability of this approach for RF applications.

2. LATERAL BIPOLAR TRANSISTOR

As illustrated in Figure. 1, inherent in a CMOS p channel device are lateral and vertical pnp parasitic bipolar transistors. The source drain and channel region of the p-MOSFET serve respectively as the emitter, collector and base of the lateral bipolar device. The vertical bipolar transistor is formed by the p^+ source acting as the emitter, the n-well acting as the base and the p-substrate acting as the collector. The vertical transistor can usually be ignored due to its very low current gain. In the bias condition given in this paper, the current ratio of lateral transistor to vertical transistor is about 60.

The objective of this paper is to make use of the lateral pnp parasitic bipolar (LPNP) in the mixer design.

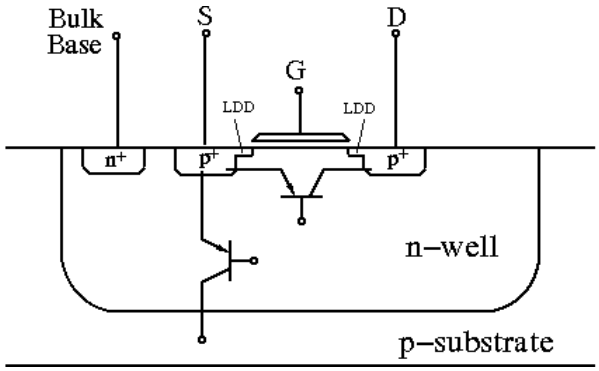

Figure 1. The lateral and vertical bipolar transistors inherent in a p-MOSFET.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.

ISLPED'01, August 6-7, 2001, Huntington Beach**,** California, USA.

Copyright 2001 ACM 1-58113-371-5/01/0008…$5.00.

3. TOPOLOGY OF THE MIXER

The topology of the mixer is shown in Figure. 2. A p-MOSFET with an inherent LPNP P1 is used as a four terminal device. The RF input signal V_{RF} is applied to the gate of the MOSFET and LO signal V_{LO} is fed to the base of the LPNP. The IF output signal Vout output is accessed from the drain. V_{G1} , V_{B1} and Vdd are the bias and supply voltages respectively. The n-MOSFET M2 acts as an active load and the conversion gain of the mixer can be adjusted by changing its gate voltages V_{G2} . L_S is used to shift the ac voltage level at the source of M1 and creat coupling between the two devices.

The small signal equivalent circuit of the mixer is shown in Figure. 2 (b). Vgs is the signal voltage across Zg which is the impedance associated with the gate of M1, gm is the transconductance of M1, Z_S is the impedance of L_S , β is the current gain of P1 and Z_b is the impedance associated with the base of the LPNP. To simply the circuit, the n-MOSFET is replaced by a resistor R_L . V_S is the voltage at the source of the M1.

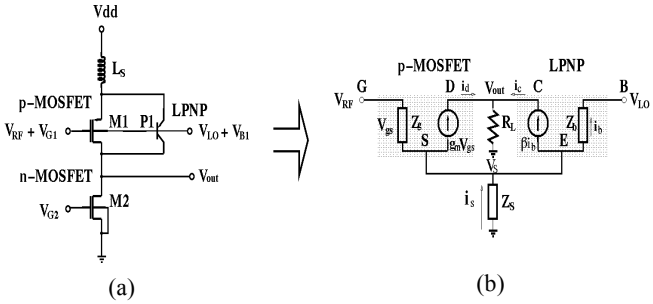

Figure 2. Configuration of the mixer (a) and its small signal model (b).

M1 should be biased in the saturation region where the gate voltage can control the source to drain current. P1 must be biased in the active region so that a small variation of the base voltage can result in a large variation in the collector current βi_b and thus vary V_S effectively by changing the current flowing through L_S . Since M2 is used as a resistive load, it must be biased in the triode region.

4. LPNP DEVICE CHARACTERIZATION

Characteristics of the LPNP bipolar transistor was carried out using 2-D ISE simulation and experimental measurement was performed on the device cell structure shown in Figure. 3. Each cell consisted of five parallel channels (L=0.5 um, Wcell =6.25 um). The RF performance of the transistor can be improved if more body contacts are placed closer to more of the active part. The layout of the device made out of parallel cells using a channel length of 0.5 um and a channel width of 438 um is illustrated in Figure 4.

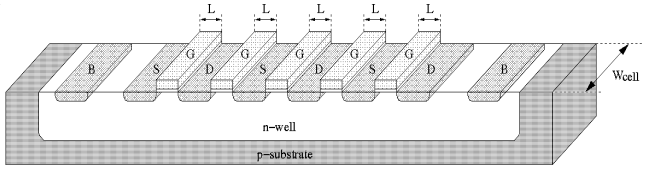

Figure 3. Cell structure of the p-MOSFET (L=0.5um, W_{cell}=6.25um)

Figure 5 shows the experimental source to drain current I_{SD} versus source to bulk voltage V_{SB} as a function of the gate to source voltage. It indicates that the LPNP contributes the dominant component of I_{SD} when V_{SB} is larger than 0.7 V where the LPNP is in active region. In the region where V_{SB} is smaller than 0.7 V, I_{SD} is mainly controlled by V_{GS} . The circled region identified in the diagram is ideal for mixer operation because both V_{SB} (or V_{BE}) and V_{GS} have significant effect on I_{SD} . Fig. 6 shows the forward output characteristic of the LPNP when V_{GS} =-0.6 V.

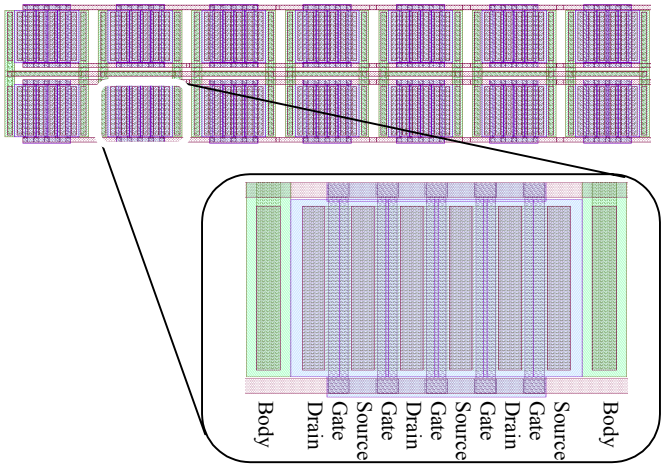

Figure 4. Layout of the p-MOSFET (L=0.5um, W=438um)

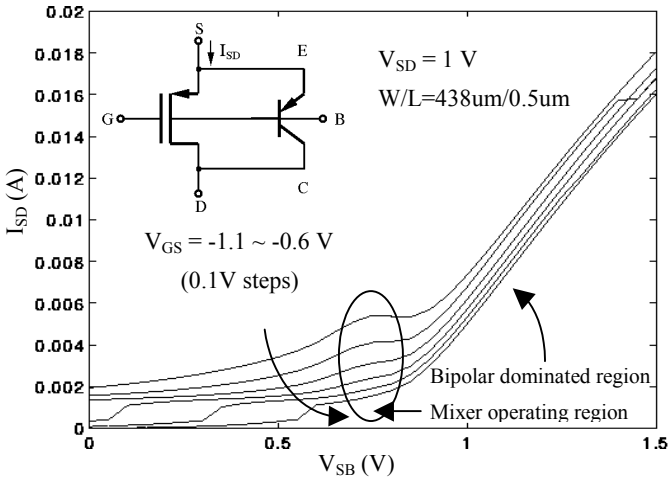

Figure 5. Experimental I_{SD} versus V_{SB} of the composite device

An Ebers-Moll model for the LPNP was extracted from a combination of experimental and simulation results for V =0.7V and V =-0.6V. The models parameter values are listed in Table 1. Since the p-MOSFET is in the n-well there is an additional junction capacitance C_S between the n-well and the p substrate. The unity current gain cutoff frequency of the device at this operation point is 6 GHz.

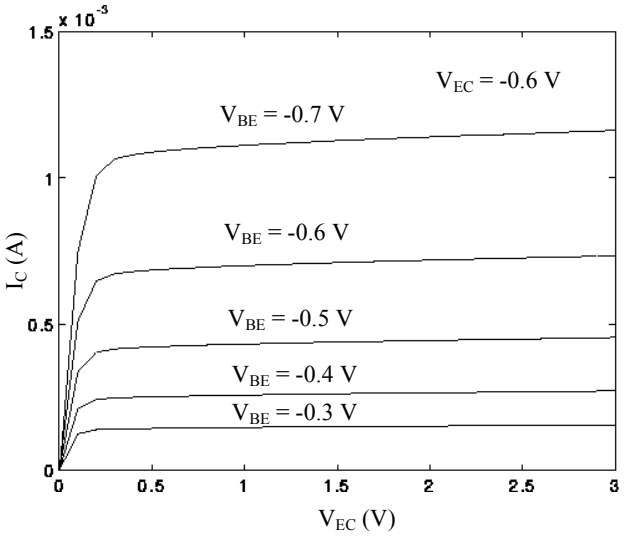

Figure 6. Experimental output characteristic of the LPNP (V_{GS}=-0.6V)

Table 1. Ebers-Moll model parameters of the LPNP (V_{GS}=-0.6V, V_{SB}=0.7V)

Symbol	Spice Keyword	Value
I_S	IS	2.2E-16 A
B_F	BF	50
r_B	RB	325 Ω
r_C	RC	15 Ω
r_E	RE	15 Ω
V_A	VAF	11.5 V
Eg	EG	1.11 eV
C_{JE}	CJE	5.3E-14 F
Φ_E	VJE	0.8 V
C_{JC}	CJC	3E-13 F
Φ_C	CJC	0.8 V
C_{JS}	CJS	2.98E-14 F
Φ_S	VJS	0.8 V
τ_F	TF	1.1E-11 S
τ_R	TR	1.1E-11 S
C_S	n/a	2E-12 F

5. 1.9 GHz MIXER CIRCUIT

The schematic of the mixer is shown in Figure 7. Both RF and LO input matching are on chip, while the output matching is off chip. C1, L1 and L2 form the RF matching network. C2, L3 and L4 form the matching network for the LO signal. C3, C4 and L5 form the IF matching network. A width of the p-MOSFET was picked to be 438 um to achieve the requested gain and IIP3. The width of 201 um was chosen for the n-MOSFET to achieve maximum adjustable range for the conversion gain. The component values in the design are listed in Table 2.

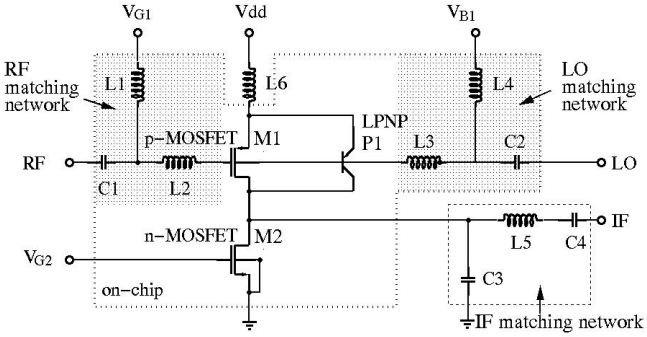

Figure 7. Schematic of the 1.9 GHz mixer

Table 2. List of mixer component

Component	Value
p-MOSFET (V_T=-0.6V)	W/L= 437.5 um / 0.5 um
n-MOSFET (V_T=0.45V)	W/L= 201 um / 0.25 um
C1	0.8 pF
C2	2.3 pF
C3	6 pF
C4	100 pF
L1	3 nH
L2	1 nH
L3	1 nH
L4	3 nH
L5	100 nH
V_{G1}	0.39 V
V_{B1}	0.4 V
V_{G2}	0.72 V

6. EXPERIMENTAL RESULTS

The mixer was implemented in a 5 level metal 0.25 um CMOS process. Careful layout of the mixer was necessary to obtain good high frequency performance. Capacitors were metal-to-metal capacitors.

A micrograph of the mixer is illustrated in Figure. 8. The area of the chip is 0.7x2 mm^2 including bonding pads. Less than 0.5% of the chip area is used for the active devices.

The fabricated chip was packaged in a 24 pin ceramic flat package (CFP) and mounted on a PCB. All measurements were performed in a 50 Ω system with all the needed external devices surface-mounted.

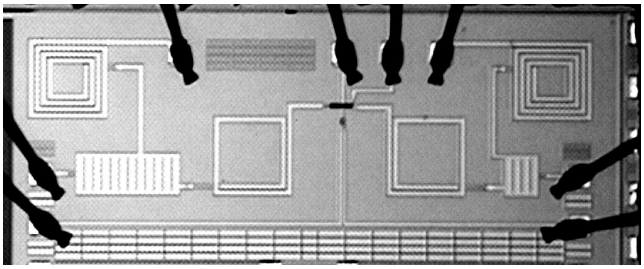

Figure 8. Microphotograph of the mixer

The measured conversion gain versus RF frequency is shown in Figure 9. The input LO power, P_{LO} and RF power Pin are -6 dBm and -20 dBm respectively. The IF frequency f_{IF} is fixed at 210MHz. A gain of 6.5 dB was obtained at 1.93 GHz. Figure 10 illustrates IF power versus RF input power. The LO frequency is fixed at 1720 MHz. P1dB is determined to be -17.5 dBm. Figure 11 illustrates the measured output spectrum of two tone test when a two-tone RF input at f_{RF1} =1930MHz and f_{RF2} =1938MHz was applied. IIP3 is measured to be -3.5 dBm. The complete set of mixer characteristics are listed in Table 3.

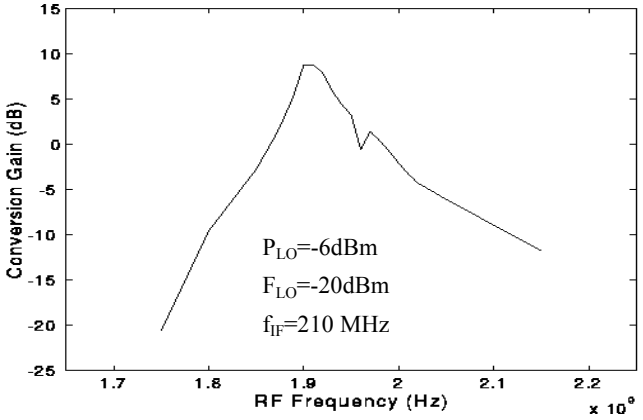

Figure 9. Experimental mixer conversion gain versus RF frequency

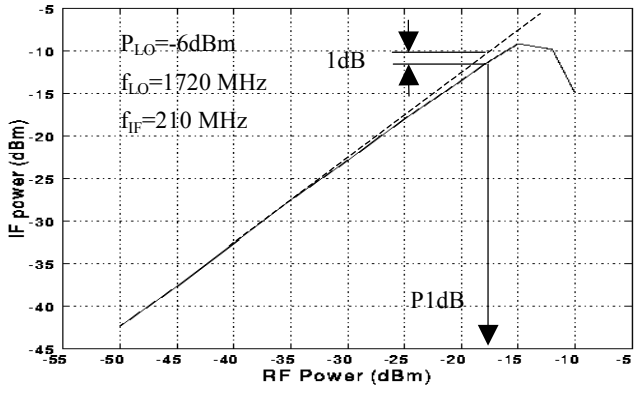

Figure 10. Experimental mixer IF power versus RF power

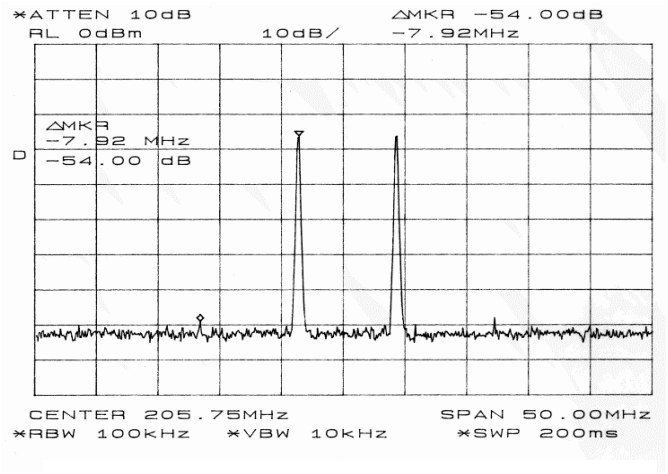

Figure 11. Experimental output spectrum of the two one test for the mixer

Table 3. Experimental characteristics of the mixer

Items	Value
Technology	W/L= 437.5 um / 0.5 um
Die area	W/L= 201 um / 0.25 um
RF frequency	0.8 pF
IF frequency	2.3 pF
Conversion gain	6 pF
P1dB	100 pF
IIP3	3 nH
SSB noise figure	1 nH
RF port return loss	1 nH
LO port return loss	3 nH
IF port return loss	100 nH
LO-RF isolation	0.39 V
LO-IF isolation	0.4 V
RF-IF isolation	0.72 V
Supply voltage	1 V
Power dissipation	1.3 mW

7. CONCLUSION

A RF mixer using the lateral bipolar transistor inherent in CMOS was designed and fabricated in a standard 0.25 um CMOS process. At 1.93 GHz, the mixer has a 6.5 dB gain, a 9.7 dB noise figure and -3.5 dBm IIP3. The circuit draws 1.3 mW from a 1 V supply.

This work has demonstrated that a MOSFET and the inherent lateral bipolar transistor can be used to design a low power mixer with good high frequency performance characteristics. Such a

mixer is a likely candidate for low power portable wireless applications. As shown in Table 4, the design compares very favorably with previous reported mixer at 1.9 GHz while using a simple architecture, requiring few components, eliminating interstage coupling, offering variable gain control by adjusting the gate bias of the n-MOSFET and reducing the supply voltage while still maintaining reasonable performance.

Table 4. Comparison with previous work

Design	Process	Gain (dB)	IIP3 (dBm)	NF (dB)	Power (Supply voltage)
Harada *et al* [8]	0.2 um CMOS/ SIMOX	6.7	-3.5	16.1	19 mW (1V)
this work	0.25 um CMOS	6.5	-3.5	9.7	1.3 mW (1V)

8. ACKNOWLEDGMENTS

The authors would like to acknowledge the support of NSERC, Micronet, CITO, Genum, Mitel, Nortel Networks and PMC-Sierra, and thank Yucai Zhang for helpful discussions on device-related issues.

9. REFERENCES

[1] Q. Huang, P. Orsatti and F. Piazza, GSM Transceiver Front-End Circuits in 0.25-um CMOS*, IEEE Journal of Solid-State Circuits*, Vol. 34, pp 292-303, 1999.

[2] E.Vittoz, MOS transistors operated in their lateral bipolar mode and their application in CMOS technology*", IEEE Journal of Solid-State Circuits*, vol SC-18, pp. 273-279, 1983.

[3] M. Degrauwe *et al*, CMOS voltage references using lateral bipolars, *IEEE Journal of Solid-State Circuits*, vol. SC-20, pp. 1151-1157, 1985.

[4] E. Vittoz, The design of high-performance analog circuits on digital CMOS chips, *IEEE Journal of Solid-State Circuits*, vol. SC-20, pp. 657-665, 1985.

[5] X. Arreguit *et al*., Precision compressor gain controller in CMOS technology*, IEEE Journal of Solid-State Circuits*, vol. SC-22, pp. 442-445, 1987 .

[6] T. W. Pan and A. A. Abidi, A 50-dB Variable Gain Amplifier Using Parasitic Bipolar Transistors in CMOS, *IEEE Journal of Solid-State Circuits*, Vol. 24, pp 951-961, 1989.

[7] Z. Yan, M. J. Deen and D. S. Malhi, Gate-Controlled Lateral PNP BJT: Characteristics, Modeling and Cir-cuit Applications, *IEEE Transactions on Electron Devices*, Vol. 44, pp. 118-128, 1997.

[8] M. Harada, T. Tsukahara and J. Yamada, 0.5-1V 2GHz Front-end Circuits in CMOS/SIMOX*, IEEE International Solid-State Circuits Conference*, pp. 378-379, 2000.