TUTORIAL 4

OPTIMIZATION STRATEGIES FOR PHYSICAL SYNTHESIS AND TIMING CLOSURE

Speakers:

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Background: This tutorial overviews various optimization techniques that can be utilized within a physical synthesis tool and/or achieve timing closure. The target audience consists of circuit designers who utilize these techniques, CAD engineers, and academic researchers. Familiarity with basic concepts in physical design is assumed.

Description: The first part of the tutorial discusses strategies for buffer insertion and wire sizing for a given net, focusing on the two stage methodology of first constructing a Steiner tree, then applying dynamic programming optimization. We show how to manage capacitance, polarity, and slew constraints while also performing blockage-aware routing. We also discuss different approaches to interconnect planning and physical resource allocation.

The second part describes optimizations that may be made at the gate and transistor levels. We will primarily focus on optimizations for transistor and gate sizing and local resynthesis. Additionally, issues related to transistor level optimization under dual threshold voltages will be addressed.

The third part is related to the consideration of signal integrity issues in design. One aspect relates to the design of supply networks to provide reliable voltage levels. We show the potential dangers that unreliable supply networks can have on timing closure and routability. A methodology to deal with the reliability of supply voltages in the design planning process will be put forward.

The fourth part will integrate all the techniques discussed into a physical synthesis methodology. Several placement techniques will be reviewed. Pros and cons of each in light of physical synthesis for design closure will be discussed. Factors that affect design closure include Congestion, Scan, Clocking, and Power Topology; each will be addressed using a coherent flow that will achieve the right trade-offs.