PANEL:

WILL NANOTECHNOLOGY CHANGE THE WAY WE DESIGN AND VERIFY SYSTEMS?

Moderator: ***Andreas Kuehlman - Cadence Berkeley Labs., Berkeley, CA***

During the past few decades advances in semiconductor technology have had only modest implications for the design and verification of integrated systems. While "deep-submicron" effects created new challenges for guaranteeing electrical integrity and necessitated the bundling of traditionally separated design steps such as logic synthesis and physical layout, the general integrated circuit design flow did not change. But what will happen when semiconductor technology hits the wall? Which of the currently futuristic nanotechnologies will step in and how will they change the way we design and verify systems? Will we just replace the implementation of the NAND-gate and D-flipflop and then do business as usual? Or do these technologies force us to abandon convenient hierarchical modeling of electrical, logical, and system levels? The panel will discuss the exciting opportunities of nanotechnologies and their implication for the design and verification of future systems.

Panelists:

Robert W. Dutton - Stanford Univ., Stanford, CA
Paul Franzon - North Carolina State Univ., Raleigh, NC
Seth C. Goldstein - Carnegie Mellon Univ., Pittsburgh, PA
Philip Kuekes - Hewlett-Packard Labs., Palo Alto, CA
Eric Parker - Zyvex, Richardson, TX
Thomas N. Theis - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY