Power-delay Modeling of Dynamic CMOS Gates for Circuit Optimization

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Abstract- We present an accurate analytical expression to compute power and delay of domino CMOS circuits from a detailed description of internal capacitor switching and discharging currents. The expression obtained accounts for the main effects in complex sub-micron gates like velocity saturation effects, body effect, device sizes and coupling capacitors. The energy-delay product is also evaluated and analyzed. Results are compared to HSPICE simulations (level 50) for a $0.18\mu m$ CMOS technology.

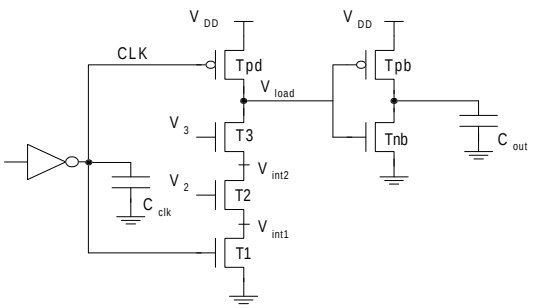

Figure 1 – 2NAND domino CMOS gate

I. Introduction

Power dissipation has become an important concern in circuit design during the last decade due to heating problems in high-density/high-performance circuits and to the power saving required for portable applications [1]. Domino CMOS is widely used in digital VLSI circuits with the advantage of small area and delay when compared to complementary static logic [2]. The pMOS transistor network is removed and replaced by a single pMOS charging transistor to reduce layout area and interconnect capacitance, thus increasing further circuit speed and reducing power dissipation. If the timing at the inputs is such that they are not asserted until after the precharge clock has been deserted, then there is no short-circuit current during the output transition reducing power dissipation and increasing througput. Power consumption is also decreased due to glitch-free operation. However, the large clock loads and signal transition activities due to the precharging result in an excessive power dissipation [3]. Since power consumption has become one of the biggest challenges in high-performance VLSI design [4], reducing power dissipation in domino CMOS ICs is critical for these applications. In this work we present analytical models to accurately compute power and delay of domino CMOS circuits from process parameters. These models can be used for fast timing and power estimation and circuit optimization. This paper is organized as follows. Section II presents an accurate and simple model of power dissipation in domino CMOS circuits. Section III develops the delay model, while Section IV presents a practical example of a 2NAND energy-delay optimization. The conclusions are in Section V.

II. Energy evaluation

Power consumption in domino circuits is mainly due to the charge/discharge of internal capacitors. This dynamic power is dissipated at the clock distribution network, the output buffer, the output load and the internal capacitors. The energy dissipated by domino CMOS circuits in one precharge/evaluation period can be expressed in a general from as $E = QV_{DD}$, where Q is the charge provided by the supply voltage during the cycle, and V_{DD} is the voltage difference through which the charge flows. The power consumption in a domino CMOS gate is related to this energy dissipated as $P = afE$, where f is the frequency of the clock, and a is the switching activity factor. In this work we analyze the power dissipation of the NAND gate of Fig. 1 when the output is charged and discharged. This analysis can be extended to gates with more than two logic transistors in the discharging path. The total energy dissipated by the NAND gate is:

$$E_{tot} = E_{clk} + E_{load} + E_{int} + E_{buff} \qquad (1)$$

where E_{clk} is the energy dissipated due to the clock, E_{load} is due to the capacitor at the logic output, E_{int} to internal switching capacitors, and E_{buff} to the output buffer.

A. Energy dissipated by the clock

This energy component is obtained computing the charge transferred per clock cycle by the clocking buffer. When the clock node is high the charge in this node is:

$$q^H_{clk} = \left(C_{clk} + C^H_{gbnT1} + C^H_{gsnT1} + C^H_{gdnT1} + C^H_{gdpd}\right) V_{DD} \quad (2)$$

where V_{DD} is the supply voltage, C_{clk} is the output load of the clock buffer, C^H_{gbnT1} and C^H_{gsnT1} are the gate-to-bulk and gate-to-source capacitances of the nMOS transistor driven by the buffer ($T1$ in Fig.1) when the clock is high, and C^H_{gdnT1} and C^H_{gdpd} are the gate-to-drain coupling capacitances of the nMOS and the pMOS transistors driven by the buffer evaluated when the clock is high. When the clock is low, the charge stored at the clock node is:

$$q^L_{clk} = -\left(C^L_{gspd} + C^L_{gbpd} + C^L_{gdpd}\right) V_{DD} \quad (3)$$

where C^L_{gspd}, C^L_{gbpd} and C^L_{gdpd} are the gate-to-source, gate-to-bulk and gate-to-drain parasitic capacitance values of transistor Tpd when the clock is low. The gate capacitance of transistors $T1$ and Tpd is $C_{gT1} = C^H_{gbnT1} + C^H_{gsnT1} + C^H_{gdnT1}$ and $C_{gTpd} = C^L_{gspd} + C^L_{gbpd} + C^L_{gdpd}$ respectively. These two components are dependent on transistor size as:

$$\begin{aligned} C_{gTpd} &= C_{ox} W_{pd_{eff}} \left(L_{peff} + 2L_{AP_p}\right) \quad (4) \\ C_{gT1} &= C_{ox} W_{n1_{eff}} \left(L_{neff} + 2L_{AP_n}\right) \end{aligned}$$

where C_{ox} is the gate oxide capacitance, $W_{pd_{eff}}$ and $W_{n1_{eff}}$ are the effective pMOS and nMOS channel width, L_{AP_n} and L_{AP_p} are the process bias on the channel length of nMOS and pMOS, while L_{peff} and L_{neff} are the effective pMOS and nMOS channel length respectively. Capacitance C^H_{gdpd} in eq.(2) is due to the side-wall capacitance between the gate and the drain of transistor Tpd, and is:

$$C^H_{gdpd} = C_{ox} W_{pd_{eff}} L_{AP_p} \quad (5)$$

From eqs. (2) and (3) we evaluate the charge provided by the supply node ($q^H_{clk} - q^L_{clk}$) and then the energy dissipated per cycle:

$$E_{clk} = \left(C_{clk} + C_{gT1} + C_{gTpd} + C^H_{gdpd}\right) V^2_{DD} \quad (6)$$

B. Power dissipated at the logic output

The power dissipated at the logic output is computed similarly. We assume that both gate inputs are at the high level when the clock pulse arrives (the worst-case in power dissipation). Under these conditions the charge stored at the output node of the domino gate is:

$$\begin{aligned} q^L_{load} &= -\left(C^H_{gdnT3} + C_{gTpb} + C^L_{gdnb} + C^H_{gdpd}\right) V_{DD} \\ q^H_{load} &= \left(C_{dpd} + C_{dnT3} + C_{gTnb} + C^H_{gdpb} + C^L_{gdpd}\right) V_{DD} \end{aligned} \quad (7)$$

Therefore, the energy dissipated due to the charge/discharge of the gate output is:

$$E_{load} = \left(C_{dpd} + C_{dnT3} + C^H_{gdnT3} + C_{gTnb} + C_{gTpb} + C^H_{gdpb} + C^L_{gdnb} + C^H_{gdpd} + C^L_{gdpd}\right) V^2_{DD} \quad (8)$$

where C_{dpd} and C_{dnT3} are the drain capacitances of transistors Tpd and $T3$, C_{gTnb} and C_{gTpb} are the gate capacitances of transistors Tnb and Tpb respectively. Finally, C^H_{gdnT3}, C^H_{gdpb}, C^L_{gdnb}, C^H_{gdpd} and C^L_{gdpd} are the gate-to-drain capacitances of transistor $T3$, Tpb, Tnb and Tpd respectively when their gate voltage are at the state defined by their superscripts. These capacitances have a linear dependence on the channel width of each transistor and can be easily evaluated.

C. Power dissipated by internal capacitors

If before precharge both inputs are high, then the internal nodes are grounded and the transistors of the chain are in the linear region. During precharge these nodes are charged until the upper transistor ($T3$ in Fig. 1) is off. The final value of the voltage at internal nodes is $V_{int1} = V_{int2} = V_{DD} - V_{T03}$ where V_{T03} is the threshold voltage of transistor $T3$. As in the previous steps we evaluate the charge provided by the supply voltage to compute the energy. The charge stored at the internal capacitors when all inputs are high and the internal nodes are low is:

$$q^L_{int} = -\left(C^H_{gsT3} + C^H_{gdT2} + C^H_{gsT2} + C^H_{gdT1}\right) V_{DD} \quad (9)$$

where C^H_{gsTi} and C^H_{gdTi} are the gate-to-source and gate-to-drain capacitances of the i-th transistor evaluated when the input is high and their drain and source are low (that is, when they are in the linear region). The value of these capacitances can be expressed as:

$$C^H_{gdTi} = C^H_{gsTi} = C_{ox} W_{ni_{eff}} \left(L_{neff}/2 + L_{AP_n}\right) \quad (10)$$

where $W_{ni_{eff}}$ and L_{neff} are the effective channel width and length of the i-th transistor.

The charge stored at the internal nodes when they are charged through the pull-up pMOS transistor is:

$$q_{int}^{H} = -\left(C_{gsT2}^{H} + C_{gdT2}^{H}\right) V_{DD} + \left(C_1 + C_2 + C_{gsT2}^{H} + C_{gdT2}^{H}\right) V_{int} \quad (11)$$

where C_1 is the drain capacitance of transistors $T1$ and $T2$, and C_2 is the drain capacitance of transistors $T2$ and $T3$. The side-wall capacitances of transistors $T1$ and $T3$ are neglected in eq.(11). Based on eqs. (9) and (11), the energy associated to the charge/discharge of this internal node capacitances is:

$$E_{int} = \left(C_{gsT3}^{H} + C_{gdT1}^{H}\right) V_{DD}^2 + \left(C_1 + C_2 + C_{gsT2}^{H} + C_{gdT2}^{H}\right) V_{int} V_{DD} \quad (12)$$

D. *Power dissipated by the buffer output*

Neglecting short-circuit currents, the charge at the buffer output when the output is high is:

$$q_{buff}^{H} = \left(C_{out} + C_{dpb} + C_{dnb} + C_{gdpb}^{L} + C_{gdnb}^{L}\right) V_{DD} \quad (13)$$

where C_{out} is the capacitance due to the gates driven by the buffer, C_{dpb} and C_{dnb} are the drain capacitances of the pMOS and the nMOS transistor of the buffer, and C_{gdpb}^{L} and C_{gdnb}^{L} are the gate-to-drain coupling capacitances of the pMOS and the nMOS transistors when the input voltage of the buffer is low. Similarly, the charge at the buffer output when it is low is:

$$q_{buff}^{L} = -\left(C_{gdpb}^{H} + C_{gdnb}^{H}\right) V_{DD} \quad (14)$$

From eqs. (13) and (14) the energy dissipated by the buffer is:

$$E_{buff} = \left(C_{out} + C_{dpb} + C_{dnb} + C_{gdpb}^{L} + C_{gdnb}^{L} + C_{gdpb}^{H} + C_{gdnb}^{H}\right) V_{DD}^2 \quad (15)$$

III. Delay model

Gate level energy reduction is always considered under timing constraints. There are several works that model delay in CMOS buffers [5, 6]. The analysis of multiple input gates is more complex due to the body effect at intermediate devices, and to charge distribution through the internal gates [5]. In this section we present a simple analytical model for delay evaluation in domino CMOS gates. We reduce the nMOS chain to an equivalent transistor. This device is then included in a simple model to compute the gate delay (t_{d_1}) and its output transition time (t_f). Finally, this simple delay model is applied to the CMOS output buffer to compute the whole delay.

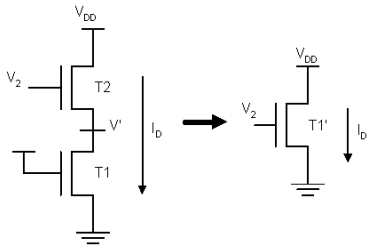

Figure 2 – Two series-MOSFET collapsing technique

A. *Current modeling of Stacked-MOSFET circuits*

The alpha-power law MOSFET model [5] provides a simple expression for short-channel devices:

$$I_D = \begin{cases} 0 & (V_{GS} \leqq V_{TH}) \\ (2 - \frac{V_{DS}}{V'_{D0}})\frac{V_{DS}}{V'_{D0}} I'_{D0} & (V_{DS} < V'_{D0}) \\ I'_{D0} & (V_{DS} \geqq V'_{D0}) \end{cases} \quad (16)$$

with

$$I'_{D0} = I_{D0}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{T0}}\right)^{\alpha} \quad (17)$$

where V_{GS} ,V_{DD}, V'_{D0} and V_{TH} are the gate, supply, saturation and threshold voltage respectively. The threshold voltage V_{TH} is expressed as:

$$V_{TH} = V_{T0} + \gamma V_{sb} \quad (18)$$

where V_{T0} is the threshold voltage with no substrate or drain bias, γ is the linearized body effect coefficient, and V_{sb} is the source-to-bulk voltage. I_{D0} is the drain current at $V_{GS} = V_{DS} = V_{DD}$. The parameter α is the velocity saturation index that ranges between 2 (long-channel devices) and 1 (short-channel). Parameters I_{D0}, V_{D0}, V_{T0} and α are extracted from the I-V data [5].

1. *Two stacked transistors*

Fig. 2 shows two series-connected nMOS transistors. We define the parameter $I_{D0}^{\langle 1,2\rangle}$ as the charge that flows through the two transistors when $V_1 = V_2 = V_{DD}$. In this state, transistor $T2$ is saturated while $T1$ is in the linear region. To compute $I_{D0}^{\langle 1,2\rangle}$ we assume that the internal node voltage V' is small compared to the supply voltage V_{DD} and equate the drain current of both transistors. Using $V_2 = V_{DD}$, a first order Taylor expansion of $T2$ drain current is:

$$I_{DS_2} \simeq I_{D0_2}\left(1 - \frac{\alpha_2 V'(1+\gamma_2)}{V_{DD} - V_{T0_2}}\right) \quad (19)$$

Since transistor $T1$ is in the linear region, its drain current when $V_1 = V_{DD}$ is:

$$I_{DS_1} = I_{D0_1}\left(2 - \frac{V'}{V_{D0_1}}\right)\frac{V'}{V_{D0_1}} \qquad (20)$$

Equating eqs. (20) and (19), and solving for V':

$$V' = V_0\left(1 - \sqrt{1 - \frac{V_{D0_1}^2 I_{D0_2}}{I_{D0_1} V_0^2}}\right) \qquad (21)$$

where:

$$V_0 = V_{D0_1} + \frac{\alpha_2\,(1+\gamma_2)\,V_{D0_1}^2 I_{D0_2}}{2\,(V_{DD} - V_{T0_2})\,I_{D0_1}} \qquad (22)$$

$I_{D0}^{\langle 1,2\rangle}$ is computed substituting eq.(21) in eq.(19).

We observed through SPICE simulations that when varying the gate voltage at transistor $T2$, the threshold and saturation voltage and also the velocity saturation coefficient of the chain were equal to the values of these coefficients for transistor $T2$. Therefore, the drain saturation current equation of the two series connected transistors when varying V_2 can be expressed as:

$$I_D = I_{D0}^{\langle 1,2\rangle}\left(\frac{V_2 - V_{T0_2}}{V_{DD} - V_{T0_2}}\right)^{\alpha_2} \qquad (23)$$

2. *Three stacked nMOS transistors*

In a three stacked transistors, the pair of transistors at the top of the chain (say $T2$ and $T3$) are collapsed to a single transistor $T2'$ with parameters $I_{D0_{T2'}} = I_{D0}^{\langle 2,3\rangle}$, $V_{T0_{T2'}} = V_{T0_3}$, $\alpha_{T2'} = \alpha_3$ and $\gamma_{T2'} = \gamma_3$. Then, transistor $T2'$ and $T1$ ($T1$ being the transistor at the bottom of the chain) are collapsed to an equivalent transistor $T1'$. The drain current when $V_1 = V_2 = V_3 = V_{DD}$ is computed as $I_{D0_{T1'}} = I_{D0}^{\langle 1,2'\rangle}$. We define this current as $I_{D0}^{\langle 1,3\rangle}$ ($I_{D0}^{\langle 1,3\rangle} \equiv I_{D0}^{\langle 1,2'\rangle}$).

3. *n-stacked nMOS transistor*

This scheme can be applied to a series of n-stacked MOSFETs. The drain current when varying the gate voltage of the n-th transistor in the chain (the upper transistor) is:

$$I_D = I_{D0}^{\langle 1,n\rangle}\left(\frac{V_n - V_{T0_n}}{V_{DD} - V_{T0_n}}\right)^{\alpha_n} \qquad (24)$$

where $I_{D0}^{\langle 1,n\rangle}$ is the drain current of the chain when $V_i = V_{DD}\ \forall i \in (1,2,...,n)$. Fig. 3 compares eq. (24) to HSPICE simulations for 4 series-connected nMOS transistors in a $0.35\mu m$ technology. Each input V_i is increased from $0V$ to V_{DD} with an input rise time of 300ps (The other three gates are fixed to V_{DD}). The current is fitted correctly when varying the top transistor $T4$ even for this dynamic simulations. Current values when varying the other three inputs provides a more complex behavior due to coupling capacitor and saturation effects.

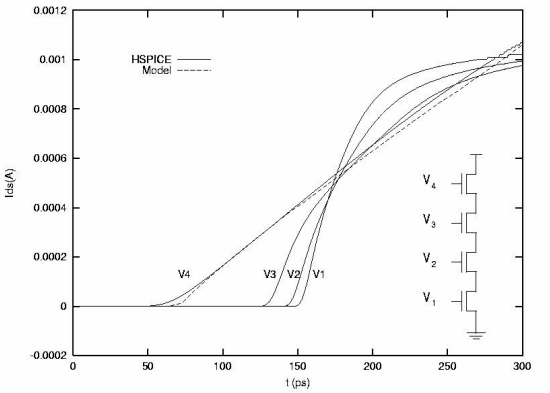

Figure 3 – Drain current of four series-connected nMOS transistors when varying each input(V_1,V_2,V_3 and V_4).

B. Delay model

The pull-down network is simplified to a single transistor following the process described previously. The parameter $I_{D0}^{\langle 1,n\rangle}$ represents the maximum current that can be driven by the chain of transistors. We compute the gate delay when the upper nMOS transistor switches. The input voltage is:

$$V_n(t) = V_{T0_n} + (V_{DD} - V_{T0_n})\frac{t - t_n}{t_{in} - t_n} \qquad (25)$$

where t_n is the time when the nMOS chain starts to conduct ($t_n = V_{T0_n} t_{in}/V_{DD}$) and t_{in} is the input rise time. At the beginning of the transition the nMOS chain is off and $V_{out} = V_{DD}$. At $t = t_n$, the nMOS chain starts to conduct. An analytical expression for the output voltage is obtained solving:

$$C_L\frac{dV_{out}}{dt} = -I_D \qquad (26)$$

where C_L is the total output capacitance of the gate, and I_D is the current of the chain. An analytical solution to eq. (26) from eqs. (24) and (25) is:

$$V_{out} = V_{DD} - \frac{I_{D0}^{\langle 1,n\rangle}}{C_L}\left(\frac{t - t_n}{t_{in} - t_n}\right)^{\alpha_n+1}\frac{t_{in} - t_n}{\alpha_n + 1} \qquad (27)$$

Eq. (27) is used to obtain the delay from the input at $0.5V_{DD}$ to the output at $0.5V_{DD}$ (t_{d_1}).

$$t_{d_1} = t_n + \left[\frac{Q_f\,(\alpha_n+1)}{I_{D0}^{\langle 1,n\rangle}}\right]^{\frac{1}{1+\alpha_n}}(t_{in} - t_n)^{\frac{\alpha_n}{\alpha_n+1}} - \frac{t_{in}}{2} \qquad (28)$$

where $Q_f = C_L V_{DD}/2$ is the charge transferred by the nMOS transistors when the output reaches $V_{DD}/2$. Eq. (28) is valid when $t_{d_1} < t_{in}/2$. If V_f is defined as the value of eq.(27) at time $t = t_{in}$, then eq.(28) is valid in the interval $V_f < V_{DD}/2$.

Otherwise, if the input node reaches the supply voltage before the output is at $V_{DD}/2$ then eq. (28) is not valid. The solution of eq.(26) when $V_n = V_{DD}$ is straightforward and in this case t_{d_1} is given by:

$$t_{d_1} = \frac{t_{in}}{2} + \frac{C_L\left(V_f - \frac{V_{DD}}{2}\right)}{I_{D0}^{\langle 1,n\rangle}} \tag{29}$$

Eq. (29) for t_{d_1} is valid when $V_f > V_{DD}/2$.

The slope of the output voltage at $V_{DD}/2$ can also be obtained as:

$$\left.\frac{dV_{out}}{dt}\right|_{V_{DD}/2} = \begin{cases} -\frac{I_{D0}^{\langle 1,n\rangle}}{C_L}\left(\frac{Q_f(\alpha_n+1)}{(t_{in}-t_n)I_{D0}^{\langle 1,n\rangle}}\right)^{\frac{\alpha_n}{\alpha_n+1}} & (V_f < V_{DD}/2) \\ -\frac{I_{D0}^{\langle 1,n\rangle}}{C_L} & (V_f > V_{DD}/2) \end{cases} \tag{30}$$

In calculating the output fall time of the dynamic gate (t_f), the output waveform slope is approximated by 70% of its derivative at the half-V_{DD} point [5].

The delay of the output buffer in Fig. 1 is obtained similarly using the alpha-power law parameters of the pMOS transistor of the buffer obtaining:

$$t_{d_2} = t_p + \left[\frac{Q_r}{I_{D0_p}}(\alpha_p+1)\right]^{\frac{1}{1+\alpha_p}}(t_f - t_p)^{\frac{\alpha_p}{\alpha_p+1}} - \frac{t_f}{2} \tag{31}$$

where $t_p = t_f |V_{TP}|/V_{DD}$ is the time when the pMOS device starts to conduct, α_p and I_{D0_p} are the velocity saturation index and the parameter I_{D0} of pMOS. Eq. (31) is valid when $V_r > V_{DD}/2$, where V_r is the voltage at the buffer output when $t = t_f$. If $V_r < V_{DD}/2$ then:

$$t_{d_2} = \frac{t_f}{2} + \frac{C_{out}\left(\frac{V_{DD}}{2} - V_r\right)}{I_{D0_p}} \tag{32}$$

The input fall time to the CMOS buffer is given by the value of t_f provided by the nMOS chain.

Short-circuit current contributions are neglected in this analysis while overshooting effects are considered. We include overshooting by computing the charge that must be transferred through the pMOS transistor to reach $V_{DD}/2$ at the output of the buffer. This charge is $Q_r = q_{buff}(V_o = V_{DD}/2) - q_{buff}^L$, where V_o is the output voltage of the buffer and the charge $q_{buff}(V_o = V_{DD}/2)$ can be approximated by $q_{buff}^H/2$ (see eqs.(13) and (14)).

Thus, the total delay is computed as the sum of this two delays ($t_d = t_{d_1} + t_{d_2}$).

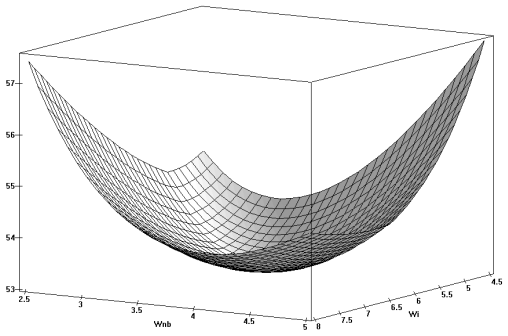

Figure 4 – Energy-delay product vs. W_{ni} and W_{nb} predicted by the model proposed.

IV. Energy-delay evaluation

The energy-delay relationship of each gate in an IC is controlled through design by device sizing. In the device description considered, the geometry dependence comes through parameters I_{D0n_i} and I_{D0p} (that are the parameter I_{D0} of transistors Ti and Tpb respectively). Since I_{D0} is linearly dependent to the channel width, we use:

$$I_{D0} = J_{D0}W + \delta I_{D0} \tag{33}$$

where J_{D0} and δI_{D0} are technology-dependent parameters. Applying eq.(33) to the energy and delay expressions derived previously we compute the energy-delay product (EDP). The channel width of the series connected MOSFETs (we assume that all transistors in the nMOS chain are equally sized) and the nMOS transistor of the buffer (W_{ni} and W_{nb}) can be optimized to obtain a minimum EDP. The pMOS channel width of the buffer is fixed to $W_{pb} = 2W_{nb}$.

In the simulations performed we compute the energy dissipated when the output is charged in the precharge phase and discharged in the evaluation phase when the gate voltage of any of the transistors of the chain (V_i) changes. The delay is computed as the time from $V_{DD}/2$ at the rising gate voltage V_i of transistor T_i to $V_{DD}/2$ at the output of the CMOS buffer. Fig. 4 is a plot of EDP as a function of parameters W_i and W_{nb} for a $0.18\mu m$ CMOS technology. A minimum is obtained for $W_{ni} = 6\mu m$ and $W_{nb} = 3.5\mu m$.

Fig. 5 compares model predictions to HSPICE simulations for EDP when varying W_{ni} for a fixed value of the buffer nMOS width $W_{nb} = 3.5\mu m$. HSPICE simulations are reproduced by the model that predicts the position of the minimum.

Fig. 6 compares the model to HSPICE when varying W_{nb} with W_{ni} evaluated at the minimum EDP obtained previously ($W_{ni} = 6\mu m$). A minimum at $W_{nb} = 3.5\mu m$ is obtained in accordance to HSPICE.

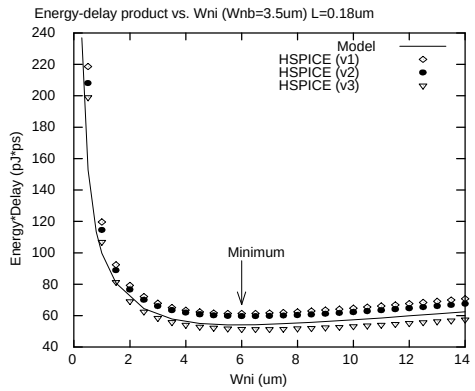

Figure 5 – Energy-delay product vs. nMOS channel width of series-connected transistors for a $0.18\mu m$ technology when varying V_1, V_2 or V_3.

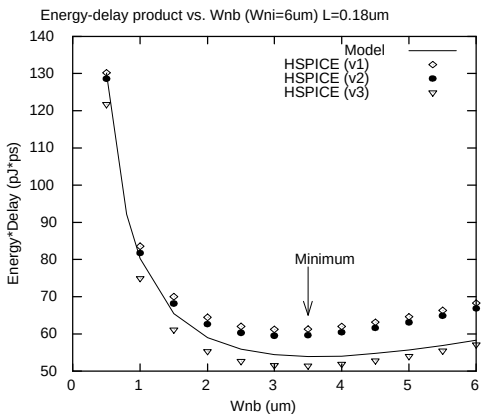

Figure 6 – EDP vs. W_{nb} for a $0.18\mu m$ technology when varying V_1, V_2 or V_3.

Finally, Fig. 7 plots EDP vs. supply voltage when $W_{nb} = 3.5\mu m$ and $W_{ni} = 6\mu m$. As can be appreciated, a minimum EDP is obtained at 0.9V as predicted by HSPICE simulations

V. Conclusions

We presented a simple and accurate analytical expression to compute power and delay of domino CMOS circuits from a detailed description of internal capacitor switching and discharging currents. The expression obtained account for the main effects present in complex sub-micron gates like velocity saturation effects, body effect, device sizes and coupling capacitors. The energy-delay product is also evaluated and analyzed showing a good agreement with HSPICE simulations for a $0.18\mu m$ technology. Although second order effects like short-circuit contribution are not included, the results obtained suggest that their contribution is not significant when computing the minimum EDP. Additional work is required to model EDP when any of the gate inputs

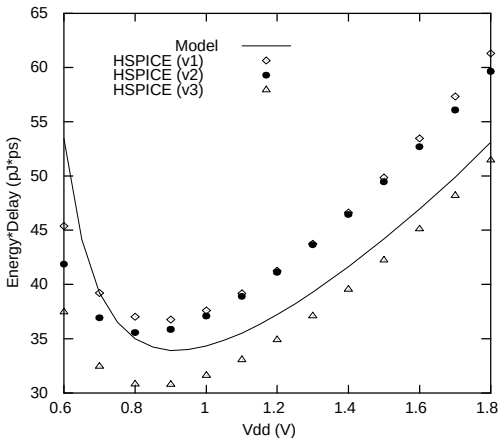

Figure 7 – Energy-delay product vs. supply voltage for a $0.18\mu m$ technology when varying V_1, V_2 or V_3.

makes a transition.

ACKNOWLEDGMENT

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