Crosstalk Fault Detection by Dynamic Idd

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Abstract

Undesired capacitive crosstalk between signals is expected to be a significant concern in deep submicron circuits. New test techniques are needed for these crosstalk faults since they may cause unacceptable performance degradation. We analyze the impact of crosstalk faults on a circuit's power dissipation. Crosstalk faults can be detected by monitoring the dynamic supply current. The test method is based on a recently developed dynamic Idd test metric, the energy consumption ratio (ECR). ECR-based test has been shown to be effective at tolerating the impact of process variations. In this paper, we apply a ECR-based test method called ECR-VDD test to detect the crosstalk faults. The effectiveness of the method is demonstrated by simulation results.

1. Introduction

Unintended capacitive interaction between signal lines in a circuit, referred to as crosstalk, is a significant concern in deep sub-micron circuits. Crosstalk capacitance may cause unanticipated additional delays which may be unacceptable. The circuit may violate timing requirements because of these crosstalk faults. Researchers have developed models to represent the effects of crosstalk capacitance. Test techniques to detect crosstalk faults, which are based on logic test, have also been reported in the literature [1] - [4].

Test techniques based on monitoring the dynamic current have recently been shown to be useful alternative test method [5] - [8]. One such dynamic current test technique is the energy consumption ratio (ECR), a test metric based on monitoring the average dynamic current consumed by a circuit [9]. ECR based test can be shown to detect many faults such as redundant faults, open faults, bridging faults and delay faults in both static and dynamic CMOS circuits. Many of these faults escape detection with other test techniques. Though the parameter monitored by the technique, the supply current, is an analog parameter, the test technique is very tolerant to the impact of process variations. ECR-based test has been demonstrated to be very effective through extensive simulation [9] and by application to an actual manufactured IC [10].

Contributions: We demonstrate the ability of ECR-based methods to detect crosstalk faults. We show that crosstalk faults can have a measurable impact on the energy consumed by a circuit. We apply ECR-VDD test, a variant of ECR test method, to detect crosstalk faults by measuring the ratio of energies consumed on the same periodic test vector at two different supply voltages. We investigate the ability of ECR-VDD test to detect crosstalk faults caused by crosstalk glitch effect and crosstalk delay effect. Our results indicate that the ECR can potentially be very effective at detecting crosstalk faults.

2. Previous Work

Several dynamic I_{dd} based test methods which measure transient or dynamic supply current to detect faults have been proposed [5] - [8]. Dynamic I_{dd} methods have been shown to have the potential to detect faults that escape other test techniques. A limitation for dynamic I_{dd} test methods is that, normal process variation can cause the supply current in a circuit to vary substantially, thereby degrade the fault coverage.

The impact of process variations can be negated by measuring the ratios of currents consumed on two different input vector transitions. The ratio of average currents, on two different periodic input sequences, is defined as the energy consumption ratio (ECR).

The ECR test method consists of taking the average current measurements on k(≥ 2) input sequences and calculating $\frac{k(k-1)}{2}$ ECRs. For each ECR a range for good circuit is pre-computed. If any of the ECRs fall outside the expected range then the circuit is declared to be faulty. For k=2, good results on actual silicon have been reported [9] [10].

A variant of ECR test method, ECR-VDD test, has been developed to detect delay faults [11]. The ECR-VDD test detects faults by measuring the ratio of energies consumed on the same periodic test vector at two different supply voltages. It is shown in [11] that the ECR-VDD test is effective in detecting resistive bridges and opens which cause delay failures..

3. Power Consumption with Crosstalk

The primary source of crosstalk interaction between two wires in undesired capacitive coupling. Fig. 1 shows a typical model used to represent crosstalk effects. Crosstalk is modeled by adding a capacitor between interacting wires. There are two major crosstalk effects: crosstalk glitch and crosstalk delay. Crosstalk glitch occurs when there is a switch for the signal at one line and the signal at the other line is driven steady, in which case a glitch is formed at the output of the steady line. The condition for crosstalk delay is that the signal at both lines switches to the opposite direction. The result is an increase in transition time.

The crosstalk effect has a great impact on the power dissipation of the circuits. To illustrate this, we investigate a simple circuit shown in Fig. 2. The channel length is 0.25μm and we indicate the ratio of widths of the PMOS

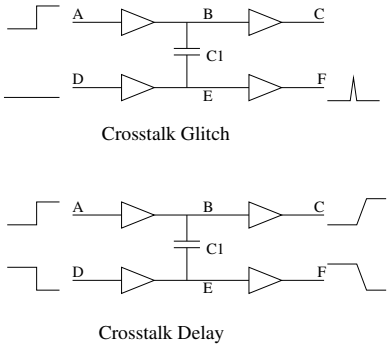

Figure 1. Model for crosstalk analysis.

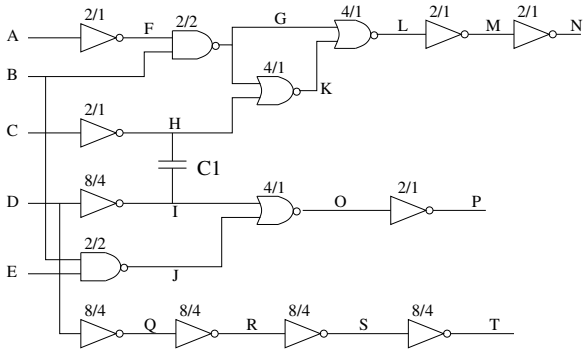

Figure 2. A simple circuit.

and NMOS FETs above each gate. The supply voltage is 2.5V, and TSMC 0.25μm technology files are used for device simulation. Assume that line H and I are long and close to each other. I is the affecting line and H is the victim line. A capacitor C_1 is put between H and I to model the crosstalk coupling capacitance. The inverter driving line I is assumed to be a buffer with strong driving strength.

We study the impact of crosstalk glitch effect first. The inputs are alternated between vectors V1 = (ABCDE) = 01111 and V2 = (ABCDE) = 01101 with a period of 10ns. Table 1 shows the average supply current (I_{DD}) and charging/discharging current on C_1 (I_{C1}) under the crosstalk glitch effect. We use letter "F" to denote the case that the glitch propagates to the output, and letter "G" for the case that no glitch propagates to the output. The glitch does not propagate to the output when $C_1 < 0.1pf$ (Fig. 3a), but propagates to the output when $C_1 \geq 0.1pf$ (Fig. 3b). The crosstalk glitch should pass a certain threshold to propagate to the output. We define N_G as the number of transitions in the case of no crosstalk glitch propagation, and N_F as the number of transitions in the case of crosstalk glitch propagation. To a first order approximation, the average supply current I_{DD} is the sum of the dynamic current due to gate transitions (I_T) and the charging/discharging current on C_1 (I_{C1}). So I_T is $I_{DD} - I_{C1}$, which is also shown in Table 1. Let $I_{DDF}(I_{DDG})$ be the average supply current for the case of crosstalk propagation(no propagation), then

$$I_{DDF} = I_T + I_{C1} = N_F C V_{DD} f + C_1 V_{DD} f \qquad (1)$$

C_1	I_{DD}	I_{C1}	I_T
0	34.966μA(G)	0	34.966μA
0.001p	35.242μA(G)	0.25μA	34.992μA
0.01p	37.577μA(G)	2.5μA	35.077μA
0.05p	49.517μA(G)	12.5μA	37.017μA
0.1p	72.048μA(F)	25μA	47.048μA
0.15p	85.988μA(F)	37.5μA	48.488μA
0.2p	99.316μA(F)	50μA	49.316μA

Table 1. The supply current under crosstalk glitch effect (2.5V supply voltage).

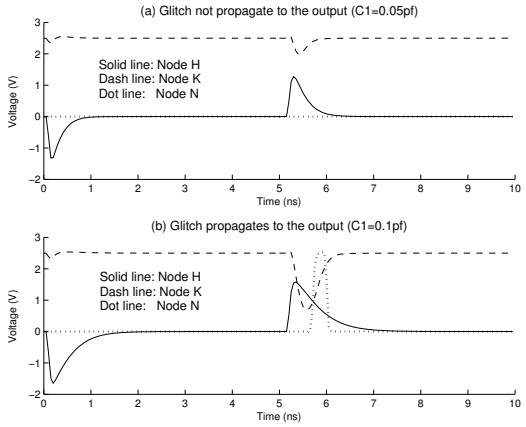

Figure 3. Crosstalk glitch propagation.

$$I_{DDG} = I_T + I_{C1} = N_G C V_{DD} f + C_1 V_{DD} f \qquad (2)$$

where C is the total capacitance in the circuit except C_1. Since $N_F > N_G$, I_T is larger in the case of crosstalk glitch propagation. So we have $I_{DDF} > I_{DDG}$. Crosstalk glitch significantly affects the power consumption of the circuits, thus crosstalk faults caused by crosstalk glitch can be detected by monitoring the average supply current.

C_1	I_{DD}	I_{C1}
0	113.57μA(B)	0
0.01p	130.61μA(B)	10μA
0.05p	212.97μA(B)	50μA
0.1p	284.40μA(D)	100μA
0.12p	298.27μA(D)	120μA
0.14p	304.49μA(D)	140μA
0.16p	305.77μA(D)	160μA
0.18p	299.31μA(F)	180μA
0.2p	297.56μA(F)	200μA

Table 2. The supply current under crosstalk delay effect (2.5V supply voltage).

Now we look at the impact of crosstalk delay effect to the power consumption of the circuit. The inputs are alternated between vectors V1 = (ABCDE) = 11101 and V2 = (ABCDE) = 01011 with a period of 5ns. Table 1 shows the average supply current (I_{DD}) and charging/discharging current on C_1 (I_{C1}) under the crosstalk delay effect. We define three error types: *logical failure*, *delay failure*, and

benign error. We use letter "L" to denote *logical failure*, letter "D" for *delay failure* and letter "B" for *benign error*. *logical failure* means that if we apply a test either at slow or high speed, the crosstalk delay effect will cause a failure at the output. *delay failure* is referred to the case that the crosstalk delay effect will not cause a failure at slow speed (e.g., a frequency of 200MHz), but will cause a failure at higher speed (e.g., a frequency of 400MHz). *benign error* means the crosstalk delay effect causes no logical and delay failure.

The charge and discharge of crosstalk capacitor C_1 has great impact on the power dissipation of the cricuit. C_1 will charge twice and discharge twice in a clock period, thus

$$I_{C1} = 2C_1V_{DD}f \tag{3}$$

Since I_{C1} is proportional to the value of the capacitance, the average supply current increases as C_1 increases until the crosstalk delay causes a logical failure.

The difference in error types also contributes to the change in the dynamic supply current. Fig. 4 shows the voltages at the input, one end of C_1 and the output in the case of *delay failure* and *logical failure*. As C_1 increases node H rises and falls much more slowly. The "ON time" of the signal after passing node H reduces and forms a glitch. When $C_1 > 0.16pf$, the glitch cannot propagate to the output node N, which cause a logical failure at the output. The number of transitions in the case of *logical failure* is smaller than that in the case of *delay failure* and *benign error*, therefore circuits under logical failure will consume less dynamic supply current.

A large number of crosstalk faults are generated during layout design (e.g., two long wires are too close to each other). If there were one crosstalk fault generated in the layout design, then all the circuits would be faulty. Therefore it is difficult to distinguish good and faulty designs by only monitoring the dynamic supply current at a single supply voltage. So in the next section, we apply ECR-VDD test, a variant of ECR test method, to detect the crosstalk faults come from layout design.

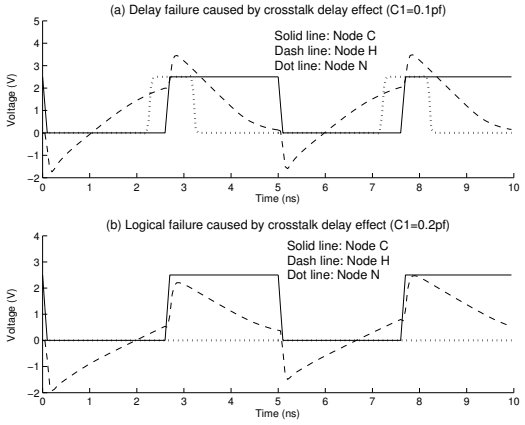

Figure 4. Crosstalk delay effect.

4. ECR-VDD Test for Crosstalk

ECR-VDD test is a variant of ECR test method. In the ECR-VDD test method the average supply current J_1, J_2 are measured on the same input sequence S_1, but for two different supply voltages V_{1DD}, V_{2DD}. The ratio $ECR_{VDD} = \frac{J_1}{J_2}$ is used to distinguish good and faulty circuits. If ECR_{VDD} falls within a predetermined range then the circuit is declared to be good, otherwise it is declared to be faulty.

4.1. Test for Crosstalk Glitch

We investigate the example circuit in section 3. The inputs are alternated between vectors V1 = (ABCDE) = 01101 and V2 = (ABCDE) = 01111 with a period of 10ns. The supply currents on different crosstalk capacitance are measured at two supply voltages 2.5V and 1.25V. The ratio ECR_{VDD} is calculated and shown in Table 3. The fault free ratio is $\frac{V_{1DD}}{V_{2DD}} = \frac{2.5}{1.25} = 2$. We set a guard band of 10 percent, so the upper bound of ECR_{VDD} is 2.2. ECR is rather insensitive to process variation so a guard band of 10 percent is reasonable. The circuits with ECR_{VDD} marked by * are declared to be faulty. When the crosstalk capacitance is between 0.1pf and 0.13pf, the crosstalk glitch will propagate to the output at the 2.5V supply voltage but will not propagate at 1.25V, thus the ratio ECR_{VDD} can be written as

$$ECR_{VDD} = \frac{N_FCV_{1DD}f + C_1V_{1DD}f}{N_GCV_{2DD}f + C_1V_{2DD}f} \tag{4}$$

Since $N_F > N_G$, the ratio ECR_{VDD} when the crosstalk capacitance is between 0.1pf and 0.13pf is larger than the fault free ratio $\frac{V_{1DD}}{V_{2DD}}$, thus can be detected by ECR-VDD test.

Table 4 shows the ECR_{VDD} ratio calculated based on the supply current measured at 2.5V and 1V. We set a guard band of 10 percent to ensure all the good circuits pass the test. The upper bound of ECR_{VDD} is 2.75. The circuits with $C_1 \geq 0.1pf$ are declared to be faulty. When V_{1DD} is decreased, it is harder for a crosstalk glitch to pass a certain threshold such that it can propagate to the output. When the supply voltage is as low as 1V, the crosstalk glitch will not propagate to the output circuits as long as $C_1 \leq 0.2pf$. It is shown on Table 4 that more circuits have different number of transitions at two supply voltages, thereby can be detected by ECR-VDD.

C_1	1.25V	2.5V	ECR_{VDD}
0	G	G	2.064
0.001p	G	G	2.063
0.01p	G	G	2.065
0.05p	G	G	2.111
0.10p	G	F	2.369*
0.11p	G	F	2.349*
0.12p	G	F	2.318*
0.13p	G	F	2.262*
0.14p	F	F	2.176
0.16p	F	F	2.176
0.18p	F	F	2.199
0.20p	F	F	2.230*
0.25p	F	F	2.340*
0.30p	F	F	2.460*

Table 3. ECR_{VDD} at 1.25V and 2.5V, for detection of crosstalk glitch. Circuits with ECR_{VDD} marked by * are detected by ECR-VDD.

C_1	1V	2.5V	ECR_{VDD}
0	G	G	2.576
0.001p	G	G	2.580
0.01p	G	G	2.581
0.05p	G	G	2.662
0.10p	G	F	3.042*
0.11p	G	F	3.046*
0.12p	G	F	3.048*
0.13p	G	F	3.053*
0.14p	G	F	3.073*
0.16p	G	F	3.116*
0.18p	G	F	3.164*
0.20p	G	F	3.199*
0.25p	F	F	3.298*
0.30p	F	F	3.553*

Table 4. ECR_{VDD} at 1V and 2.5V, for detection of crosstalk glitch. Circuits with ECR_{VDD} marked by * are detected by ECR-VDD.

4.2. Test for Crosstalk Delay

The same circuit in section 3 is used to analyze the ability of ECR-VDD test to detect faults caused by crosstalk delay effect. The inputs are alternated between vectors V1 = (ABCDE) = 11101 and V2 = (ABCDE) = 01011 with a period of 5ns. The ratio ECR_{VDD} at two supply voltages 1.75V and 2.5V is shown in table 5. The fault free ratio is $\frac{2.5}{1.75} = 1.429$. If we set a guard band of 10 percent, the upper bound ECR_{VDD} for good circuits is 1.57. From Table 5 we may see that, circuits with different error types at two supply voltages have larger ECR_{VDD} ratios. It is clearly explained in [11] that, at different error type, the number of gate transitions is different. If the circuit has different error types at two different supply voltages V_{1DD} and V_{2DD}, the ECR_{VDD} ratio is no longer the fault free ratio $\frac{V_{1DD}}{V_{2DD}}$. For example, if circuit has a *delay failure* at V_{1DD} and *logical failure* at V_{2DD}, the ECR_{VDD} ratio is

$$ECR_{VDD} = \frac{N_{FD}V_{1DD} + C_1V_{1DD}}{N_{FL}V_{2DD} + C_1V_{2DD}} \quad (5)$$

Where $N_{FD}(N_{FL})$ is the number of transitions at *delay failure* (*logical failure*).

Our results above show that the ECR-VDD will be good at detecting crosstalk faults caused by crosstalk glitch and delay.

5. Conclusion

We showed that crosstalk effects have a great impact on the average supply current, and investigated the capability of ECR-based test methods to detect crosstalk faults. We applied the ECR-VDD test, a variant of ECR test method, to detect crosstalk faults caused by crosstalk glitch and crosstalk delay. Our results showed the effectiveness of ECR based test methods in detecting crosstalk faults.

C_1	1.75V	2.5V	ECR_{VDD}
0	B	B	1.484
0.001p	B	B	1.484
0.01p	B	B	1.470
0.05p	B	B	1.475
0.08p	D	B	1.566
0.10p	D	D	1.658*
0.12p	F	D	1.775*
0.14p	F	D	1.812*
0.16p	F	D	1.813*
0.18p	F	F	1.770*
0.20p	F	F	1.756*
0.25p	F	F	1.744*
0.30p	F	F	1.743*

Table 5. ECR_{VDD} at 1.75V and 2.5V, for detection of crosstalk delay. Circuits with ECR_{VDD} marked by * are detected by ECR-VDD.

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