CASh: A Novel "Clock as Shield" Design Methodology for Noise Immune Precharge-Evaluate Logic

Yonghee Im and Kaushik Roy
Email: yonghee, kaushik@ecn.purdue.edu
School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA

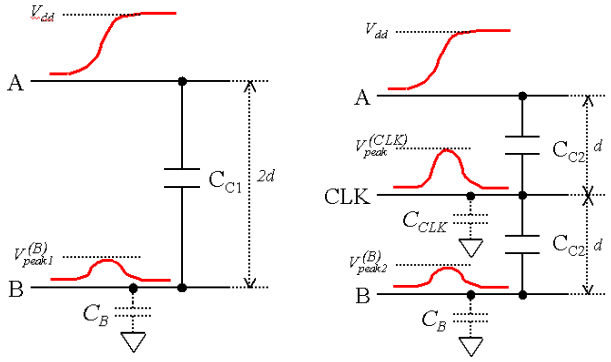
Abstract— **In gigascale integrated circuits (GSI), interconnects are expected to play a more dominant role in circuit performance than transistor cells. The circuit performance is affected by signal integrity as cross-talk becomes more significant with the scaling of feature sizes. Many attempts have been made to improve noise immunity, but all require the sacrifice of speed as a trade-off, especially in dynamic circuits. Avoiding noise problems while maintaining the desired speed would involve increased wire spacing or extensive shielding, both of which are unfavorable due to demands for high density and a relatively higher cost of wires in current process technologies. We propose a novel methodology in which clock lines are used as shielding wires to reduce cross-talk effects in domino circuits, thereby minimizing the possiblity of functional failures. In addition, this method provides another benefit: a small buffer size is required for driving a long interconnect for iso-noise immunity. Since clock lines, which are always required in domino circuits, are used to shield signal lines, speed penalty and area overhead which are drawbacks of previous work can be avoided. This design methodology CASh (Clock As Shielding) demonstrates the superiority over conventional methods. HSPICE simulations on a 2-input domino AND gate and 4 and 8-bit full adders designed in CASh show higher noise immunity over conventional design.**

I. INTRODUCTION

It was claimed by Meindl [1] that *gigascale integration* (GSI) would be governed by a hierarchy of five levels: (1) fundamental, (2) material, (3) device, (4) circuit, and (5) system. It is expected that the performance limit on GSI would be imposed by interconnect and not by a *metal-oxide semiconductor field effect transistor* (MOSFET). Besides performance, interconnect is also anticipated to have a large impact on *signal integrity* in GSI. The voltage level of the signal on a node is disturbed by *cross-talk*, which is induced by unwanted coupling from neighboring signal wires to the node. Cross-talk increases because the spacing between wires narrows as features scale down. Increase in cross-talk is also attributed to increasing the wiring *aspect ratio* (AR = height/width) that results from an attempt to prevent a drastic increase in wire resistance.

In GSI, the signal integrity issue will be more crucial for dynamic logic designs, which have been widely used to achieve better performance at the cost of low noise immunity. Let us consider domino circuits as an example. First, during the evaluation mode, the precharged output leaks in the form of subthreshold current, charge-sharing, and reverse-bias diode leakage. Since subthreshold current increases exponentially as threshold voltage (V_t) scales down, the leakage current cannot be ignored any longer [2]. Second, the DC noise margin of a domino circuit is equal to V_t of NMOS in *pull-down network* (PDN). With the down-scaling of V_t, the DC noise margin decreases. Furthermore, it is hard to effectively restore the damaged output level in domino circuits. Quantitative analysis and comparisons of a few dynamic logic styles in terms of *dynamic noise margin* (conceptually, the product of voltage and time) were reported by Somasekhar et. al. in [3].

This work was supported in part by SRC (98-HJ-638), GSRC (Gigascale Silicon Research Center), and Intel Co.



(a) Non-CASh (b) CASh

Fig. 1. Comparison of V_{peak}^{victm} between Non-CASh and CASh

Realizing that low noise immunity is a significant issue in dynamic logic, much effort has been devoted to *noise tolerant circuit* design [4], [5]. However, the weakness of all past research on noise tolerant dynamic circuits is that speed has been sacrificed in exchange for increased noise immunity. Such approaches should be re-examined, in the sense that dynamic logic was originally created for high performance. Therefore, the best way to achieve high noise immunity would be to minimize coupling capacitance (C_c) between wires.

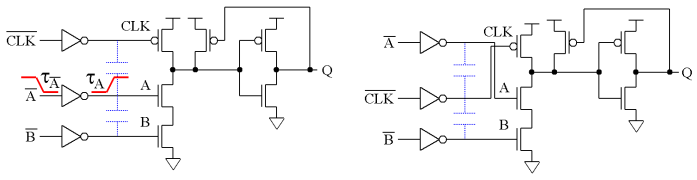
Avoiding noise problems caused by increased C_c would involve increased wire spacing or extensive shielding. However, demand for high density and relatively higher cost of wires restrict these approaches to reduce C_c. This paper suggests a novel methodology, in which clock lines are used as shielding wires in domino circuits to tackle noise issues. The methodology is named *CASh* (*Clock As Shielding*). Since clock is always required in any dynamic circuit, including domino, extra area consumption caused by inserting power lines in the traditional shielding method can be avoided. CASh not only provides improved noise immunity, but also reduces the buffer size for iso-noise immunity.

The rest of the paper is organized as follows. The basic concepts and potential advantages of CASh methodology are explained in section 2. Section 3 demonstrates the superiority of CASh in comparison to the conventional layout methods.

II. CLOCK AS SHIELDING METHODOLOGY

A. Basic Concept

Let us consider a pair of neighboring wires. Signal transitions on one wire induce a coupling noise on the other because the wires are coupled capacitively and inductively. We restrict our attention to capacitive coupling in the paper. This form of noise, which is also referred to as cross-talk, is recognized as a dominant source of noise in GSI [6]. Conventionally, an affecting wire is named *aggressor*, while the affected ones are called *victims*. When the signal on the aggressor rises from 0 V



(a) Non-CASh (b) CASh

Fig. 2. Schematics of 2-input domino AND gate

to V_{peak}^{aggr} and the victim remains still, the peak voltage level of coupling noise induced on the victim is determined by Eq. 1

$$V_{peak}^{vctm} = \frac{C_c}{C_c + C_v} V_{peak}^{aggr} \quad (1)$$

where C_c is the coupling capacitance between aggressor and victim nodes, and C_v is the capacitance to ground of the victim node. Notice from Eq. 1 that V_{peak}^{vctm} depends on not only C_c, but also on V_{peak}^{aggr}. CASh reduces V_{peak}^{vctm} by reducing V_{peak}^{aggr}. Now let us examine how the relationship among these three factors, V_{peak}^{vctm}, C_c, and V_{peak}^{aggr}, changes when a certain wire is inserted in the middle of a pair of wires.

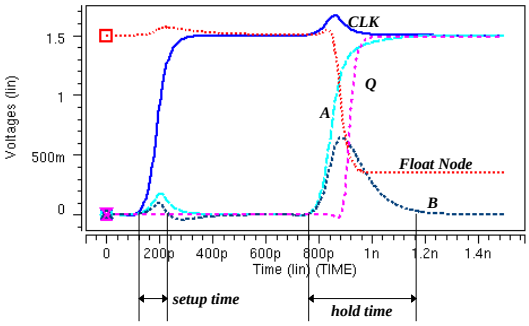
Let us consider two conductors forming a plate capacitor, as shown in Fig. 1 (a). With coupling capacitance C_{c1}, the peak voltage level on victim node B (V_{peak1}^{B}) is easily obtained from Eq. 1 when aggressor node A transits from 0 to V_{dd}. If another sheet conductor is inserted between node A and node B (Fig. 1 (b)), the peak voltage on B (V_{peak2}^{B}) is calculated as follows:

$$\begin{aligned} V_{peak2}^{B} &= \frac{C_{c2}}{C_{c2}+C_B} V_{peak}^{CLK} \\ &= \frac{C_{c2}}{C_{c2}+C_B}\left(\frac{C_{c2}}{C_{c2}+C_{CLK}} V_{dd}\right) \text{ assume } C_B = C_{CLK} \\ &= \left(\frac{C_{c2}}{C_{c2}+C_B}\right)^2 V_{dd} \\ &= \left(\frac{2C_{c1}}{2C_{c1}+C_B}\right)^2 V_{dd} \\ &= \left(\frac{C_{c1}}{C_{c1}+C_B/2}\right)^2 V_{dd} \end{aligned} \quad (2)$$

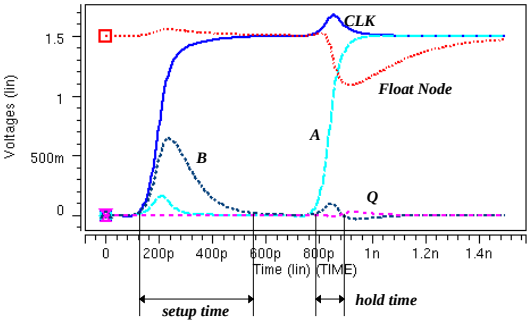
Comparing the peak voltage levels of these two cases, V_{peak1}^{B} is always larger than V_{peak2}^{B}, as long as $C_B = C_{CLK}$. In other words, if a conductor is inserted, the peak voltage level on the victim node can be less, although the coupling capacitance between victim (B) and aggressor (A) remains the same regardless of wire insertion.

B. Side Effects in CASh

Even though CLK lines in CASh succeed in shielding signal lines from each other during an evaluation mode, CLK lines itself may give rise to another coupling noise on the signal lines. If this CLK-induced noise is large enough to result in any functional fault, the benefit during an evaluation mode would be nullified. In order to see how serious the side effect of CLK insertion is, we did HSPICE simulation on a CASh style 2-input domino AND gate and Non-CASh one (Fig. 2). Unlike in Fig. 1, the coupling capacitances of two cases are the same by just shuffling the wires in Fig. 2. In this simulation, we used a small driver to victim node B so that aggressor node A could induce a sufficient coupling noise voltage to cause functional fault during an evaluation mode in the non-CASh case. The same buffer sizes are used for CLK and input A. Under the condition of a large C_c of $20fF$, it is shown in Fig. 3 that cross-talk induced

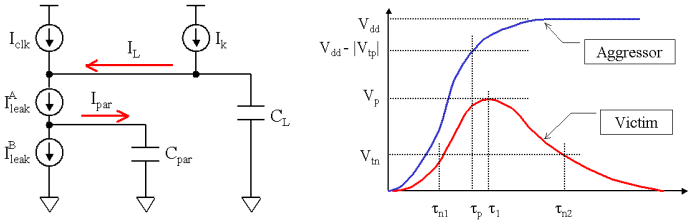


(a) Non-CASh



(b) CASh

Fig. 3. HSPICE simulation results (confirming side effect of CASh can be negligible)



(a) Current model of the 2-input domino AND gate (b) Waveforms and time stamps

Fig. 4. Current modeling and associate time stamps

by CLK during its transition does not induce functional failure. This is due to the precharge PMOS transistor which keeps supplying more charges than those leaking through PDN.

C. Upper Bounds of Slew Rate of Aggressor (τ_A) and Coupling Capacitance (C_c)

In a domino circuit, if the voltage level on the floating node falls below the trip point of the following inverter due to leakage, the output of the gate changes, resulting in functional fault. The amount of leakage charge is determined mainly by the waveforms on victim nodes, which are, in turn, determined by the slew rate of associated aggressors (τ_A) and the coupling capacitances (C_c).

We attempted to derive upper bounds of τ_A and C_c between aggressor and victim for the 2-input domino AND gate designed in CASh style. Fig. 4(a) shows a current modeling used in the 2-input domino AND gate, while Fig. 4(b) displays the waveforms of aggresor and victim along with a few time stamps. τ_{n1} is the time stamp at which the pulse at the victim passes through the threshold voltage of the associated NMOS transistor at upturn of the waveform, while τ_{n2} is such a time stamp at downturn.

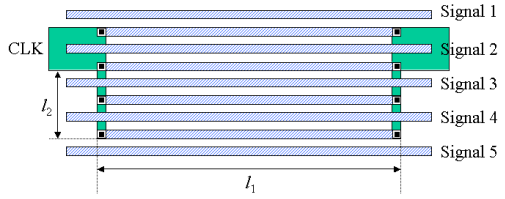


Fig. 5. Rake clock

The pulse at the victim reaches its peak point at τ_1. PMOS transistor of the aggressor stays on until τ_p. As explained previously, functional fault may occur when the remaining charge ($Q_{leak}(t)$) on the floating node having load capacitance, C_L, crosses below the trip point of the inverter. $Q_{leak}(t)$ at the trip point is approximately a half of the total charge on C_L during a precharge mode (Eq. 3). Therefore, Eq. 4 holds for the 2-input domino AND gate, which is modeled in terms of current in Fig. 4(a). Since NMOS transistors A and B are connected in series, the amount of charge leaking through PDN is determined mainly by that flowing through NMOS B (I^B_{leak}). Current sources from precharge PMOS and keeper (I_{clk} and I_k) should be subtracted from I^B_{leak} to calculate the final value of I_{leak}.

$$Q_{remain}(t) = C_L V_{dd} - Q_{leak}(t) = \frac{1}{2} C_L V_{dd} \quad (3)$$

$$Q_{leak}(t) = \frac{1}{2} C_L V_{dd} = \int_0^{T_{eval}} I_{leak}(t)dt$$

$$= \int_0^{T_{eval}} I^B_{leak}(t) - (I_{clk} + I_k)dt \quad (4)$$

$$\therefore \frac{1}{2} C_L V_{dd} = \int_{\tau_{n1}}^{\tau_{n2}} \kappa^n \nu^n_{sat} C^n_{ox}(V_b(t) - V_{tn})dt -$$

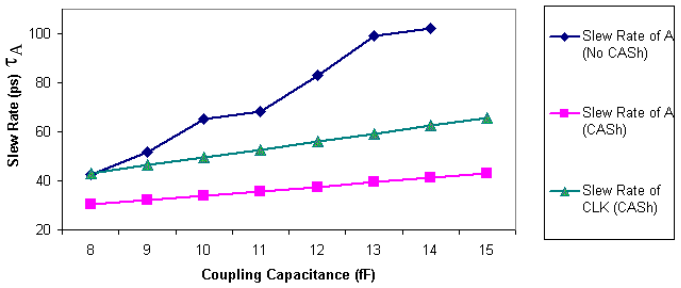
$$\int_{\tau_{n1}}^{\tau_p} \kappa^p \nu^p_{sat} C^p_{ox}(V_{dd} - V_{clk}(t) - V_{tp})dt - \int_{\tau_{n1}}^{\tau_{n2}} I_k dt \quad (5)$$

In Eq. 5, $\nu^{n(p)}_{sat}$ is the saturation velocity of a short channel NMOS(PMOS) transistor. $\kappa^{n(p)}$ is a measure of the velocity-saturation degree of NMOS(PMOS), which is determined by the longitudinal electrical field. $C^{n(p)}_{ox}$ is the gate capacitance of NMOS(PMOS) [2].

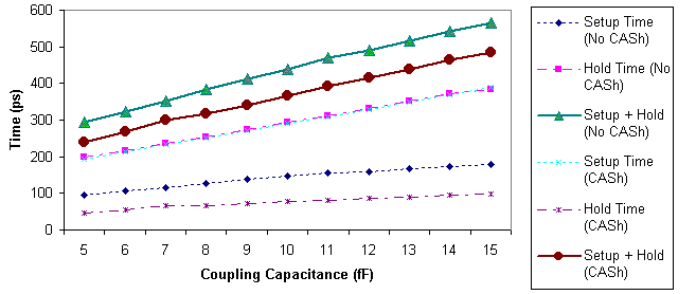
Theoretically, the upper bounds of τ_A and C_c can be obtained from the relationship between waveforms ($V_b(t)$ and $V_{clk}(t)$) and time stamps (τ_p, τ_{n1} and τ_{n2}) at $Q_{leak}(t)$ equal to $\frac{1}{2} C_L V_{dd}$ in Eq. 5. As depicted in Fig. 4(b), τ_{n1} and τ_{n2} are the time stamps when the noise induced on the victim node crosses threshold voltage, V_{tn} in upward or downward direction, respectively, whereas the aggressor waveform reaches $V_{dd} - |V_{tp}|$ at τ_p. Even though these waveforms and time stamps can be obtained through some simplification (See Appendix V), it is difficult to derive the exact closed formed expressions for τ_A and C_c. However, the approach presented in Appendix V may be useful in calculating both τ_A and C_c numerically when other parameters are known.

D. Benefits of CASh

Two merits are expected from CASh: one is the prevention of functional fault, and the other is the reduction of buffer size at iso-noise immunity. The former is achieved in conjunction with the concept of *rake clock* (Fig. 5). In general, signal lines are more than one in a domino gate. In order to effectively shield signal lines, the clock line should be divided and inserted between signals, and then merged again at the gate of the precharge PMOS. It is required to do post-processing of clock redistribution in the area of interest, since clock is usually pre-laid out at the early stage to satisfy a given performance. This scheme can be applied in a straightforward way only when the spacing between signal wires is not a minimum distance determined by lithographic limit. If signal wires are apart by the minimum spacing, the spacing between them should be widened to make room for clock insertion. In this case, area overhead increases, however C_c between the clock and signal line remains the same as before. The possible clock skew caused by the branch length l_2 can be neglected since l_1 is much larger than l_2 in Fig. 5. We refer to the clocking scheme as rake clock after its appearance.



(a) Slew rates with no functional fault



(b) Setup + Hold for non-CASh and CASh

Fig. 6. Results of experiment 1

Another application of CASh is in buffer size minimization while meeting the specifications of delay and dynamic noise margin. For the 2-input domino AND gate, the increase in the size of the buffer feeding a victim node is favored in order to suppress the possibility of functional fault. This method requires extra area. CASh can be applied to effectively immunize a circuit against external aggressors without enlarging buffers. These two benefits are demonstrated by HSPICE simulations in the following section.

III. EXPERIMENTS

HSPICE simulations are shown in this section to demonstrate the superiority of CASh over conventional methods. A simple 2-input domino AND gate is used to determine if CASh works well w.r.t. the prevention of functional fault and buffer size reduction. For other gates such as OR, the cross-talk between signals do not induce any functional failure. Thus, OR gate is not considered in our experiments. Results on 4-bit and 8-bit full adders are shown next.

A. Experiment 1 - Functional Fault in 2-Input Domino AND

Two different cases for a 2-input domino AND gate (Fig. 2) were considered to determine whether functional failures occured if C_c increases from $8fF$ to $15fF$. For each value of C_c, the input signal speed was increased from $200\,MHz$ to $10\,GHz$.

Assuming that rise time is about a tenth of a given clock period, 200 ps and 5 ps are assigned as rise times for 200 MHz and 10 GHz signals, respectively.

In the case of non-CASh, functional fault (which does not occur up to $C_c = 8fF$) starts to occur at some faster τ_A for C_c, ranging from $9fF$ to $14fF$. If C_c exceeds $14fF$, the gate always malfunctions even at the slowest slew rate, or $\tau_A = 200\ ps$. On the contrary, if CASh is used for the same design, no functional fault is observed for any τ_A or for any C_c between $9fF$ and $15fF$. Surprisingly, the gate in CASh-style functions properly even at $C_c = 40fF$ (which is much larger than what is expected in practical design in a $0.25\mu m$ technology and below). Fig. 6(a) shows the slew rates of aggressors when no functional fault occurs. It can be noticed that the gate functions correctly. The slew rates in the case of CASh are much steeper than that of non-CASh as shown in Fig. 6(a). This is an outstanding feature of CASh.

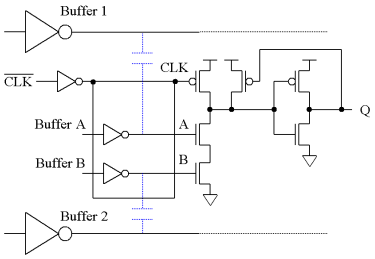
Setup time is defined as the time taken for a victim node to settle down from its disturbed state caused by CLK during the precharge mode, whereas *hold time* is defined as time taken for the victim node to stabilize from disruption induced by the aggressor during the evaluation mode (Fig. 3). This setup time increases as C_c becomes large, thereby threatening the desired performance. When the sum of setup time (τ_{setup}) and hold time (τ_{hold}) is compared between non-CASh and CASh designs in which there is no functional fault, CASh still shows better result (shorter time) than non-CASh (Fig. 6(b)).

B. Experiment 2 - Buffer Size Reduction in 2-Input Domino AND

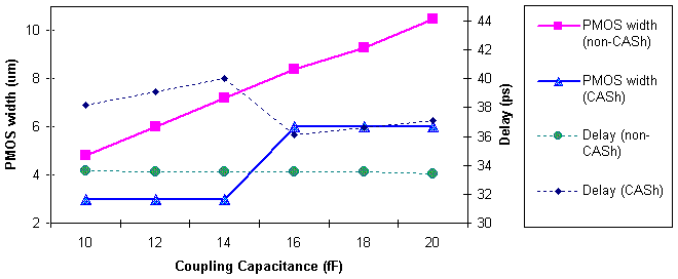
Another merit of CASh (i.e. buffer size reduction for iso-noise immunity) is established using the following experiment. Fig. 7(a) shows an example of applying CASh to a 2-input NAND, which otherwise is susceptible to coupled noise by the buffers (Buffer 1 and 2). Let us assume that a delay constraint imposed on this gate is $40ps$. Even though buffers (denoted *Buffer A and B*) with $P_{width}/N_{width} = 3.0/1.0$ (denoted *3.0/1.0 buffer*), meets the delay specification, the buffers should be enlarged to avoid functional fault in case of non-CASh. If CASh is employed as shown in Fig. 7(a), the buffer can be reduced in size. Fig. 7(b) shows the reduction in the size of buffers while the given timing specification is still satisfied. For example, CASh uses only 6.0/2.0 buffer at $C_c = 20fF$, whereas a buffer of at least a 10.5/3.5 is needed in non-CASh case. Since it is assumed that the CLK line are squeezed between the wires driven by Buffer 2 and Buffer B in Fig. 7(a) and the spacing between the two wires remains the same as in non-CASh, the area overhead of using CASh is nearly zero.

C. Experiment 3 - Noise Immunity in a Full Adder

The same concepts were applied to 4-bit and 8-bit adders. Due to the non-inversion property of domino logic, an entire full adder cannot be implemented in an orthodox domino style. Instead, only the carry part is implemented in domino style, whereas the sum part is built the same way as in a Mirror adder [2]. Since there are three inputs, namely C_i, A and B, to a single bit adder, CLK lines are inserted between each pair of the signals in order to apply CASh (Fig. 8(a)). In order to reduce area overhead, the inserted CLK line width was made half of the original width. We measured the values of C_c in which functional error occurs and the sum of setup time and hold time with varied C_c. We measured hold time w.r.t. carry output and sum output separately. However, only the sum of the setup time and hold time w.r.t. carry is plotted in Fig. 8(b)

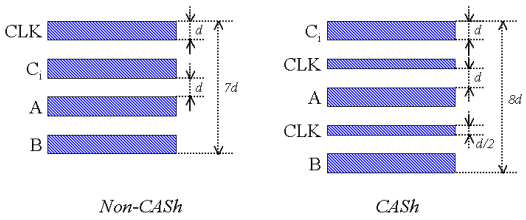


(a) Another application of CASh into the 2-input domino AND gate

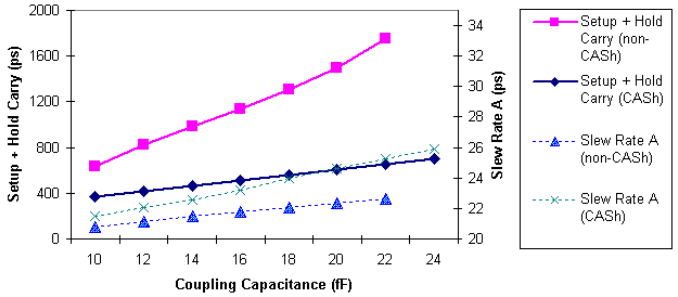


(b) Comparisons of buffer size and delay

Fig. 7. Circuit and results of experiment 2



(a) Application of CASh for a full adder



(b) Comparisons of the sum of setup time and hold (carry) time

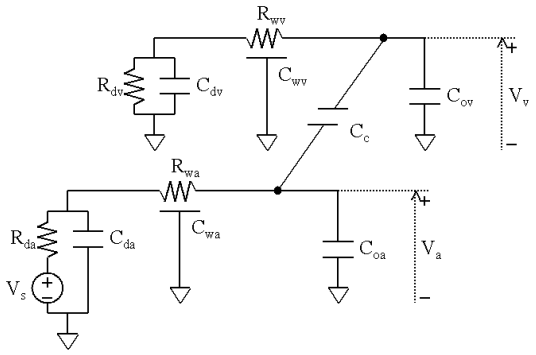
Fig. 8. Results of experiment 3

because this is the critical delay in adder circuits.

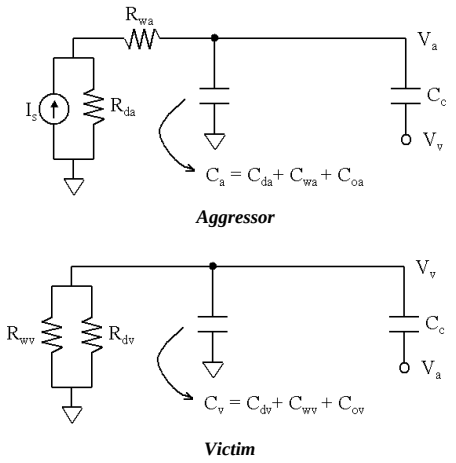
As seen in Fig. 8(b), the adder in a conventional layout style suffers from functional failure when C_c exceeds $22fF$, which does not cause any malfunction in a CASh styled adder. Furthermore, CASh shows outstanding result in terms of the sum of setup and hold times.

IV. CONCLUSIONS

In this paper, the basic concept of CASh, a novel methodology of using clock lines as shielding wires in domino circuits, is explained. CASh can be used to effectively reduce the possibility of functional fault due to cross-talk noise. In addition, the size of buffers driving long interconnects can be reduced us-



(a) Modeling aggressor and victim nodes



(b) Simplification of aggressor and victim

Fig. 9. Modeling and simplification of a pair of aggressor and victim

ing CASh, while meeting a given delay and a noise immunity specification. These two potential benefits are confirmed by HSPICE simulations on domino circuits. In conclusion, CASh can be applied to GSI applications, which demand both high noise immunity and high performance even under the worst operating conditions caused by increasing cross-talk over different technology generations.

V. Appendix : Derivation of $V_a(t)$, $V_v(t)$, τ_p, τ_{n1}, and τ_{n2} in $Q_{leak}(t)$

A. Simplification of the Differential Equations

Two neighboring wires, an aggressor and a victim, are modeled in Fig. 9(a) by using RC network. Each line can be further simplified into Fig. 9(b). Then we can have two differential equations (expressed after Laplace transform) as follows:

$$\begin{aligned}(C_a + C_c)sV_a(s) - C_c sV_v(s) + \frac{1}{R_{da}+R_{wa}}V_a(s) &= \frac{1}{R_{da}+R_{wa}}V_s(s)\\ (C_v + C_c)sV_v(s) - C_c sV_a(s) + \frac{1}{R_{dv}+R_{wv}}V_v(s) &= 0\end{aligned} \quad (6)$$

Though the solution of Eq. 6 turns out to be very complicated, it can be simplified with a simple yet useful insight on domino circuits: $V_v(s)$ in Eq. 6 can be considered to be small because, in CASh, a CLK line (aggressor) is hardly affected by other signal lines (victims) due to high driving capacity and large ground capacitance. With such simplification we get, Eq. 7 are the closed forms of voltage waveforms of aggressor and victim when a step input is applied.

$$\begin{aligned}V_a(t) &= V_{dd}(1 - e^{-t/\tau_a})\\ V_v(t) &= \frac{V_{dd}C_L G_a}{C_v G_a - C_a G_v}(e^{-t/\tau_v} - e^{-t/\tau_a})\end{aligned} \quad (7)$$

From Eq. 7, the voltage waveform on the victim ($V_v(t)$) can be interpreted as a superposition of two exponential waveforms. More accurately, it is obtained by subtracting discharging waveform on the aggressor (the faster) from that of the victim (the slower).

B. Obtain τ_p, τ_{n1} and τ_{n2}

τ_p can be obtained directly from $V_a(t)$ in Eq. 7 by equating $V_a(t)$ to $V_{dd} - |V_{tp}|$ at $t = \tau_p$. Then,

$$\tau_p = -\tau_a \ln\left(\frac{V_{dd}}{|V_{tp}|}\right) \quad (8)$$

To determine τ_{n1} and τ_{n2}, we should use τ_1, at which the waveform on the victim reaches a peak point. τ_1 is easily obtained by finding a root of $dV_v(t)/dt = 0$ and expressed as $\frac{\tau_a\tau_v \ln(\tau_v/\tau_a)}{\tau_v - \tau_a}$. The peak voltage value at $t = \tau_1$, V_p is obtained as follows:

$$\begin{aligned}V_p &= V_v(\tau_1)\\ &= \frac{C_c}{C_c + C_v}V_a(\tau_1)\\ &= \frac{C_c}{C_c + C_v}V_{dd}\left(1 - \exp\left(-\frac{\tau_v \ln(\tau_v/\tau_a)}{\tau_v - \tau_a}\right)\right)\end{aligned} \quad (9)$$

Between τ_{n1} and τ_{n2}, the victim voltage waveform is above V_{tn} (Fig. 4(b)). Hence, Eq. 9 can be used to obtain τ_{n1}. τ_{n2} is determined by approximating the victim waveform as exponential from time τ_1 and τ_{n2}. See Eq. 10 and Eq. 11.

$$\begin{aligned}V_v(t = \tau_{n1}) &= \frac{C_c}{C_c + C_v}V_a(\tau_{n1}) = V_{tn}\\ V_a(\tau_{n1}) &= \frac{C_c + C_v}{C_c}V_{tn}\\ V_{dd}(1 - e^{-\frac{\tau_{n1}}{\tau_a}}) &= \frac{C_c + C_v}{C_c}V_{tn}\\ \therefore \tau_{n1} &= -\tau_a \ln\left(1 - \frac{C_c + C_v}{C_c}\frac{V_{tn}}{V_{dd}}\right)\end{aligned} \quad (10)$$

$$\begin{aligned}V_{tn} &= V_p e^{-\tau_{n2}/\tau_v}\\ \therefore \tau_{n2} &= -\tau_v \ln\left(\frac{V_{tn}}{V_p}\right)\\ &= -\tau_v \ln\left(\frac{C_c + C_v}{C_c}\frac{V_{tn}}{V_{dd}}\frac{1}{1 - \exp\left(-\frac{\tau_v \ln(\tau_v/\tau_a)}{\tau_v - \tau_a}\right)}\right)\end{aligned} \quad (11)$$

Finally, if τ_p, τ_{n1} and τ_{n2} obtained above are substituted into Eq. 5, the upper bounds of C_c and τ_a can be numerically evaluated.

References

[1] James D. Meindl, "Gigascale integration:is the sky the limit?", *IEEE Circuits and Devices*, November 1996.

[2] J. M. Rabaey, *Digital Integrated Circuits : A Design Perspective*, Prentice-Hall, 1996.

[3] D. Somasekhar, S. H. Choi, K. Roy, Yibin Ye, and Vivek De, "Dynamic noise analysis in precharge-evaluate circuits", *Design Automation Conference*, June.

[4] L. Wang and N. R. Shanbhag, "Noise-tolerant dynamic circuit design", *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 549–552, 1999.

[5] G. Balamurugan and N. R. Shanbhag, "A noise-tolerant dynamic circuit design technique", *Customized Integrated Circuits Conference*, 2000.

[6] L Gal, "On-chip cross talk - the new signal integrity challenge", *IEEE Custom Integrated Circuits Conference*, 1995.