CAD Solutions and Outstanding Challenges for Mixed-Signal and RF IC Design

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Abstract

This tutorial paper addresses the problems and solutions that are posed by the design of mixed-signal integrated systems on chip (SoC). These include problems in mixed-signal design methodologies and flows, problems in analog design productivity, as well as open problems in analog, mixed-signal and RF design, modeling and verification tools. The tutorial explains the problems that are posed by these mixed-signal/RF SoC designs, describes the solutions and their underlying methods that exist today and outlines the challenges that still remain to be solved at present. In the first part the design of analog and mixed-signal circuits is addressed, while the second part focuses on the specific problems raised by RF wireless circuits.

1 Introduction

The growth of wireless services and other telecom applications increases the need for low-cost highly integrated solutions with very demanding performance specifications. This requires the development of intelligent front-end architectures that circumvent the physical limitations posed by the semiconductor technology. In addition, with the evolution towards nanometer CMOS technologies, the design of complex systems on a chip (SoC) is emerging in consumer-market applications such as telecom and multimedia. These integrated systems are increasingly mixed-signal designs, embedding high-performance analog blocks and possibly sensitive RF frontends together with complex digital circuitry on the same chip.

This tutorial paper addresses the problems and solutions that are posed by the design of such mixed-signal integrated systems. These include problems in design methodologies and flows, design productivity, design, modeling and verification tools. The tutorial explains the problems that are posed by these mixed-signal/RF SoC designs, describes today's solutions and their underlying methods, and outlines the challenges that still remain to be solved at present.

The paper is organized as follows. Section 2 addresses the design of analog and mixed-signal circuits, while section 3 focuses on the specific problems raised by RF wireless circuits. The conclusions are then provided in section 4, followed by an extensive list of references.

2 Analog and mixed-signal ICs

Figure 1 shows a typical mixed-signal IC that integrates several memories (RAM and ROM), random logic, a small CPU core, along with an analog signal processing frontend. This particular design comes from the automotive industry, but is fairly illustrative of the sort of designs we are concerned with in this section.

Before describing problems and evolving solutions in the design of these chips, it is worth first summarizing why "analog" in general poses such a different set of design problems than do digital ICs.

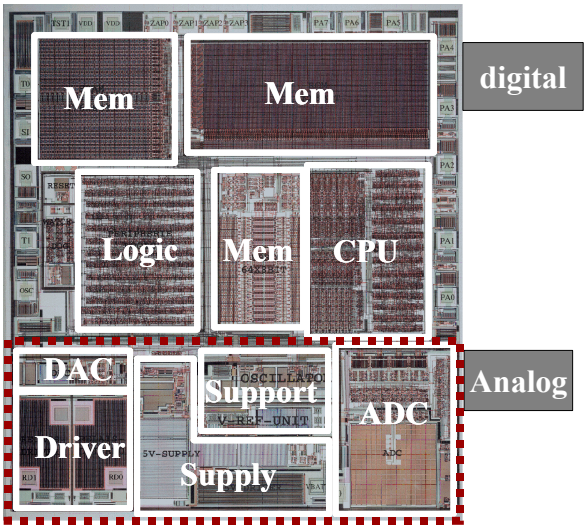


Figure 1. A typical mixed-signal SoC design.

2.1 About analog IC design

Two misperceptions are common when non-analog designers look at these sorts of designs. We can summarize these as:

- *Misperceptions about size:* how can these designs be so difficult when they are so small—seemingly just a few transistors?
- *Misperceptions about libraries:* even if these designs are difficult, why can't we just build them once, store them in a library and reuse them at will? Isn't it true that we just need some "standard" A/D and D/A converters, filters, phase locked loops (PLLs), and so on?

Consider first the "size" issue. The analog part of a typical mixed-signal SoC is typically a small fraction of the total number of devices; 15,000 to 25,000 devices seems a common range for the number of analog devices. But as shown clearly in the figure above, this minority of devices can easily translate into one fourth or even one half of the silicon area of a mixed-signal chip. Analog devices are typically very large, to handle large currents for external interfaces, and to guarantee the precision necessary in many analog signal processing tasks. These precision requirements are really at the heart of why analog circuits are difficult to design.

Unlike digital circuits, analog circuits exploit rather than avoid the physics of the fabrication process. Analog circuits manipulate precise analog quantities—voltages, currents, charge, and continuous ratios of parameter values such as resistance or capacitance. As such, they are not insulated from the physics of the manufacturing process by nice abstractions such as logic values, or noise margins. As a result, second-order and third-order effects that are not so critical for digital design become first-order problems for analog designs.

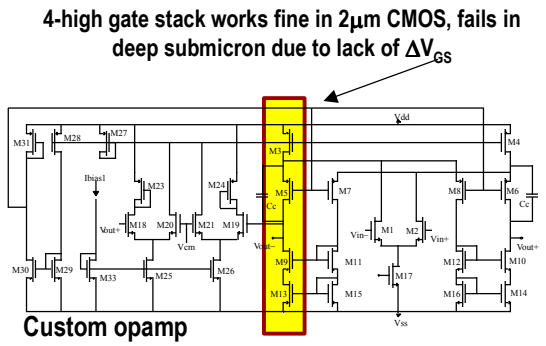


Figure 2. Example of voltage scaling impact on analog.

This problem is only getting worse as we head deeper into extremely scaled nanometer designs. For example, voltage scaling in modern processes has already had a profound impact on the way we design analog circuits. Many classical circuit topologies use transistor stacks (source-drain connected FETS in series between a pair of power rails) with too many devices in series; these are no longer feasible, due to a lack of ΔV_{GS} across the stack. The figure above shows one custom amplifier design from 1992 [31] that cannot work in today's scaled technologies.

Now, let us consider the second problem: if these designs are difficult to create, why not create them once, and save them in a library? The central problem is that analog circuits have many continuous parameters, unlike most digital circuits. Consider a digital standard cell library. It contains probably 500 to 1500 cells, which we can regard as the rough product of 10 different logic functions (NAND, NOR, flip flop, etc.), 10 different input/output alternatives per function (NAND2, NAND4, flip flop with preset, with clear, etc.), and 10 different timing and power alternatives per cell. But even a small analog cell can have a dozen continuous parameters, and if we try to create versions of the cell with each parameter set to some sensible "high" and "low" value, we need 2^{12} = 4096 libraried implementations of this cell. Now, not all of these will be sensible designs, but it easy to create hundreds of useful variants for a given analog circuit topology just by resizing the devices to meet different performance requirements.

A further problem is that analog circuits resist technology migration and retargeting (see Figure 3 below). Because of their tight dependence on the specifics of the fabrication process, even small changes—in the performance of devices, in the parasitics associated with interconnect or substrate, or in the desired performance specification—can require a substantial redesign of the circuit.

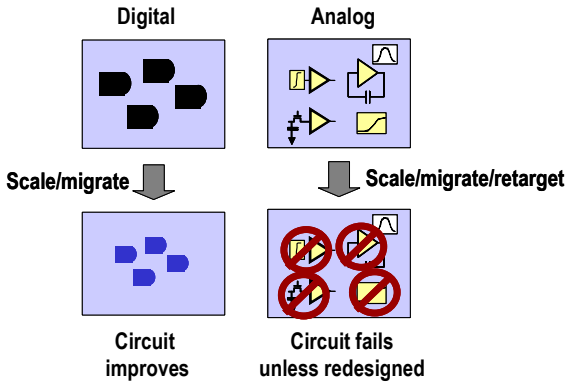


Figure 3. Contrasting the difficulty of migrating/scaling digital and analog circuits

Digital circuits tend to work better—faster, less power, smaller—as we migrate them to new processes. Analog circuits certainly benefit from higher feasible operating frequencies, but suffer from the difficult voltage scaling, and the fact that the devices themselves are really optimized for digital logic switching, and not analog precision. Indeed, it is still common for aggressive analog designs to require extra device characterization work to create models with the fidelity needed for high-performance applications (e.g., high precision tasks that require extreme device matching, precision passive devices such as resistors or inductors, etc).

2.2 Challenges in analog design methodology and tools

Today, work on analog design methodology focuses mainly on two related problems: *rapidness*, and *correctness*. Analog designs have a reputation—unfortunately well deserved—for long design times. Rapid design is all about reducing the design cycle for these difficult circuits. Emphasis is on design discipline, reuse of analog intellectual property (IP), and design automation. Correct design is all about increasing the likelihood that a mixed-signal design work on first silicon. Indeed, many analog design projects still routinely plan multiple silicon spins just to ensure that problems unknown during the design can be uncovered, diagnosed and repaired using silicon prototypes.

An important area of recent concern is the need to improve *design capture* for the analog side of mixed-signal designs. Disciplined top-down methodology has come late to the analog community, in part because of the tight coupling across layers of the analog design hierarchy. Process and device characteristics may be cleverly exploited by custom circuit topologies and system architectures to achieve some aggressive performance specifications. Change anything in this hierarchy—a process parameter, a device model, a critical specification on a critical analog cell, etc.—and one risks radically compromising the overall design. Hence, it is vitally important in any attempt to use top-down strategies to be able to document where these sorts of dependencies arise, and how the specifics of implementation choices affect these dependencies.

There is considerable hope that the recent evolution of hardware description languages (HDLs) to support analog and mixed-signal behaviors (the so-called "AMS" HDLs) will address this problem. These AMS HDLs support both continuous analog modeling, usually with a SPICE-like ordinary differential equation-solving (ODE) numerical engine, and discrete-event digital modeling. Also, they support not only simple structural descriptions (gates, transistors, wires), but also behavioral descriptions, with primitives for numerical derivatives, frequency-domain transfer functions, etc., built directly into the engine. Thus, one can describe an analog circuit as either a collection of devices simulated with SPICE-like accuracy, or as a set of more idealized blocks, with appropriate behaviors modeled as equations (e.g., we can write I = C dV/dt directly, if we choose to). Verilog-AMS and VHDL-AMS are the HDLs garnering the most attention here; see [32, 33] for relevant information about these languages.

Most visions of top-down design here assume that it is possible to specify the desired behavior at some level of the design hierarchy, and use this specification to derive the necessary behaviors of the components at the next level of design detail. HDLs play an essential role here: it is assumed that an abstract version of each sub-block is created early and used to verify system-level function, but that subsequent design refinements are "backannotated" into appropriately updated model refinements for more careful verification of system correctness. Kundert *et al* [34] and Gielen [17] are good surveys of these ideas.

However, there remain some significant holes in this vision of an integrated top-down flow. We argue that the two of the most important of these are:

- *Predictive top-down modeling:* in digital designs, we have rough models of resource usage fairly early in the design process, for example, how big or how fast a block of random logic can be. We can even make some decent predictions from RTL inputs today. The capability is far less mature for analog designs. Predictions of area, or power, or noise, are still mostly based on human expertise. There is some recent work in the area, e.g. [35], but the wide range of analog end applications makes this challenging.
- *Nonlinear macromodeling:* in digital designs, we have some capabilities for characterizing our basic bocks (e.g., gate-level modeling of delay and power for standard cell libraries), and backannotating relevant information from detailed design "back" up onto a more abstract description. These capabilities are much less mature for analog. A particular problem that seems highlighted by advances in AMS modeling is our inability to create automatically a nonlinear macromodel for an arbitrary circuit-level block, for example, an opamp, comparator, voltage reference, or mixer. Top-down methodology assumes we create idealized models to verify our top-level analog architecture, but then reverify later by replacing these ideal models with more accurate, yet still simplified, macromodels. These macromodels represent the "real" circuits we have designed to implement each of these idealized blocks. Simplification is essential to be able to perform sufficient simulations to verify a complex system. Practical methodologies that try to stay "top down" today usually resort to a hodge podge of *ad hoc*, mostly manual modeling strategies to build these models. This is obviously fraught with peril: if our refined system simulation fails, is it because we mis-modeled a critical analog concern, or is the system really compromised by unexpected second-order effects in the circuit realization of each block? Some efforts have appeared recently, e.g., [36, 37], but the lack of a truly general solution is increasingly a problem.

Another active area of late is *analog synthesis*, along with related work on *analog intellectual property*. Reuse has become an enormously important area in digital SoC design, with much investment in methodologies for reuse of layouts, of netlists, and of parameterized/compilable design blocks, and the development of appropriate implementation platforms that allow configurability, yet minimize custom design. Synthesis is a critical part of most visions for analog IP—just as RTL / logic synthesis, coupled with backend physical synthesis, occupies central roles in today's evolving strategies for digital IP.

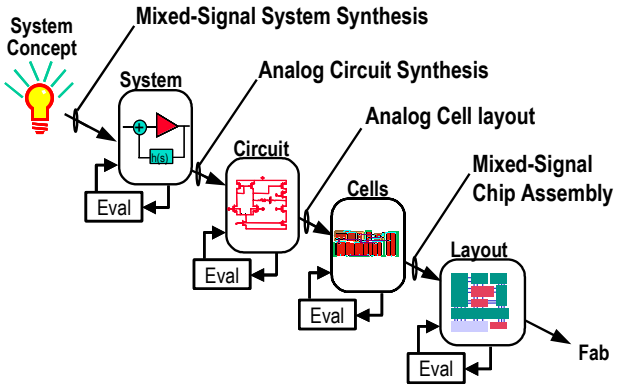


Figure 4. Synthesis flow for Analog & Mixed-Signal

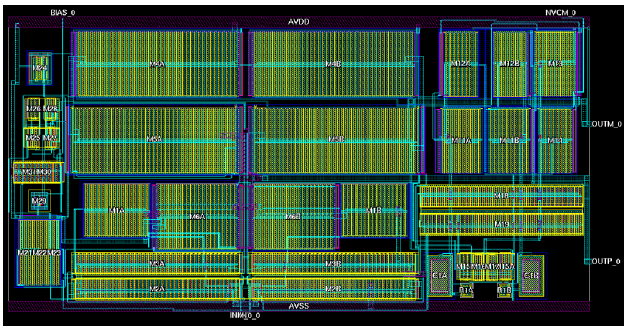
Figure 4 shows an "idealized" version of an analog synthesis flow. There has been remarkable progress over the last few years in the area, with several commercial offerings starting to appear. Gielen and Rutenbar [38] offer a recent survey of the area. Most of the basic techniques in the area rely on numerical and geometric optimization engines coupled to "evaluation engines" that qualify the merit of some evolving analog circuit or layout candidate. Recent progress in simulation-based synthesis, e.g., [39 – 41] has made it possible to couple robust numerical optimization with full SPICE simulation, making it possible for the first time to synthesize designs using the same modeling and verification tool infrastructure that human experts would use for manual design. Given the enormous investments in modeling and simulation that inevitably surround any analog design project, this is a significant and new capability in the area. Some other approaches argue instead for equation-based modeling of useful analog circuits, and emphasize simplifications in the modeling that render the optimization problem easier to solve. Recent work in this area focuses on convex models solved by geometric programming, as in [21,22,42].

By coupling improved design capture methodologies to archive essential constraints *on the schematic* (instead of inside the heads of the designers themselves) with analog circuit and physical synthesis, we have for the first time some credible strategies for analog reuse and analog IP. Figure 5 below shows one example of an industrial analog cell migrated from an older 0.6um technology to a more modern 0.35um foundry process, using one commercial analog synthesis flow from Neolinear [44].

Nevertheless, there remain several significant challenges in the design of the analog side of any mixed-signal SoC. We enumerate several of these below:

- *System-level synthesis for analog*: most analog synthesis efforts have targeted basic building blocks. The next significant challenge is evolving techniques that can handle

Industrial analog cell synthesized
for proprietary 0.6um CMOS fab



Same industrial analog cell,
resynthesized to migrate
to standard TSMC
0.35um foundry process.
Migrated cell is 78% smaller,
and consumes 42% less power.

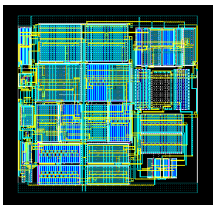


Figure 5. An industrial example of using synthesis in support of reusable analog IP. (Courtesy Neolinear, Inc.)

system-level designs. Recent efforts are still bound closely to specific application domains (e.g., [16]) and require of their users (and tool creators) extensive domain expertise. Some work on simulation-based synthesis has emerged [41, 24], but there is much more work to be done. Macromodeling again plays a crucial role here, in simplifying these complex systems to the point that the expense of synthesis search can be made tractable.

- *Chip-level assembly for mixed-signal:* this is the physical design problem of layout for multiple sensitive analog blocks and (probably) noisy digital blocks at full chip level. Today, this is an embarrassingly *ad hoc* process. Defensive tactics, involving guard rings and other isolation structures for the analog parts, along with some careful methodology for the design of the chip-level power distribution and IO pin assignment, are the dominant strategies we have today. However, these are often over-designed, or worse, incorrectly designed. Layout here is still mostly a combination of manual floorplanning coupled with auto/interactive chip-level routing using routing features originally intended for (and evolved from) high-speed board design. There are some early efforts at layout automation here [44-47], but the problem remains quite open.
- *Chip-level verification for mixed-signal:* Part of the physical design problem is a lack of adequate full chip analysis tools. Some tools have recently emerged to assist here: tools for full chip power grid analysis [48], and for full chip substrate analysis [49]. However, we still lack tools with the capacity to handle the full chip and also the speed to be able to see dynamic effects like substrate or power grid bounce, which may require very many cycles of transient simulation to setup and diagnose.

Many of these problems become, unfortunately, worse, as we increase frequency from the "analog" regime to RF, in particular, the difficulties of creating adequate macromodels, and verifying large-scale coupling at chip level. We address these sorts of challenges next.

3 CAD solutions and problems for RF IC design

3.1 Evolution in RF circuit design

The field of telecommunication design is recently confronted with an explosive growth in wireless mobile phones. The success of standards like GSM and DECT forced industry to put more research in realizing more system functionality on a smaller size, while consuming less power and reducing the overall price of the product [1,2]. For instance, in 1994 the second generation of GSM radio came on the market. This mono-band system had a total of 270 components. Five years later this was reduced to 130 components while the functionality was upgraded to a dual-band system. A reduction of 50% in components, 50% in PCB area and more than 60% in RF PCB area had been achieved. This consumer product example shows how in a few years time a large evolution has been achieved.

At least three trends can be observed in RF systems if we look over the last decade:

- The carrier frequency for cellular mobile communication will stay between 800 MHz and 3 GHz. However, in wireless data communication the trend is towards carrier frequencies deep into the microwave band, e.g. 5 GHz for IEEE802.11a, 17 GHz and 60 GHz for ETSI BRAN/HIPERLAN.
- In the early nineties, the RF circuitry was mainly designed in an (expensive) GaAs technology. Currently, all RF front-ends in cellular mobile phones are realized in BiCMOS technology processes, some having special RF options. We can observe a trend towards integration in advanced CMOS technologies for wireless data communication systems.
- The existence of dedicated RF BiCMOS technologies allows for fully integrated RF front-ends including the data converters, instead of having separate chips per functionality. The evolution towards deep submicron CMOS technologies with RF capabilities allows even for complex RF systems on a chip (RF SoC), i.e. RF front-end plus (parts of the) baseband integrated together.

The design of these complex RF front-ends and RF SoC demands for dedicated CAD tools. For instance, the first trend indicates that applying lumped-element theory is no longer valid and transmission line concepts have to be applied. The first and second trends reflect the need for dedicated RF simulation models for the active and passive components used in the circuits. The third trend requires CAD tools capable of handling difficult problems such as substrate noise coupling, and electromagnetic analysis combined with current/voltage analysis.

3.2 Evolution in CAD for RF applications

RF front-ends are constructed primarily using a few basic blocks, e.g. amplifiers, mixers, oscillators and prescalars. Analog amplifiers are common blocks in standard analog design and are well handled by SPICE-like simulators. Although the simulation of RF low-noise amplifiers is basically not different from analog amplifiers, specification parameters like noise figure, (delivered) power gain and intercept point require small adaptations in mainly the post processing.

This does not hold anymore when, for instance, an RF power amplifier must be analyzed. The carrier frequency at the input is a large signal, indicating that the operating point is periodic in time. The carrier frequency is normally modulated in amplitude and phase. This means that small-signal analysis must be performed based upon the results of the periodic analysis. These so-called (quasi) periodic steady-state and AC analysis can be seen as RF extensions of SPICE-like DC and AC analysis. The intrinsic nonlinear behavior of mixers and oscillators causes spectral folding, complicating noise analysis. The time-varying operating point modulates the noise sources and, even more, the noise transfer function from the noise sources to the output is also periodically time-varying. In both cases the mechanism is referred to as being cyclostationary. This requires extensions to the standard analysis tools. The theory and methods to speed these techniques up for large practical circuits have been developed extensively in recent years. A good overview can be found in [3-6]. These RF techniques are now available within commercial RF simulators such as Cadence's Spectre-RF, Agilent EESof's ADS, and Mentor's ELDO-RF.

Although we will mainly focus on analysis tools here, also academic research tools for the synthesis and layout generation of RF circuits exist. However, these tools are still in their infancy and not used in industrial environments yet. They will be discussed briefly later on.

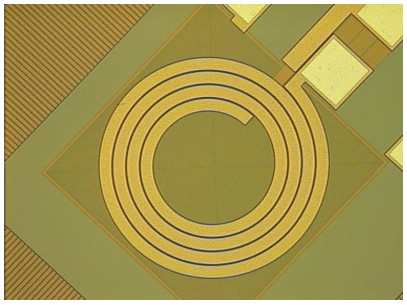


Figure 6. Integrated planar inductor coil.

3.3 Capabilities and limitations in existing RF analysis tools

Let us consider the design of a dedicated quadrature VCO, a key RF block. One of the main concerns is the design of the inductor. To find the proper geometric layout, simulation tools like Momentum and ASITIC [7] can be used. These CAD tools use a combination of electromagnetic analysis and analytical expressions to calculate the inductance and quality factor as function of the frequency. We have verified the accuracy of these tools with the measured performance of more than 50 inductors in a 0.18 µm CMOS technology on 10 Ω.cm substrate. An example of one of the inductors is shown in Figure 6.

Name	Measured			ASITIC (simulated)		
	L [nH]	Q [-]	Fres [GHz]	L [nH]	Q [-]	Fres [GHz]
L5N400T	4.3	9.7	9.9	4.5	12	4
L5N300T	3.9	10.9	12	4.1	12	5.9
L6N400T	5.7	10.1	8.3	7	10	3
L6N400shield	6.0	10.2	6	7	10	3
L6N500T	9.8	7.5	5.8	7.3	9	3
L5N500T	5.2	10.5	7.7	5.3	12	3.5
L5N400shield	4.6	10.0	6.5	5.4	15	3
L5N300shield	4.0	10.5	9	4.9	15	5
L5N200shield	3.7	9.1	9.2	4.5	11	8
L6N300shield	5.0	9.5	7.8	6.3	13	4
L6N200shield	4.7	8.5	10	6	11	6
L1N400	0.7	10	>18	0.8	19	15
L2N200	1.7	7.8	10	1.6	8.7	12
L2N300	1.7	8.2	7.6	2	23	7

Table 1. Simulated and measured performance of inductors.

The results in Table 1 indicate that, on average, ASITIC [7] (as well as other similar tools) is too optimistic in predicting the inductance and quality factor Q, and too pessimistic in predicting the resonance frequency. Because the inaccuracy is more than 10%, this kind of tools are not very useful for industrial applications. Even worse is the fact that these tools are not capable in predicting the influence of shields beneath the inductor. These shields are needed to avoid substrate noise coupling, but influence the performance of the inductor. One of the main problems in these tools is the incapability to provide the exact geometric situation and proper doping levels of the used technology.

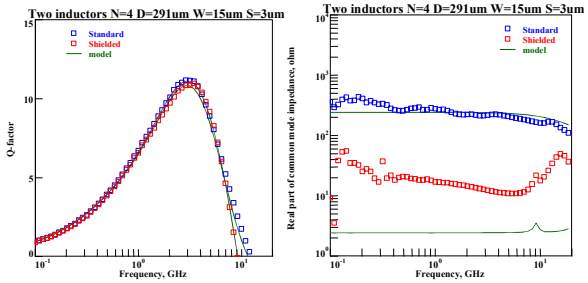


Figure 7. Comparison of Q factor and DC resistance between L5N300T (without shield) and L5N300shield.

To overcome the mentioned problems, a scalable equivalent circuit model suitable for both AC and transient circuit simulation of planar spiral inductors on silicon substrates has been developed at Philips. The model can accurately predict the performance of an inductor with diameters between 200 and 500 µm, number of turns ranging from 1 to 7, and inductances between 0.2 nH and 9 nH for frequencies up to 40 GHz. It can be seen that the prediction of the DC resistance for a shielded inductor is still a problem, see Figure 7. If, from this model, the exact geometry and parameter values of the inductor are known, a PCELL directly generates the layout.

Now let us assume that the RF engineer has a good RF model for the inductor; this can then be used during the design of the VCO. One of the most debated topics in literature is the subject of phase noise in oscillators, defined as the ratio between the power of the side band component at an offset frequency Δω and the power of the carrier [8-9]. In general, the calculation of phase noise consists of two steps. In the first step one obtains the periodic steady-state (PSS) solution $x_s(t)$ of the noiseless system. In the second step the phase noise can be calculated by applying a nonlinear perturbation analysis, resulting in the phase $\varphi(t)$ [10]. Finally solving $v_o(t) = A(t)\cos(\omega_o t + \varphi(t))$ leads to the phase noise. The solution in the second step could be calculated with the Impulse Sensitivity Function (ISF) method [11]. Instead of nonlinear perturbation analysis, linearization around the PSS solution can be performed to study the noise as a small signal perturbation (PNOISE analysis, see [12]).

Frequency offset	Simulated (Spectre-RF)	Measured
10 kHz	-71	-60
50 kHz	-91	-82
500 kHz	-116	-108
1 MHz	-123	-115
2 MHz	-129.2	-120
3 MHz	-132.5	-128
400 MHz	-176	-174

Table 2. Simulated and measured VCO phase noise [dBc/Hz].

Although simulated and measured phase noise are in good agreement for large frequency offsets, this is not the case for phase noise close to the carrier (see Table 2). The VCO is made in a MOS technology for which the knee of the 1/f-noise is into the MHz range. Because the MOS models have a proper DC 1/f-noise fit, the inaccuracy is due to other reasons, e.g. the analysis routines do have problems with solving feedback systems with pulled oscillation, the solution algorithms do not properly take into account the frequency folding for this particular noise [13], and the 1/f-noise must be modeled as a nonstationary process [14]. It is clear that more research on this topic is needed.

Similar problems as for the analysis of VCOs exist for the analysis of mixers. In passive MOS device mixers there is no bias current flowing, only a non-zero time-varying drain current exists. Taking a single MOS device and simulating such conditions shows that 1/f-noise appears around DC and around even harmonics (see Figure 8). Measurements indeed showed 1/f-noise behavior around DC, but did not indicate the existence of the 2nd harmonic [15]. This discrepancy is still the subject of debates in the literature.

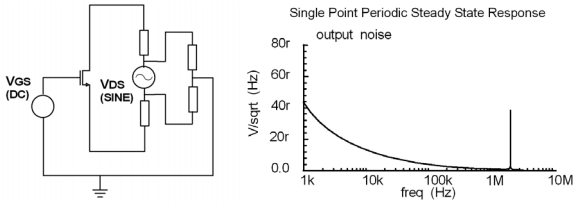


Figure 8. PSS/PNOISE simulation of a mixer circuit with 1 MHz sinusoidal signal.

Another important analysis tool that is getting more important when integrating more and more system functionality is architectural exploration at the system level [16]. Consider for example the digital telecommunication link of Figure 9. In order

for the entire system to meet the standardized requirements for the given application (e.g. GSM, WLAN, UMTS, etc.) at minimal power and chip implementation cost, a proper architecture for the receive and transmit front-ends has to be chosen and proper specifications for the front-end subblocks have to be determined (e.g. the number of bits in the A/D converter, or the IP3 of the LNA).

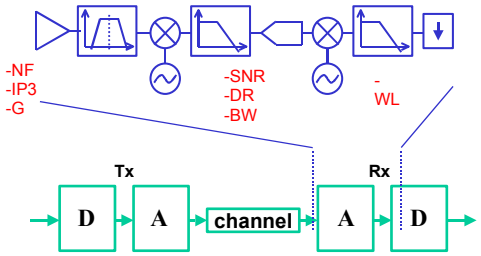


Figure 9. Digital telecommunication link, indicating a possible receiver front-end architecture.

The aim of a system exploration environment is to provide the system designer with the platform and the supporting tool set to fast explore front-end architecture alternatives and decide on subblock specifications based on quantified rather than heuristic information. Important in this context is a correct modeling of subblock nonidealities, but also a fast high-level simulation method. As these aspects are not sufficiently available in present commercial simulators, dedicated solutions need to be developed. ORCA for instance uses dedicated signal spectral manipulations to gain efficiency [17]. Figure 10 shows the spectrum at the output of some front-end, distinguishing clearly between the wanted signal, the noise, the distortion, aliased signals, etc., providing useful feedback to the system designer. More recent approaches use data-flow processing methods [18] or alternative signal bases [19].

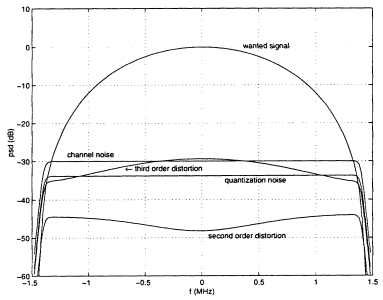


Figure 10. Spectrum at the output of a receiver front-end.

3.4 Other RF CAD tools

So far we have discussed analysis issues in RF design. Other important aspects, however, especially in the context of productivity gain for RF SoC design, are the automatic synthesis, i.e. optimal sizing and layout generation, of RF circuits.

Recently some prototype CAD tools for RF circuit optimization, although typically circuit-specific, have been presented. Since RF circuit performance is very sensitive to layout parasitics, the calculation or estimation of these parasitics is typically incorporated within the optimization loop. In [20] CMOS RF power amplifiers are optimized using a simulated-annealing-based custom tool. A compact inductor model enables the incorporation of parasitics as an integral part of the parasitic-aware design and CAD optimization. In [21-22] a CMOS VCO optimization tool is presented that applies geometric programming to a posynomial model of all circuit and spiral inductor characteristics.

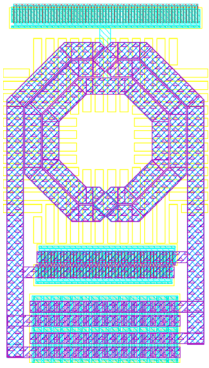


Figure 11. Full VCO layout generated with CYCLONE.

The CYCLONE tool [23] generates optimal CMOS RF LC-tank VCOs. Both the circuit's device sizes and the inductor coil parameters are globally optimized for the specified technology process as to meet the specifications (center frequency, tuning range, phase noise) at minimum power consumption. The tool automatically performs electromagnetic simulations for the on-chip inductor to exactly calculate its losses during the circuit optimization. It uses a template-based layout generation approach to obtain accurate predictions of the actual layout parasitics. See Figure 11 for an automatically generated VCO layout. The results depend on the characteristics of the target technology, as shown by the optimized coil parameters in Table 3.

Parameter	Technology	
	Low resistive substrate	High resistive substrate
Ls	1.81 nH	2.85 nH
Rs	0.95 Ω	0.74 Ω
Inner Rad, W, #Turns	134 µm, 22µm, 2	178 µm, 18 µm, 2
Used metal layers	3 top layers	All 4 layers
Power	12.8 mW	8.8 mW

Table 3. VCO parameters in two different technologies.

Ultimately, in order to get the best parasitic calculations, the layout generation will have to be integrated as a full part of the RF circuit optimization loop. This has been implemented in the gaRFeeld tool [24-25] that combines the power of a differential evolution algorithm with cost function response modeling and integrated procedural layout generation to synthesize RF CMOS low-noise amplifiers and mixer circuits.

Generating good RF layouts is one of the most delicate topics in the RF community. Currently, this is a full-custom task, no automation is involved. Needless to say that it is a time-consuming task and hence an expensive part in the complete design flow. This is mainly due to the fact that, especially in CMOS technology, engineers are still looking for the optimal layout of active and passive devices. For example, a standard digital layout for an 0.18 µm CMOS technology will result in a maximum oscillation frequency of 10 GHz for the nMOS and a finger layout structure (often used in the RF community) results in 60 GHz. Recently, within Philips new layout geometries have been developed, resulting in maximum oscillation frequencies beyond 100 GHz. Similar aspects are involved in the design of passive components, see for instance the planar inductor. Once such rules are available they can be incorporated in procedural generators (PCELLS) that automate the generation of individual devices, e.g. MOS transistors, spiral inductors, varactors, etc.

Some effort has been done in the automation of the full layout process [26-27] for entire analog circuits, incorporating many performance-degrading effects such as wire capacitance and resistance, crosstalk, thermal effects, mismatch. Recently, even the inclusion of substrate coupling has been taken into account by minimizing the coupling with neighboring modules depending on their relative positions according to [28]:

$$\text{minimize } \Delta P_i = \sum_j S^2_{SCi,j} \cdot \partial P_i / \partial(1/R_{i,j})(x_i, y_j) \cdot n_i$$

where $\partial P_i / \partial(1/R_{i,j})$ is the substrate coupling sensitivity of performance function P defined on module i, (x_i,y_j) reflects the Manhattan distance between the two modules, and $R_{i,j}$ represents the resistive substrate coupling between the two modules and is a function of their distance. In practice, the substrate model is more complex. The noisiness n_i of module i depends on both the amplitude and time derivatives of a predefined electric property. The above minimization can be seen as an additional constraint in the simulated annealing loop typically used in placement and routing algorithms. The problem of substrate-aware coupling lies in obtaining accurate information on the substrate sensitivity function.

In conclusion, a major effort is still needed before these CAD tools can automatically and optimally design and lay out high-performance RF circuits in industrial practice.

3.5 Challenges for RF SoC CAD tools

Integrating complete RF front-ends, eventually together with large digital circuitry, causes interesting problems. Currently no adequate CAD tools exist to tackle these problems. We will mention a few remaining challenges:

- *Integrated antennas:* Integration of antennas on silicon demands CAD tools capable of combined electromagnetic (EM) analysis and voltage/current analysis. Today these two forms of analysis are performed separately, but the information from the EM analysis is not easy to translate into lumped elements to allow for standard SPICE-like simulation.
- *VCO pulling:* A major problem in integrated front-ends is the pulling behavior between the two VCOs and between a VCO and a power amplifier. Both operate at similar frequencies and may interact with each other via substrate or electromagnetic coupling via the integrated planar inductors. No tools exist to adequately analyze this kind of behavior.
- *Substrate modeling and simulation:* The substrate becomes a major concern in RF design. Digital circuitry can inject spiky signals into the substrate, which then will be picked up by the sensitive RF circuits. As example, consider a VCO at 2.3 GHz and a digital circuit block (250kgates) running at 13 MHz. The digital clock is FM modulated around the VCO frequency and may cause conflicts with out-of-band emission requirements (see Figure 12). Although some CAD tools are available to tackle (parts of) this problem, it is still one of the major concerns in RF design [29-30].
- *Fast system-level analysis:* The analysis of complex modulation schemes like multi-carrier QAM (e.g. 64-QAM, 52 OFDM, used in IEEE 802.11a or HIPERLAN/2) is still difficult. Simple two-tone analysis is inadequate to get correct performance data for currently used transceivers. At this moment, tools like Cadence SPW and Ailent/EESOf ADS are used at the system level, but the problem remains difficult to verify a circuit with these kinds of complex signals within SPICE-like simulators.

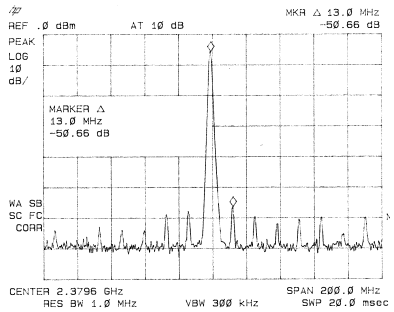


Figure 12. Measured FM modulation due to substrate switching noise coupling.

4 Conclusions

The last few years have seen some significant strides in both design methodology and CAD tool support for analog and RF designs. The emergence of AMS simulators has reenergized plans for "real" top-down design flows in many industrial scenarios. New simulators with higher capacity and the ability to handle RF's unique frequency domain requirements have appeared. Analog synthesis, both for circuit sizing and for physical layout, has appeared commercially in several competing formulations. There is an increasing emphasis on system-level modeling, analysis, and verification, in the research community.

However, several problems remain. Nonlinear macromodeling and the various sorts of "forward" predictive models and backannotated model information one would expect in a robust top-down design flow are *ad hoc* and inadequate. There remain behaviors unique to RF systems that are difficult to design for and verify. Chip-level physical assembly for sensitive mixed-signal designs is essentially unautomated. Chip-level verification, especially for substrate coupling effects, is incompletely handled, especially for higher frequency designs. As we move forward, we expect to see design scenarios in which complex systems are assembled from parameterized pieces, and we expect that at least some of the analog and RF blocks will be synthesized on demand or retargeted from prior designs, assembled under well-constructed high-level electrical constraints, and verified rigorously for correctness. As a result, we expect continuing pressures to keep innovating in tools and methodologies for these difficult but important circuits.

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