Coupled Analysis of Electromigration Reliability and Performance in ULSI Signal Nets

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Abstract

In deep submicron VLSI circuits, interconnect reliability due to electromigration and thermal effects is fast becoming a serious design issue particularly for long signal lines. This paper presents for the first time a rigorous coupled analysis of AC electromigration that are prevalent in *signal lines* and thermal effects arising due to Joule heating of the wires. The analysis is applied to study the effect of technology scaling using ITRS data, wherein the effects of increasing interconnect (Cu) resistivity with line dimensions and the effect of a finite barrier metal thickness have been included. Finally, we have also quantified the reliability implications for minimum sized vias in optimally buffered signal nets. Our analysis suggests that for the optimally buffered interconnects, while the maximum current density in the line remains limited by the performance, the current density in the vias exceeds the reliability limits and therefore requires careful consideration in the physical design process flow.

1 Introduction

1.1 Electromigration and Thermal Effects in ULSI Interconnects

As VLSI technology scales, interconnects are becoming the dominant factor determining system performance and power dissipation [1, 2]. Additionally, interconnect reliability due to *electromigration* and *thermal effects* is fast becoming a serious design issue particularly for long signal lines [3]. In fact, it has been recently shown that interconnect Joule heating in advanced technology nodes can strongly impact the magnitude of the maximum temperature of the global lines despite negligible changes in chip power density [4] which will, in turn, strongly affect the electromigration lifetime of the interconnect.

The ever increasing demand for speed and functionality in Silicon based VLSI systems has caused aggressive scaling of devices, reduction in the interconnect pitch and increase in metallization levels. This aggressive interconnect scaling has resulted in increasing current densities and associated thermal effects [5, 6]. Furthermore, low dielectric constant (low-k) materials are being introduced as alternative insulators to silicon dioxide to reduce interconnect capacitance (therefore delay) and cross-talk noise to enhance circuit performance [7] and reduce power dissipation. These materials can further exacerbate thermal effects owing to their poor thermal properties.

In a VLSI system, the interconnect current densities are determined by the interconnect parameters (resistance and capacitance per unit length and interconnect length) and the buffer size driving the interconnect. Additionally, thermal effects can limit interconnect current densities in the following ways. Firstly, they limit the maximum allowable RMS current density, $j_{rms-\max}$ (since the RMS value of the current density is responsible for heat generation) in the interconnects, in order to limit the temperature increase. Secondly, interconnect lifetime (reliability) which is limited by electromigration (EM), has an exponential dependence on the inverse metal temperature [8]. Hence, temperature rise of metal interconnects due to self-heating phenomenon also limits the maximum allowed average current density, $j_{avg-\max}$, since EM capability is dependent on the average current density [9].

1.2 Previous Works

Traditionally, EM and Self-heating are not simultaneously considered for generating EM life-time guidelines for interconnects. Hunter [10], for the first time, solved the EM lifetime equation for Aluminum, and the 1-D heat equation, in a self-consistent manner which comprehended both EM and self-heating simultaneously. Recently, we have presented a methodology for analysis of the role of EM reliability and interconnect performance in determining the optimal interconnect design for advanced ULSI interconnect systems [3, 11]. However, the analysis for reliability in *signal lines* was based on EM analysis for unipolar waveforms and therefore presented a conservative current density limit. This is due to the fact that signal lines carry *bipolar* currents for which the EM lifetimes are known to be higher [12]. Furthermore, only two technology nodes based on NTRS [13] were considered. Also, since the analysis was based on NTRS data wherein global lines were not scaled, a constant metal resistivity was assumed across all technologies.

1.3 Scope of this Study

The analysis presented in this paper examines the self-consistent solutions for allowed interconnect current density for technologies up to 50 nm involving Cu and various low-k materials as per the International Technology Roadmap for Semiconductors (ITRS) [14]. Bidirectional current waveforms which are present in signal lines have been considered for the first time in this analysis which simultaneously comprehends EM and Joule heating. Since the line widths of even global wires scale with technology, one needs to consider the metal resistivity increase with technology scaling due to increased electron scattering from the interfaces [15] and because of a greater fraction of interconnect area being consumed by the barrier metal. Furthermore, prior work [3, 11] only considered current densities obtained for interconnect lines with optimal buffer insertion. For global lines, the interconnect cross-section area is large and therefore the rms current is fairly large. However, this current also flows through the contacts and vias which connect the global lines to the Silicon substrate. In this work we also quantify the reliability implications for vias and show that if minimum sized vias are used for optimal buffering of global interconnects, the metal lines may not be a reliability concern but the current densities in the vias will cause reliability concerns.

2 Preliminaries

Circuit designers are typically provided with the maximum allowable values for the average current density, j_{avg}, the RMS current density, j_{rms}, and the peak current density, j_{peak}. For a fixed temperature, EM lifetime of interconnects is known to be determined by j_{avg} [9] while self-heating is determined by j_{rms}. Presently, high performance interconnect design is based on the specified limits for the maximum values of the average, RMS, and peak current densities [16]. However, they are not self-consistent, i.e., these values do not simultaneously comprehend the two temperature dependent mechanisms: EM and self-heating.

2.1 Electromigration

EM is the transport of mass in metals under an applied current density and is widely regarded as a major wear out or failure mechanism of VLSI interconnects [8]. When current flows through the interconnect metal, an electronic wind is set up opposite to the direction of current flow. These electrons upon colliding with the metal ions, impart sufficient momentum, and displace the metal ions from their lattice sites creating vacancies. These vacancies condense to form voids that result in increase of interconnect resistance or even open circuit conditions [17]. EM lifetime reliability of metal interconnects is modeled by the well known Black's equation [8], given by,

$$TTF = A^* j^{-n} \exp\left(\frac{Q}{k_B T_m}\right) \quad (1)$$

where *TTF* is the time-to-fail (typically for 0.1% cumulative failure), A^* is a constant that is dependent on the geometry and microstructure of the interconnect, j is the DC or average current density, the exponent n is typically 2 under normal use conditions. The activation energy Q in narrow ($< 1\mu$) Copper lines is dominated by surface transport [18] and is ~ 0.5 eV [19], k_B is the Boltzmann's constant, and T_m is the metal temperature. Therefore the EM lifetime of Copper interconnects decreases as line width decreases as opposed to Al-Cu lines where EM lifetimes are known to improve with line scaling [20]. The typical goal is to achieve 10 year lifetime at 100°C, for which (1) and accelerated testing data produce a design rule value for the acceptable current density at T_{ref}, j_0.

2.2 Self-Heating

The effect of self-heating can be analyzed from the following: The metal temperature, T_m in (1) is given by,

$$T_m = T_{ref} + \Delta T_{self-heating} \tag{2}$$

and, under steady-state thermal conditions,

$$\Delta T_{self-heating} = (T_m - T_{ref}) = \frac{1}{T}\int_0^T I^2 R R_\theta \mathrm{d}t = I_{rms}^2 R R_\theta \tag{3}$$

where T_{ref} is the reference chip (silicon junction) temperature and is typically taken as 100°C to 120°C, $\Delta T_{self-heating}$ is the temperature rise of the metal interconnect due to the flow of current, R is the interconnect resistance at temperature T_m, and R_θ is the thermal impedance of the interconnect line to the substrate. This equation assumes that the frequency of interconnect current is much greater than the inverse of thermal time constant (few MHz) which implies that the metal temperature has very small variations about T_m. The reference temperature of the chip, T_{ref}, results primarily due to the total power dissipation in the chip and consists of switching, leakage, short-circuit and static power dissipation [21]. T_{ref} can be estimated from the following equation [4],

$$T_{ref} = T_0 + R_n\left(\frac{P}{A}\right) \tag{4}$$

where T_0 is the chip ambient temperature, P is total power dissipation, A is the chip area. Here R_n represents the substrate (Si) layer plus the package thermal resistance. Using (4) R_n for the present technology node (180 nm) can be calculated. Assuming the same value for R_n, the die temperatures at other technology nodes can be estimated using (4). R_n is dominated by the package thermal resistance [4]. Thus, both EM and self-heating are temperature dependent effects, and as self-heating increases, EM lifetime decreases exponentially according to (1).

3 Coupled AC Electromigration and Self-Heating Analysis

Interconnects can be broadly classified into two categories: signal lines[1] and power lines. Power and ground lines typically carry an almost constant current and therefore their EM reliability can be easily determined from the DC current density. On the other hand, current in signal lines is both positive and negative and the time-average of this current is zero. Therefore one needs to analyze the EM and self-heating of signal lines in a more rigorous manner. We now present the coupled EM and self-heating analysis for bipolar pulses. Results for unipolar case have also been provided for the purpose of comparision.

3.1 Unipolar Current Stress Condition

For unipolar current stress, it has been shown that [10]

$$r = j_0^2 \frac{\exp\left(\frac{Q}{k_B T_m}\right)}{\exp\left(\frac{Q}{k_B T_{ref}}\right)} \frac{t_{ins} t_m W_m \rho_m(T_m)}{(T_m - T_{ref}) K_{ins} W_{eff}} \tag{5}$$

where r is the effective duty factor, T_{ref} is the reference temperature, j_0 is the design rule current density stress at T_{ref} for a target minimum lifetime value (such as 10 years), t_{ins} is the insulator thickness underneath the metal, t_m is the metal line thickness (Figure 1), W_m is the metal line width, ρ_m is the metal resistivity at temperature T_m, K_{ins} is the thermal conductivity of the insulating material and W_{eff} represents the effective width from which the heat escapes from the metal line. A quasi 2-D heat conduction model [10] can be used to determine W_{eff} as

$$W_{eff} = W_m + 0.88 t_{ins}$$

which is valid for $W_m/t_{ins} > 0.4$ and is accurate to within 3% [10].

Equation (5) is a single equation in the single unknown temperature T_m. Once this self-consistent temperature is obtained the corresponding maximum allowed j_{rms} and j_{peak} can be calculated from the relationship between jrms and jpeak (caption of Figure 2) and the following equivalent expression of (3)

$$j_{rms}^2 = \frac{(T_m - T_{ref}) K_{ins} W_{eff}}{t_{ins} t_m W_m \rho_m(T_m)} \tag{6}$$

The self-consistent equation given by (5) for unipolar pulses is also valid for more general time varying waveforms with an effective duty cycle r_{eff} [22].

One of the consequences of the self-consistent equation is that, for a certain j_0, as r decreases the self-consistent temperature and the maximum allowed j_{peak} increases. This effect is shown in Figure 2 for Cu interconnects. Secondly, it can be observed that as r decreases the ratio

$$\frac{j_{peak(self-consistent)}}{j_{peak(\text{without self-heating, i.e., the line labeled } j_0/r)}}$$

decreases monotonically. At $r = 10^{-2}$, the self-consistent j_{peak} is nearly two times smaller than the j_{peak} obtained from EM constraint only, i.e., without self-heating. From the EM lifetime relation given by (1) this implies that if a design used only the average (EM) current as the design guideline without comprehending self-heating it could have a lifetime nearly three times smaller than the reliability requirement.

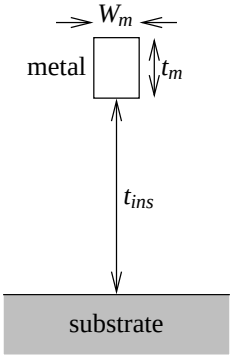


Figure 1: Cross-section of a metal interconnect over Silicon substrate.

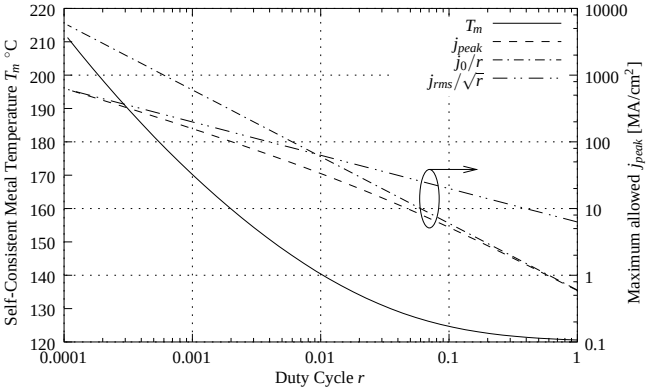


Figure 2: Self-consistent solutions of T_m and j_{peak} for metal 6 of 180 nm technology node with $j_0 = 0.6$ MA/cm^2, $\rho_m(T_m) = 2.7 \times 10^{-6}\left[1 + 6.8 \times 10^{-3}/\mathrm{K} \times (T_m - T_{ref})\right]$ Ω-cm, $T_{ref} = 120$°C and $Q = 0.5$ eV. The two dotted lines indicate j_{peak} based on (a) $j_{peak} = \frac{j_0}{r}$ and (b) $j_{peak} = \frac{j_{rms}}{\sqrt{r}}$.

[1] Clock lines and data buses are special cases of signal lines.

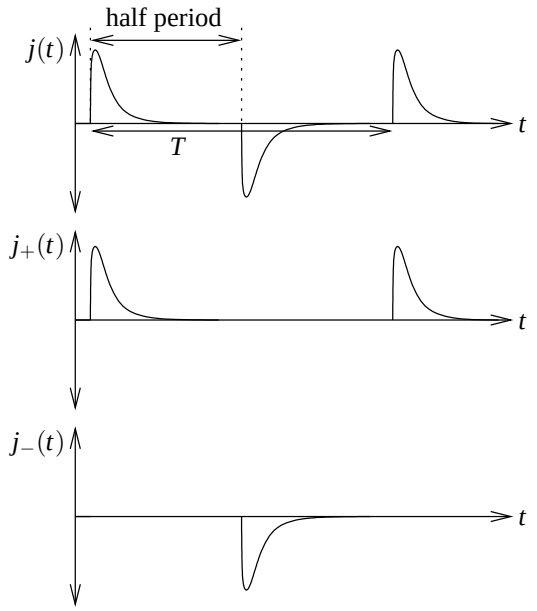


Figure 3: A bipolar pulsed waveform illustrating various current definitions.

3.2 Bipolar (AC) Current Stress Condition

As pointed out earlier, contrary to the current in power supply lines, current waveform in signal lines is both positive and negative. The average current j_{avg} is zero for these signal lines. Therefore for signal lines, the electromigration problem is not as severe as lines with unidirectional current flow. However, Joule heating is dependent on the RMS current density which is not altered. Therefore, an expression similar to (5) needs to derived for bipolar current case. Hunter [22] derived an expression for the self-consistent metal temperature for square bipolar currents. However, the current in a VLSI interconnect is not a square waveform and therefore we need to derive the expression for the self-consistent metal temperature for a general bipolar waveform.

Figure 3 shows the bipolar current density waveform $j(t)$ found in typical signal lines. Let $j_+(t)$ denote the positive excursions of the current density while $j_-(t)$ denote the negative excursions of the current density. Therefore

$$j(t) = j_+(t) + j_-(t)$$

Obviously $j_+(t)$ and $j_-(t)$ are mutually exclusive in t.

For the case of an arbitrary bipolar ac signal, detailed studies have shown that the effective ac value of current density responsible for EM, $j_{EM\ bipolar}$, is given by the Average Current Recovery (ACR) model [22] as follows:

$$\begin{aligned} j_{EM\ bipolar} &= j_{ACR} \\ &= \frac{1}{T}\left\{\int_0^T |j_+(t)|\mathrm{d}t - R\int_0^T |j_-(t)|\mathrm{d}t\right\} \end{aligned} \tag{7}$$

where j_{ACR} is the current density of the ACR model and R is a recovery parameter (< 1) of the ACR model. It heuristically accounts for the degree of healing of EM void damage that occurs when the current direction changes [22].

Now, similar to the unipolar case, in order to achieve an EM reliability lifetime goal mentioned in Section 2.1, we must have the lifetime in any ($j_{EM\ bipolar}$) current density and metal temperature T_m, equal to or larger than the lifetime value (e.g. 10 year) under the design rule current density stress j_0 at the temperature T_{ref}. Therefore we must have

$$\frac{\exp\left(\frac{Q}{k_B T_m}\right)}{j_{EM\ bipolar}^2} \geq \frac{\exp\left(\frac{Q}{k_B T_{ref}}\right)}{j_0^2} \tag{8}$$

From (8) it follows that

$$j_{EM\ bipolar} \leq j_0 \exp\left(\frac{Q}{2k_B T_m} - \frac{Q}{2k_B T_{ref}}\right) \tag{9}$$

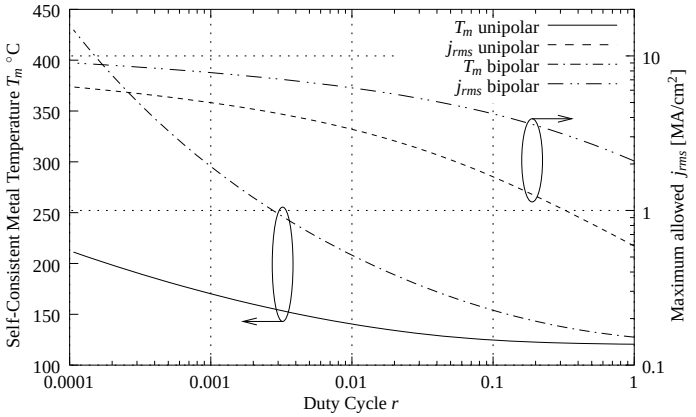


Figure 4: Self-consistent solutions of T_m and j_{peak} for metal 6 of 180 nm technology node for unipolar and bipolar pulses with $R = 0.5$. Other parameters are same as in Figure 2.

For an arbitrary bipolar pulse the average current model for EM should be replaced by the ACR model, hence it follows that

$$j_{ACR} \leq j_0 \exp\left(\frac{Q}{2k_B T_m} - \frac{Q}{2k_B T_{ref}}\right) \tag{10}$$

The current waveforms in signals lines are invariably *symmetric bipolar* waveforms. A symmetric bipolar waveform is defined as

$$\int_0^T |j_+(t)|\mathrm{d}t = \int_0^T |j_-(t)|\mathrm{d}t$$

From now on we will concentrate on developing the self-consistent equation for maximum allowed j_{peak} for symmetric bipolar current waveforms. For these waveforms, (7) can be rewritten as

$$j_{ACR} = (1-R)\frac{1}{T}\int_0^T |j_+(t)|\mathrm{d}t \tag{11}$$

Substituting (11) in (10) with the equality sign we have

$$\frac{1}{T}\int_0^T |j_+(t)|\mathrm{d}t = \frac{j_0}{1-R}\exp\left(\frac{Q}{2k_B T_m} - \frac{Q}{2k_B T_{ref}}\right) \tag{12}$$

Define the average current as

$$j_{avg\ bipolar} = \frac{1}{T}\int_0^T |j(t)|\mathrm{d}t \tag{13}$$

It follows that for a symmetric bipolar case

$$j_{avg\ bipolar} = \frac{2}{T}\int_0^T |j_+(t)|\mathrm{d}t = \frac{2}{T}\int_0^T |j_-(t)|\mathrm{d}t \tag{14}$$

Using (12)

$$j_{avg\ bipolar} = \frac{2j_0}{1-R}\exp\left(\frac{Q}{2k_B T_m} - \frac{Q}{2k_B T_{ref}}\right) \tag{15}$$

Define the equivalent duty cycle as

$$r = \frac{j_{avg\ bipolar}^2}{j_{rms}^2} \tag{16}$$

Therefore from (6) and (15)

$$r = \frac{4j_0^2 \exp\left(\frac{Q}{k_B T_m} - \frac{Q}{k_B T_{ref}}\right) t_{ins} t_m W_m \rho_m(T_m)}{(1-R)^2 (T_m - T_{ref}) K_{ins} W_{eff}} \tag{17}$$

Figure 4 compares the maximum allowed j_{rms} and metal temperature T_m for unipolar and bipolar pulses for $R = 0.5$. Note that j_{peak} will depend on the actual shape of the bipolar waveform and therefore j_{rms} is

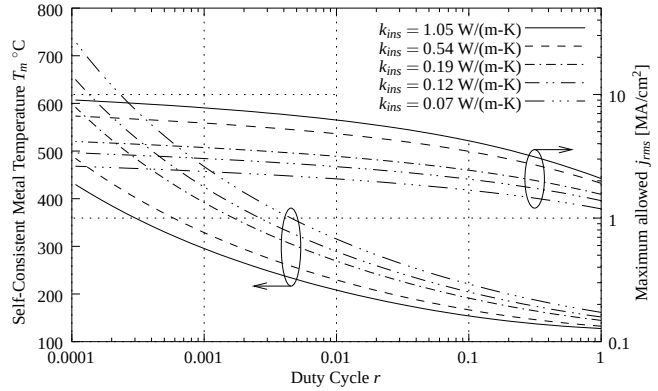


Figure 5: Self-consistent solutions for maximum allowed j_{rms} and T_m for a metal 6 in 180 nm technology for symmetric bipolar waveform for $R = 0.5$ for different dielectrics.

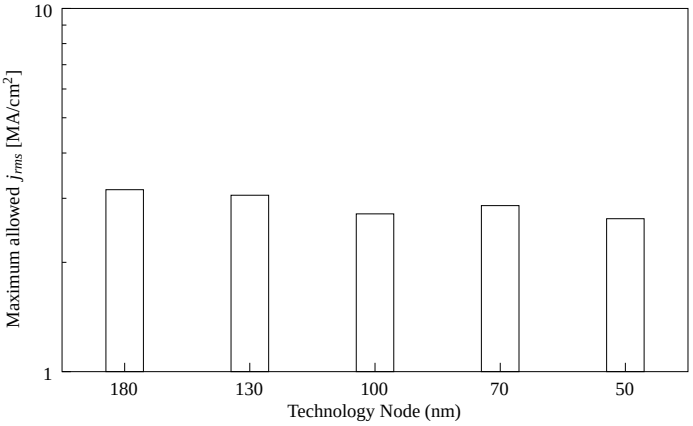


Figure 6: Maximum allowed j_{rms} for top layer metal of ITRS technologies for symmetric bipolar currents.

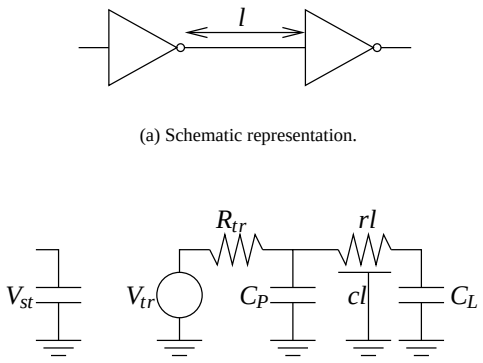
used for comparison. Equivalent duty factor as defined in (16). Note that if only half-period was considered (see Figure 3), the effective r for the bipolar case in defined in (16) would be the same as the unipolar case. From Figure 4 we observe that the maximum allowed j_{rms} increases from the unipolar case. However, as the effective duty factor decreases, the maximum allowed j_{rms} values for the two case become very similar. For instance, for $r = 1$, allowed j_{rms} for the bipolar case is $3\times$ higher than the allowed j_{rms} for the unipolar case, while at $r = 10^{-4}$, this factor is only 1.2.

4 Reliability Based Limits of Interconnect Current Densities

We now consider the technology specifications for VLSI technology process ranging from 180 nm to 50 nm as per the ITRS [14] shown in Table 1. The interconnect metal is Cu. We then solve for the self-consistent metal temperature, T_m and the corresponding maximum allowed j_{rms} and j_{peak} values for the top layer metal which has been shown to have the worst thermal characteristics [3].

We begin by analyzing the effect of introducing new dielectric materials on reliability. In Figure 5 the self-consistent values of T_m and j_{rms} are plotted as a function of duty cycle (r) for different dielectrics but using the top level metal dimensions of 180 nm technology node for symmetric bipolar current waveforms. It can be observed that j_{rms} decreases significantly as dielectrics with lower thermal conductivity are introduced. For small values of r, j_{rms} varies very slowly with r, thereby signifying the increasing importance of self-heating. Another detrimental effect of using low-k dielectric materials is that the metal temperature increases, as is evident in Figure 5 which makes these lines more susceptible to high current failures [23].

Figure 6 plots the maximum allowed j_{rms} for the top level metal lines for the ITRS technology nodes for symmetric bipolar waveforms. The duty factor r is taken to be 0.3 for all technologies except for the 50 nm technology for which $r = 0.44$. The reason for this choice is explained



(a) Schematic representation.

(b) Equivalent *RC* circuit.

Figure 7: Interconnect of length l between two identical inverters.

in Section 5. It is evident from Figure 6 that j_{rms} shows a slight decreasing trend as the technology scales. It is instructive to contrast this result with Figure 5 which shows j_{rms} variation by *only* considering different dielectric materials while the interconnect geometry is not scaled. From Figure 5 it can be observed that if interconnect geometry is not scaled, maximum allowed j_{peak} decreases by a factor of 2.25 from 180 nm technology to 50 nm technology node due to decreasing thermal conductivity of dielectrics. If scaled interconnects as per ITRS specifications are considered j_{rms} reduces by only 16.8%. Therefore for isolated lines, scaling of interconnect geometries helps to offset the detrimental effects of using dielectric materials with poor thermal properties.

5 Performance Based Interconnect Current Densities

As a next step we outline a methodology for computing current density from performance considerations only. Consider an interconnect of length l between two buffers. The schematic representation is shown in Figure 7(a). Figure 7(b) shows an equivalent RC circuit for the system. The voltage source (V_{tr}) is assumed to switch instantaneously when voltage at the input capacitor (V_{st}) reaches a fraction x, $0 \le x \le 1$ of the total swing. Hence the overall delay of one segment is given by:

$$\tau = b(x)R_{tr}(C_L + C_P) + b(x)(cR_{tr} + rC_L)l + a(x)rcl^2 \qquad (18)$$

where $a(x)$ and $b(x)$ only depend on the switching model, i.e., x. For instance, for $x = 0.5$, $a = 0.4$ and $b = 0.7$ [24]. If r_0, c_0 and c_p are the resistance, input and parasitic output capacitances of a minimum sized inverter respectively then R_{tr} can be written as r_0/s where s is size of the inverter in multiples of minimum sized inverters. Similarly $C_P = sc_p$ and $C_L = sc_0$. If the total interconnect of length L is divided into n segments of length $l = L/n$, then the overall delay is given by,

$$T_{delay} = \frac{L}{l}b(x)r_0(c_0 + c_p) + b(x)\left(c\frac{r_0}{s} + src_0\right)L + a(x)rclL \qquad (19)$$

It should be noted in the above equation that s and l appear separately and therefore T_{delay} can be optimized separately for s and l. The optimum values of l and s are given as:

$$l_{opt} = \sqrt{\frac{b(x)r_0(c_0 + c_p)}{a(x)rc}} \qquad (20)$$

$$s_{opt} = \sqrt{\frac{r_0 c}{rc_0}} \qquad (21)$$

Note that s_{opt} is independent of the switching model, i.e., x.

Since, for deep sub-micron technologies, a significant fraction of interconnect capacitance, c, is contributed by coupling and fringing capacitances to neighbouring lines as shown in Figure 8, we performed a full 3D-capacitance extraction using FASTCAP [25] for signal lines at global metal levels to obtain the values of c.

Tech.	ε_r	k_{ins} (W/(m-K))	Local Tier				Semiglobal Tier				Global Tier			
			n	w_m	t_m	t_{ild}	n	w_m	t_m	t_{ild}	n	w_m	t_m	t_{ild}
180	3.75	1.05	2	250	350	350	2	320	640	672	2	525	1155	1260
130	3.1	0.54	3	182.5	273.75	273.75	2	232.5	511.5	488.25	2	382.5	956.25	1032.75
100	1.9	0.19	3	132.5	225.25	225.25	3	170	408	374	2	280	756	784
70	1.5	0.12	3	92.5	175.75	125.75	3	120	300	276	3	195	546	565.5
50	1.25	0.07	3	65	136.5	136.5	3	82.5	222.75	198	3	137.5	398.75	412.5

Table 1: ITRS interconnect parameters for 180 nm to 50 nm technologies. All dimensions are in nm. Pitch is twice the width for all cases. n is the number of layers in the current tier. t_{ild} is the inter-layer dielectric thickness.

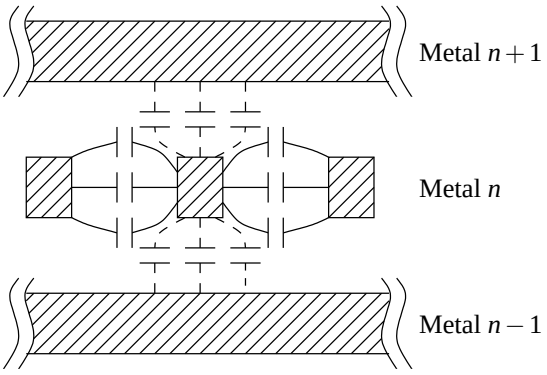


Figure 8: Typical metal interconnect structure.

Tech.	l_{opt} (mm)	s_{opt}	j_{rms} (MA/cm^2)	$j_{avg\ bipolar}$ (MA/cm^2)	r
180	3.33	174	0.622	0.339	0.297
130	2.5	151	0.66	0.368	0.311
100	2.22	110	0.61	0.34	0.311
70	1.32	82	0.66	0.373	0.319
50	1.06	53	0.46	0.302	0.431

Table 2: Optimized interconnect and buffer parameters for global tier for various ITRS technology nodes.

This inverter-interconnect structure can be simulated using SPICE to obtain the interconnect current waveforms along the interconnect. In order to compare the current densities using SPICE simulations and those computed in Section 4, an appropriate value of r needs to be chosen for simulations. Since these lines are mostly global tier interconnects, they are expected to carry signals at almost every clock cycle unless the block they are communicating to is powered down. Therefore this inverter-interconnect structure is used as a delay stage in a multi-stage ring oscillator and the current waveforms and current densities along the interconnect are obtained. These current waveforms and (16) are used to determine the equivalent duty factor. Table 2 summarizes these values for various ITRS technologies.

In practice, the input capacitance C_L of the inverter is almost constant but the output resistance R_{tr} and output parasitic capacitance C_P are voltage dependent and therefore change during the output transition. Therefore accurate values of optimal interconnect length and buffer size need to be determined by SPICE simulations. For this, we take advantage of the fact that the optimal interconnect length does not depend on the buffer size. Therefore, we first set the buffer size to an appropriate value and sweep the interconnect length and find the optimum length which minimizes the ratio of the ring oscillator stage delay and interconnect length. Using this optimum length, we subsequently sweep buffer sizes and find the optimum buffer size which minimizes ratio of the stage delay and interconnect length. This allows us to obtain the values of l_{opt} and s_{opt} taking into account the bias dependence of transistor resistances and capacitances and the switching model.

Note that due to the distributed nature of the interconnect, the maximum current density occurs close to the buffer output. Hence, we need to verify whether this maximum current density, which is obtained from performance considerations ($j_{performance}$) only, also meets the EM current density limits ($j_{reliability}$) obtained earlier using the self-consistent approach.

Also, the relative rise and fall skew was found to be same across all technologies. From our simulations it was observed that drivers and interconnects optimized using (21) and (20), maintain good slew rates for rising and falling transitions across all technologies, except the 50 nm node, with an effective duty cycle ($r = j^2_{avg\ bipolar}/j^2_{rms}$) of 0.31 ± 0.01 as shown in Table 2. r is higher for 50 nm technology node because the transistors don't switch off completely (according to the BSIM3 models) and therefore interconnect waveform is affected. Since for the signal lines the current waveform is symmetric and bipolar, $j_{avg\ bipolar}$ is computed over half the time-period to obtain r.

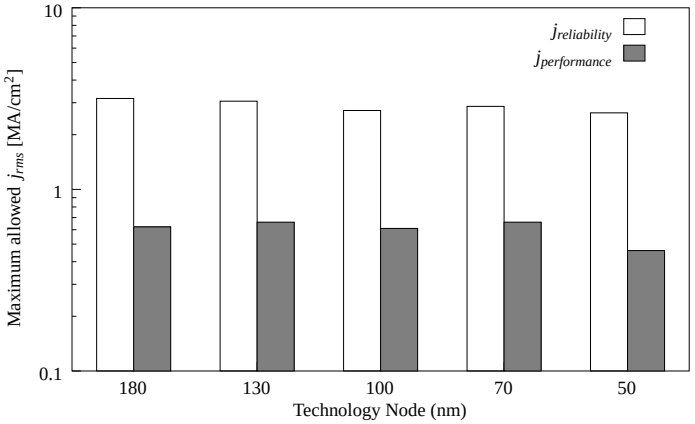


Figure 9: Comparison of j_{rms} values obtained from reliability and electrical performance considerations for top layer metal for various ITRS technology nodes.

Figure 9 shows the comparison of $j_{performance}$ with the values of $j_{reliability}$ for various technology nodes. It can be observed that $j_{performance}$ is always lower than $j_{reliability}$ for all technologies. This implies that optimum interconnect length of an isolated signal is determined solely by performance considerations.

6 Effect of Interconnect Dimension on Copper Resistivity

The experiments in the previous section were carried out assuming that the metal resistivity does not change with line width. In an actual VLSI interconnect, metal resistivity starts increasing as the minimum dimension of the metal line becomes comparable to the *mean free path* of the electrons (i.e., interconnect metal is considered to be a *thin-film*). This is because surface scattering starts having a non-negligible contribution to the resistivity compared to the contribution due to bulk scattering. Furthermore, surface scattering also reduces the thermal coefficient of resistivity of material.

Another effect which is responsible for increased resistivity is the presence of barrier material for Copper interconnects. Since the resistivity of the barrier material is extremely high compared to Copper, it can be assumed that all the current is carried by Copper. Therefore the effective area through which the current conduction takes place reduces, or equivalently the effective resistivity of the metal line of the same drawn dimension increases. This becomes more of a problem as metal lines scale since it is very difficult to scale the thickness of the barrier material [26].

According to [27] the resistivity, ρ, of a thin-film metal can be expressed in terms of bulk resistivity ρ_0 as

$$\frac{\rho_0}{\rho} = 1 - \frac{3}{2k}(1-p)\int_1^\infty \left(\frac{1}{x^3} - \frac{1}{x^5}\right)\frac{1-e^{-kx}}{1-pe^{-kx}}\mathrm{d}x$$

Tech.	w_m	$\frac{\rho}{\rho_0}$ (thin-film)	$\frac{\rho}{\rho_0}$ (barrier)	$\left[\frac{\rho}{\rho_0}\right]_{eff}$	$\frac{\alpha}{\alpha_0}$
180	525	1.0162	1.0487	1.0657	0.9527
130	382.5	1.0224	1.0663	1.0902	0.9353
100	280	1.0308	1.0914	1.1250	0.9122
70	195	1.0448	1.1351	1.1859	0.8752
50	137.5	1.0646	1.2003	1.2779	0.8263

Table 3: Resistivity and temperature coefficient ratios for the global tier metals for various technologies. All dimensions in nm. Barrier thickness of 10 nm assumed for all technology nodes.

Tech.	l_{opt} (mm)	s_{opt}	j_{rms} (MA/cm^2)	$j_{avg\ bipolar}$ (MA/cm^2)	r
180	3.0	179	0.633	0.344	0.296
130	2.4	146	0.643	0.353	0.302
100	2.12	96	0.559	0.311	0.310
70	1.2	82	0.626	0.361	0.332
50	0.99	48	0.400	0.263	0.432

Table 4: Optimized interconnect and buffer parameters for global tier for various ITRS technology nodes taking into account increased resistivity due to surface scattering and barrier materials.

where $k = d/\lambda_{mfp}$, d is the smallest dimension of the film (in our case, the width), λ_{mfp} is the bulk mean free path of electrons and p is fraction of electrons which are elastically reflected at the surface. For Copper, $p = 0.47$ and $\lambda_{mfp} = 421$Å at 0° C [15]. Moreover, since the temperature alters the mean free path of the electrons, the temperature coefficient α of the thin film of metal is also different from its bulk value. α can be related to the bulk temperature coefficient α_0 as [27]

$$\frac{\alpha}{\alpha_0} = \frac{1-\frac{3}{k}(1-p)\int_1^\infty\left(\frac{1}{x^3}-\frac{1}{x^5}\right)\frac{1-e^{-kx}}{1-pe^{-kx}}dx+\frac{3}{2}(1-p)^2\int_1^\infty\left(\frac{1}{x^2}-\frac{1}{x^4}\right)\frac{e^{-kx}}{(1-pe^{-kx})^2}dx}{1-\frac{3}{2k}(1-p)\int_1^\infty\left(\frac{1}{x^3}-\frac{1}{x^5}\right)\frac{1-e^{-kx}}{1-pe^{-kx}}dx}$$

The resistivity and temperature coefficient ratios for the global tier metals for various technologies is given in Table 3. Table 4 shows l_{opt}, s_{opt}, j_{rms}, $j_{avg\ bipolar}$ and r values recalculated taking into account increased resistivity due to surface scattering and the presence of barrier materials. Figure 10 shows the $j_{rms\ reliability}$ and $j_{rms\ performance}$ considering the increased metal resistivity and decrease thermal coefficient of resistivity due to decreasing metal line width. It can be seen that both $j_{rms\ reliability}$ and $j_{rms\ performance}$ reduce slightly as compared to the case when bulk values are used.

Another effect that can cause metal resistivity to increase is skin effect. This is normally observed at high frequencies at which the current gets confined almost entirely to a very thin sheet at the surface of the conductor. The thickness of this sheet, known as the skin depth, determines the effective cross sectional area of the conductor and its resistance. The skin depth (δ) is given by [28],

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{22}$$

Here the frequency $f = \omega/2\pi$, and μ and σ are the permeability and conductivity of the interconnect material respectively. It was found that for skin effect to start impacting the line resistance, the thickness of Cu lines needs to be larger than 2.089 μm for 1 GHz and 0.661 μm for 10 GHz signals. Since the dimensions of the global Cu lines used in this study were $\ll 1$ μm, skin effect is not expected to impact the resistivity of these lines at least for frequencies upto 10 GHz.

7 Thermal Coupling in 3-D Interconnect Arrays

In this section we will briefly address the issue of thermal coupling in VLSI interconnects. Our self-consistent analysis of self-heating and EM effects presented earlier in Sections 3.1 and 3.2 were based on single isolated interconnect lines. In a real IC there are densely packed layers of interconnect lines which form a 3-D array. The self-heating of interconnect lines within such array could be significantly more severe due to thermal coupling between neighbouring lines [5]. The heat flow analysis for such structures is complicated and must involve numerical simulation techniques such as finite element method.

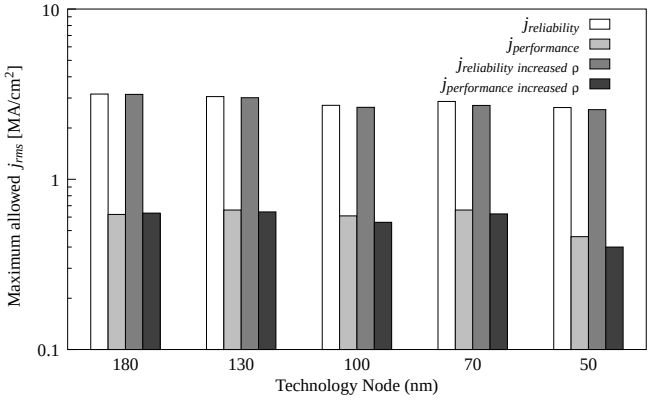


Figure 10: Comparison of j_{rms} values obtained from reliability and electrical performance considerations for top layer metal for various ITRS technology nodes with and without taking into account increased resistivity due to surface scattering and barrier materials.

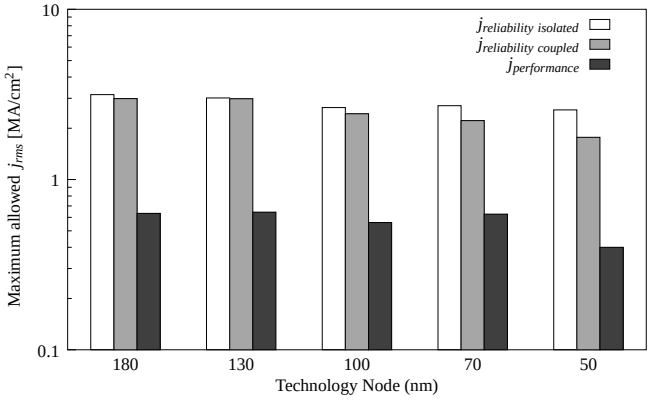


Figure 11: Maximum allowed j_{rms} for top layer metal of ITRS technologies for symmetric bipolar currents with and without thermal coupling from neighbouring lines. Also shown is the j_{rms} from performance considerations.

The RMS current density can be empirically shown to obey the following relationship

$$j_{rms}^2 \propto \frac{T_m - T_{ref}}{\rho_m(T_m)} \tag{23}$$

and the proportionality constant κ (which is independent of the interconnect material) can be obtained empirically from the finite element analysis. In our work we use the results presented in [4] which include coupling between interconnects at all metal layers.

Substituting (23) and (15) in equation (16), we can obtain another self-consistent equation similar to (17)

$$r = \frac{4j_0^2\exp\left(\frac{Q}{k_BT_m}-\frac{Q}{k_BT_{ref}}\right)\rho_m(T_m)}{(1-R)^2(T_m-T_{ref})\kappa} \tag{24}$$

From this we can calculate the maximum allowed j_{rms} for densely packed metal lines. Figure 11 compares this with the j_{rms} obtained from Figure 10 for isolated metal lines. We find that the maximum allowed j_{rms} reduces for the 3-D case, where all the metal lines are heated with equal current load in all the leads. Moreover, with technology scaling, the percentage reduction in j_{rms} due to coupling from neighbouring lines increases, therefore $j_{rms\ reliability}$ comes closer to $j_{rms\ performance}$ as the technologies scale.

8 Reliability Issues in Vias

In this section we investigate the possible cases when the performance based rms current density may potentially exceed the reliability rms current limit. We first examine the case of global interconnects when the buffer size is increased beyond s_{opt}. Figure 12 plots the rms current density as a function of buffer size driving an interconnect of length l_{opt} as obtained from SPICE simulations. We observe that j_{rms} saturates at a

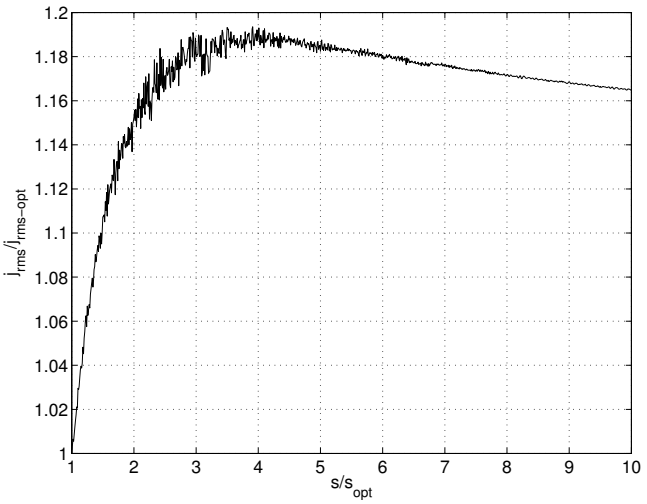


Figure 12: j_{rms} as a function buffer size for an interconnect length of l_{opt} for the 100 nm technology node.

Tech.	j_{rms} (MA/cm^2)	minimum area (μ^2)	via area (local tier) (μ^2)
180	4.18494	0.091718	0.049087
130	4.14404	0.056753	0.026159
100	4.09105	0.028924	0.013789
70	3.95897	0.016835	0.067201
50	3.50195	0.0062626	0.0033183

Table 5: Maximum allowed j_{rms} for a via and minimum via area for various technology nodes.

value of approximately $1.2 \times j_{rms-opt}$ which is well below the reliability limit. The rms current density in global interconnects becomes more than the reliability current density if the buffer size exceeds $3 \times s_{opt}$ and the interconnect length is less than 5μ. This is highly unlikely in any practical design.

We now investigate whether rms current density in vias used in these large buffers can exceed the reliability limit. In a technology with multiple levels of interconnect, the buffers are connected to the global lines by a series of vias and possibly short interconnects at intermediate layers of metal if the technology does not allow stack vias. The vias at the local and semiglobal layers are pitch-matched to the interconnects at these layers. However, they are carrying the same current as the global metal layers and therefore can potentially be a thermal reliability concern. For Copper vias, (23) holds (with a different proportionality constant κ_{via}). Therefore an equation of the form (24) can be derived for Copper vias as well which can be used to calculate the maximum allowed j_{rms} for the via. In our work, κ_{via} was determined using the measured value of temperature rise ($T_{via} - T_{ref}$) for a given current density (j_{rms}) [29]. These values are summarized in Table 5 for various ITRS technology nodes along with the minimum via area such that the current density in the via due to performance considerations is equal to the maximum allowed j_{rms} from thermal and reliability considerations. Also shown are the areas of minimum sized vias at the local tier as per the ITRS. It can be observed that for optimally buffered global lines, in order to meet the thermal reliability constraints, the area of the via at the local tier should be at least three times the area of the minimum sized via at that tier.

9 Summary

In conclusion, this paper has highlighted an important physical design issue in deep submicron ICs arising from interconnect reliability due to electromigration and thermal effects. It has been shown that for long (global) signal lines that require optimal buffering for delay minimization, performance based current density limits in the minimum sized vias can conflict with those based on reliability and thermal effects.

A rigorous coupled analysis of electromigration under bipolar stress conditions that are prevalent in signal lines, and thermal effects arising due to Joule heating of the wires have been presented for the first time. The analysis has been applied to study the effect of technology scaling using ITRS data, wherein the effects of increasing interconnect (Cu) resistivity with line dimensions, the effect of a finite barrier metal thickness and thermal coupling between wires have been included. Finally, the reliability implications for minimum sized vias in optimally buffered signal nets have also been quantified. This analysis suggests that for the optimally buffered interconnects, while the current density in the line remains limited by the performance, the current density in the vias significantly exceeds the reliability based limits, which has important implications for the physical design process flow and various optimization techniques.

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