Classical Floorplanning Harmful?*

Andrew B. Kahng
UCLA Computer Science Department
3713 Boelter Hall
Los Angeles, CA 90095-1596 USA
abk@cs.ucla.edu

ABSTRACT

Classical floorplanning formulations may lead researchers to solve the wrong problems. This paper points out several examples, including (i) the preoccupation with packing-driven, as opposed to connectivity-driven, problem formulations and benchmarking standards; (ii) the preoccupation with rectangular (and L or T shaped) block shapes; and (iii) the lack of attention to algorithm scalability, fixed-die layout requirements, and the overall RTL-down methodology context. The right problem formulations must match the purpose and context of prevailing RTL-down design methodologies, and must be neither overconstrained nor underconstrained. The right solution ingredients are those which are scalable while delivering good solution quality according to relevant metrics. We also describe new problem formulations and solution ingredients, notably a *perfect rectilinear floorplanning* formulation that seeks zero-whitespace, perfectly packed rectilinear floorplans in a fixed-die regime. The paper closes with a list of questions for future research.

Categories and Subject Descriptors

B.7.2 [**Hardware**]: Integrated Circuits— *design aids; placement and routing*; F.2.2 [**Theory of Computation**]: Analysis of Algorithms and Problem Complexity—*geometrical problems and computations; routing and layout*

General Terms

VLSI floorplanning, coarse placement, block packing and layout, hierarchical design methodology.

1. INTRODUCTION

Classical floorplanning takes as input a set of blocks, a netlist, and a target layout region. The (rectangular) blocks may be *hard*, *soft* or *semi-soft*. Hard blocks have fixed aspect ratio and pin locations. Soft blocks have fixed area, with (upper- and lower-bounded) continuously variable aspect ratio. Semi-soft blocks have fixed area with discrete allowed aspect ratio, usually corresponding to alternative block realizations (e.g., allowed foldings of datapaths).[1] Since the mid-1990s, L- and T-shaped block shapes have been specifiable and/or permissible; this is motivated by enforced colocation of a datapath block with related control, or the shape of particular types of datapath blocks. The target layout region is typically specified by upper and lower bounds on its aspect ratio, e.g., a square layout has upper bound = lower bound = 1.

The classical floorplanning problem seeks to shape and pack all blocks, such that no blocks overlap and the enclosing layout region has minimum area while satisfying aspect ratio constraints. This corresponds to a *minimum whitespace* objective. Optionally, the packing can attempt to minimize an estimate of the wiring needed to realize the netlist connectivity. This corresponds to a *minimum wirelength* objective.[2] With respect to wiring, early works such as [13] focused on channeled block layouts and the associated global routing and pin assignment issues. Today, for various reasons – fixed-die regime, presynthesis floorplanning, N-layer metal with available over-the-block routing – channelless layouts are the norm and the top-level routing is more or less viewed (or more accurately, ignored) as "area-routed".

This invited paper addresses the question, "Classical floorplanning harmful?" The "classical floorplanning" problem has inspired an immense literature of valuable research results. Nevertheless, "classical floorplanning" has in several ways led researchers and practitioners to focus on the wrong problem. Examples include (i) preoccupation with packing driven, as opposed to connectivity driven, problem formulations and benchmarking practices; (ii) preoccupation with only rectangular (and L- or T-shaped) block shapes; (iii) lack of attention to the fixed-die context; (iv) lack of attention to the overall RTL-down methodology context, and to whether there are any real differences between "floorplanning" and "hierarchical approaches to achieving placement"; and (v) lack of attention to achieving a holistic, scalable approach. The main conclusion is that *the problem must be changed.* The right problem formulations must match the purpose of floorplanning (i.e., coarse placement enabling

*This research supported by Cadence Design Systems, Inc. and the MARCO Gigascale Silicon Research Center.

ISPD 2000, San Diego, CA.

[1] An alternative taxonomy lumps soft blocks together with semi-soft blocks: since the layout region is row-based, block heights are discrete and there is no such thing as a block with continuously variable aspect ratio.

[2] The minimum wirelength objective is not yet consistently addressed in either the definition or the reporting of benchmarks in the literature.